The future of bent MAPS, full-wafer (stitched) design: status and challenges

Magnus Mager (CERN)
on behalf of the ALICE collaboration

13th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD13), Vancouver, Canada
Overview

- **Introduction & Motivation**
  - Monolithic Active Pixel Sensors
  - stitching
  - bending

- **Challenges**
  - power (dissipation/distribution)
  - yield (mitigation strategies)

- **Two stitched prototypes**
  - design approaches
  - first characterisation results

- **Next steps**
Monolithic Active Pixel Sensors (MAPS)

Reminder

- **Quadruple well process**: deep p-well to allow CMOS circuitry inside matrix
- **Detection layer**: 10-30 μm high-resistive epitaxial
- **Small collection electrode**: large Q/C, low power consumption
- **Thickness**: ~50 μm (!)
**Full depletion**
faster and more radiation tolerant

- Addition of a **low-dose n-implant**
  - developed together with foundry

- Now crucial for the 65 nm development

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**Partially depleted epitaxial layer**
Charge collection time < 30 ns
Operational up to $10^{14}$ 1 MeV $n_{eq}/cm^2$

**Fully depleted epitaxial layer**
Charge collection time < 1 ns
after further improvements (outside ALICE):
operational up to $10^{15}$ 1 MeV $n_{eq}/cm^2$

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Developed and prototyped within ALPIDE R&D

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[doi:10.3390/s8095336]
Qualification of 65 nm CMOS
TPSCo 65 nm CMOS Imaging Technology

- Concentrated effort **ALICE ITS3** together with **CERN EP R&D**

- **Key benefits**
  - smaller features/transistors: higher integration density
  - smaller pitches
  - lower power consumption
  - **larger wafers** (200→300 mm)

- **Verification:**
  - comprehensive *first* submission: **55** prototype chips
  - goal: qualify the technology for radiation hardness and particle detection (**achieved**)
Qualification of 65 nm CMOS process variants

- Following the experience with 180 nm, the 65 nm CIS process could be modified
- Three different designs “standard”, “modified”, “modified with gap” are tried
  - modified with gap is the default for the next developments
- Largely increases the charge collection speed and radiation hardness
- Lowers the charge spread / cluster size → more signal per pixel
Qualification of 65 nm CMOS selected results

- Intrinsic time resolutions of 77 ps for 10 μm pixels
- >99% detection efficiency even after $10^{15}$ NIEL for 15 μm pixels at room temperature

Excellent performances of the 65 nm technology have been established experimentally.
Wafer-scale sensors: stitching introduction

- Chip size is traditionally limited by CMOS manufacturing ("reticle size")
  - typical sizes of few cm$^2$
  - modules are tiled with chips connected to a flexible printed circuit board
Wafer-scale sensors: stitching introduction

- Chip size is traditionally limited by CMOS manufacturing ("reticle size")
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  - modules are tiled with chips connected to a flexible printed circuit board

- New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  - actively used in industry
  - a 300 mm wafer can house a chip to equip a full half-layer
  - requires dedicated chip design
Stitching
simplified principle

what we “design”

what we want to fabricate

wafer
(Ø=300 mm)

reticle
(mask)
Stitching
simplified principle

- top part

wafer ($\varnothing=300$ mm)

reticle (mask)
Stitching
simplified principle

- repeated part (1)
Stitching simplified principle

- repeated part (2)

wafer ($\varnothing=300$ mm)

reticle (mask)
Stitching
simplified principle

- repeated part (3)

wafer
(⌀=300 mm)

reticle
(mask)
Stitching simplified principle

- final circuit is a concatenation of different parts of the masks

![Diagram of wafer and reticle (mask)]
Flexibility of silicon systematically

- **Monolithic Active Pixel Sensors** are quite flexible

- Bending force scales as \( (\text{thickness})^{-3} \)
  - large benefit from thinner sensors

![Graph showing bending force vs. displacement for different thicknesses.](image)

### Graph Details:
- **Channels**:
  - 97 μm (8x)
  - 50 μm (1x)
  - 40 μm
  - 30 μm
- **Parameters**:
  - L = 12 m
- **Legend**:
  - Each line represents a different thickness, with 97 μm being the thickest and 30 μm the thinnest.

Magnus Mager (CERN) | Stitched MAPS | HSTD13 | 07.12.2023 | 15
Flexibility of silicon

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![Graph showing force vs. displacement for different thicknesses of silicon](image)

- 97 μm (/8)
- 50 μm (x1)
- 40 μm
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$L = 12 \text{ m}$
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![Image of testing setup and graph showing force vs. displacement for different thicknesses of sensors. The graph indicates that as the thickness decreases, the bending force increases significantly.]
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Bending of fully processed wafers (48x speedup)
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Motivation: material budget

- Reduction to 1/7th
- By removing support mechanics, colling, and FPC

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- $R = 18, 24, 30$ mm (beam pipe: 16 mm)
- $L \sim 28$ cm

→ Jian's ITS3 presentation
Challenges: powering power consumption

- Power consumption directly impacts material budget
  - power supply (metal, possibly circuit boards)
  - cooling (pipes, water, …)

- To take full advantage of the stitching, an operation with air cooling is wanted, setting a limit around 20-40 mW/cm²

- Off-state leakage is crucial in 65 nm
  - dedicated versions of standard cells are being designed
  - operating temperature needs to be contained

- Also worst process corners are to be watched out very carefully

<table>
<thead>
<tr>
<th></th>
<th>Power density [mW cm⁻²]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Expected 25 °C</td>
</tr>
<tr>
<td>Left End Cap (LEC)</td>
<td>791</td>
</tr>
<tr>
<td>Active area (RSU)</td>
<td>28</td>
</tr>
<tr>
<td></td>
<td>44</td>
</tr>
<tr>
<td></td>
<td>62</td>
</tr>
<tr>
<td>Pixel matrix</td>
<td>15</td>
</tr>
<tr>
<td>Biasing</td>
<td>168</td>
</tr>
<tr>
<td>Readout peripheries</td>
<td>432</td>
</tr>
<tr>
<td>Data backbone</td>
<td>719</td>
</tr>
<tr>
<td></td>
<td>719</td>
</tr>
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<td>719</td>
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</table>
Challenges: powering power distribution

- 65 nm has a core voltage of 1.2 V
  - low power consumption
  - little voltage margin

- Sensor is ideally connected only at the short sides

- Local voltage regulators:
  - possible, but overall power consumption will increase

- Conductivity of metal layers is imposing a limit

\[ \Delta V = k \left( \frac{\rho}{t} \right) J z^2 = k \left( \frac{\rho}{t} \right) \frac{P_S}{V_0} z^2 \]

Low-power design is key!
Challenges: yield
defect density and mitigation

- A wafer with a reasonably complex designs and w/o defects does not exist
- It is key to deal with imperfections and defects smartly
- Twofold strategy:
  - design critical (global) circuits very cautiously (large spacing)
  - allow to disable malfunctioning parts (masking, power-off)
- First prototypes to address the sensitivity and density of faults on different circuit plots (more on next slides)
  - MOSS: separate power domains for large pieces of a sensor
  - MOST: switches per small groups of pixels
Chip development roadmap
status and plans

- **MLR1:** first MAPS in TPSCo 65nm (2021)
  - successfully qualified the 65nm process for particle detectors

- **ER1:** first stitched MAPS (2023)
  - large design “exercise”
  - “MOSS”: 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 μm²): conservative design, different pitches
  - “MOST”: 2.5 x 259 mm, 0.9 MPixel (18 x 18 μm²): more dense design

- **ER2:** first ITS3 sensor prototype (2024)

- **ER3:** ITS3 sensor production (2025)
Prototypes: handling

ER1

- ER1 wafers are thinned down to 50 μm
- Tools to pick, handle and ship chips have been developed

A set of dedicated tools have been developed — handling is under control
Prototypes: handling
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ER1 test systems

MOSS

MOSS CHIP Carrier Card

Proximity_v2 Board

Proximity_v2 Board

Proximity_v2 Board

Proximity_v2 Board

Test system scale in size as the sensors do

MOST

+ same FPGA board (x1) as MOSS

+ oscilloscope for readout
Prototypes: MOSS design (1/2)

- MOSS is segmented into:
  - 10 repeated sensor units (RSU)
  - top and bottom halves with different pitches (22.5 and 18µm)
  - four different sub-matrices each with different analog designs

- Each half RSU is powered and can be tested independently
  - goal: understanding of yields and possible defects
  - difficulty: large number of power domains

- Stitched “back-bone” allows to control and readout the sensor from the left short side

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Stitched “back-bone” allows to control and readout the sensor from the left short side.
Prototypes: MOSS design (2/2)

- 1.4 x 26 cm monolithic stitched sensor

- 256 x 256 pixels
- 320 x 320 pixels
- LARGE PITCH PIXELS (22.5 μm)
- FINE PITCH PIXELS (18 μm)

Pitch 22.5 μm
- Conservative layout
- 7 mW/cm² (analog FE)
- 1μs peaking time

Pitch 18 μm
- Compact layout
- 11 mW/cm² (analog FE)
- 1μs peaking time
MOSS lab testing
power tests

- Powering up the large chip is not easy
  - some important learnings were made here for the next chip iteration (ER2)

- Current results are based on a very gentle and careful powering
  - “you cannot repeat the first power up”
  - subsequently allowing larger margins continues to increase the “yield”

- A large wafer-wafer spread is observed
  - compatible with first findings from the second prototype (MOST)

- “Powerable” units are also functionally working (slow control)
MOSS test beams

- Several campaigns in 2023
- Works out of the box
- Parameters still to be optimised and data to be analysed in more detail
- But very encouraging result!
MOSS test beams
Detection efficiencies and fake-hit rates

MOSS-4_W24B5_T6
Pitch: 22.5 μm
Type: 5 μm gap
$\textbf{I_{bias}} = 62$ DAC
$\textbf{I_{biasn}} = 100$ DAC
$\textbf{I_{reset}} = 10$ DAC
$\textbf{I_{db}} = 50$ DAC
$V_{\text{shift}} = 192$ DAC
$V_{\text{casn}} = 64$ DAC
$V_{\text{psub}} = 0$ V (via 0 Ω)
Strobe length: 6 μs
$T = 30{^{\circ}}C$

ALICE ITS3 beam test \textit{preliminary},
@ CERN PS September 2023,
10 GeV/c hadrons,
Plotted on 23 Nov 2023

Operational with a bit of margin — NB: bias settings are still being optimised
MOSS test beams
spatial resolutions and cluster sizes

Spatial resolutions and cluster sizes match those of small prototypes
Prototypes: MOST design (1/2)

- MOST is based on a very densely integrated pixel matrix

- Power is distributed globally
  - yield is addressed by a highly granular set of switches that allow to turn off faulty parts locally

- Readout is purely asynchronous and hit-driven
  - low power consumption + timing information
Prototypes: MOST design (2/2)

- Each set of 4 pixels contains a local oscillator and address serialiser
  - only active when a hit is detected
- Signal is buffered several times along chip
- Sharing of the same transmission channels along a column
Digital pulsing & readout concept

- A test pulse can be fed at the bottom - travels across the full chip to the top - and then back

- Fired pixels send their address to the bottom - as serial bitstream of \(~1\text{Gbit/s}\) - there are 256 of these lines on MOST (4 per column)

- Total round trip is expected to be of \(O(200\ \text{ns})\) for the top most stitch

- Pulsing and readout signal each go via up to **880 repeaters over 26 cm**
Pulsing & readout measurement

- All 256 readout lines work across the full length of the chip/across all stitches

- Decoding of pixel addresses work nicely

- Tests of the analog front-ends are starting (they are alive, stay tuned for more soon)
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- Tests of the analog front-ends are starting (they are alive, stay tuned for more soon)
Next steps
MOSAIX (ER2) (1/2)

▶ “MOSAIX” is being designed
  - a real sensor with all functionality
  - to be used in an experiment (ALICE ITS3)

▶ Learnings from MOSS and MOST on stitching are folded into the design
  - powering granularity has been adjusted: 20→144 per segment
  - introduction of on-chip power switches

▶ Interfaces with off-detector electronics are incorporated

▶ New low-leakage standard cell library

▶ Stitching plan fixed and under review with foundry
Next steps
MOSAIX (ER2) (2/2)

- Left end cap circuit
  - like a separate “readout chip”
- 12 repeated units with 12 independent matrices each
- Design ongoing, plan to submit in fall 2024
Summary

- **Stitched, wafer-scale MAPS** offer a unique possibility to build ultra-light, highly granular detectors

- **Bending** of 50 μm-thick chips and wafers is exercised routinely

- **Two key design challenges** are being dealt with:
  - power
  - yield

- Two 26 cm long, stitched prototypes ("MOSS", "MOST") have been fabricated in a first engineering rung ("ER1") in TPSCo 65 nm
  - both work!
  - detailed characterisation is ongoing

- Next step: integration of a sensor that can be used on a detector ("MOSAIX")
  - design is ongoing for submission in fall 2024
Thank you!
MOSS probe testing on wafer level

- Dedicated needle card for MOSS ready
- Compatible with test system for chips on carriers
  - first functional tests of MOSS were actually done using this needle card
- Systematic impedance tests carried out for 8 wafers
MOSS probe testing
Impedance measurements

under detailed analysis right now!