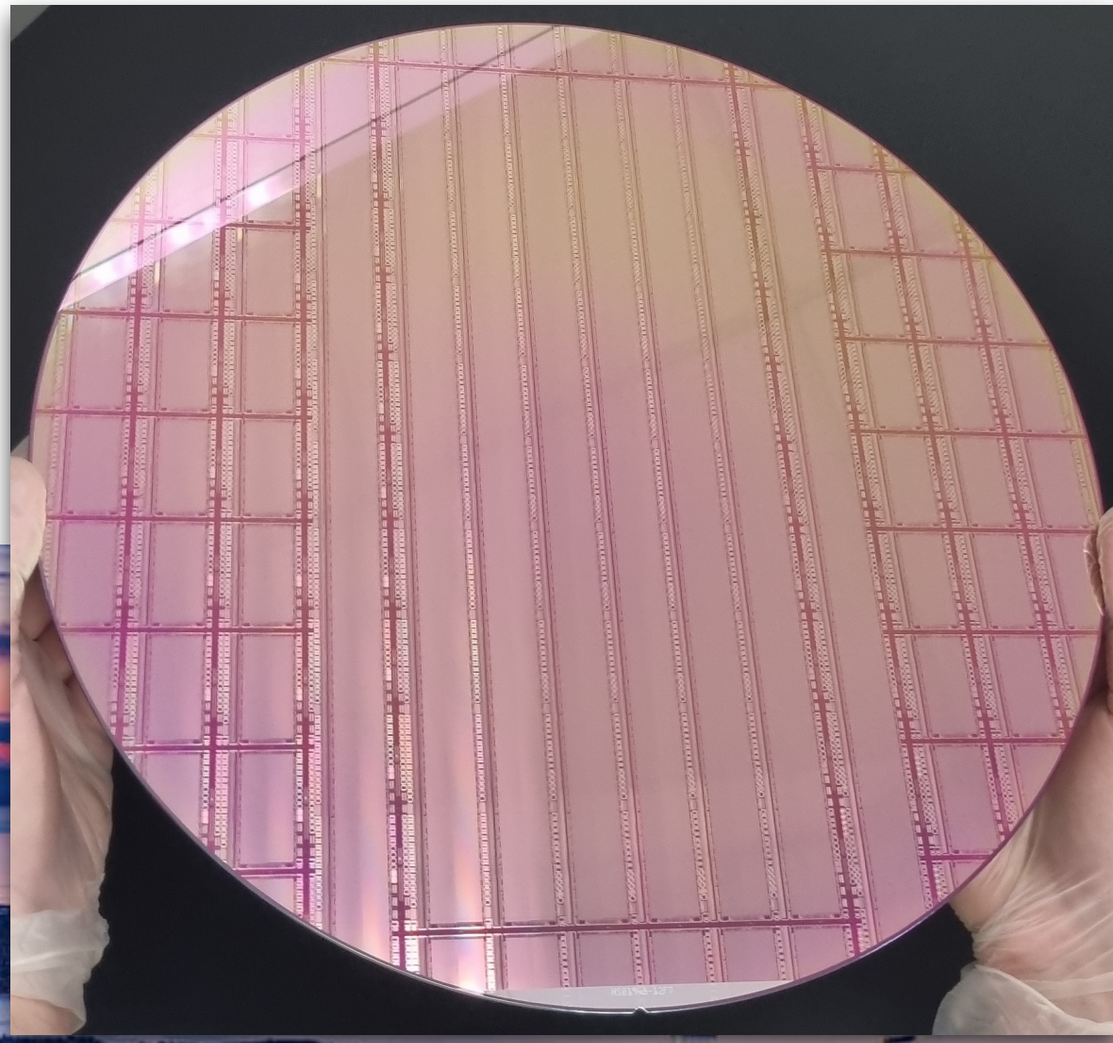
The future of bent MAPS, full-wafer (stitched) design: status and challenges

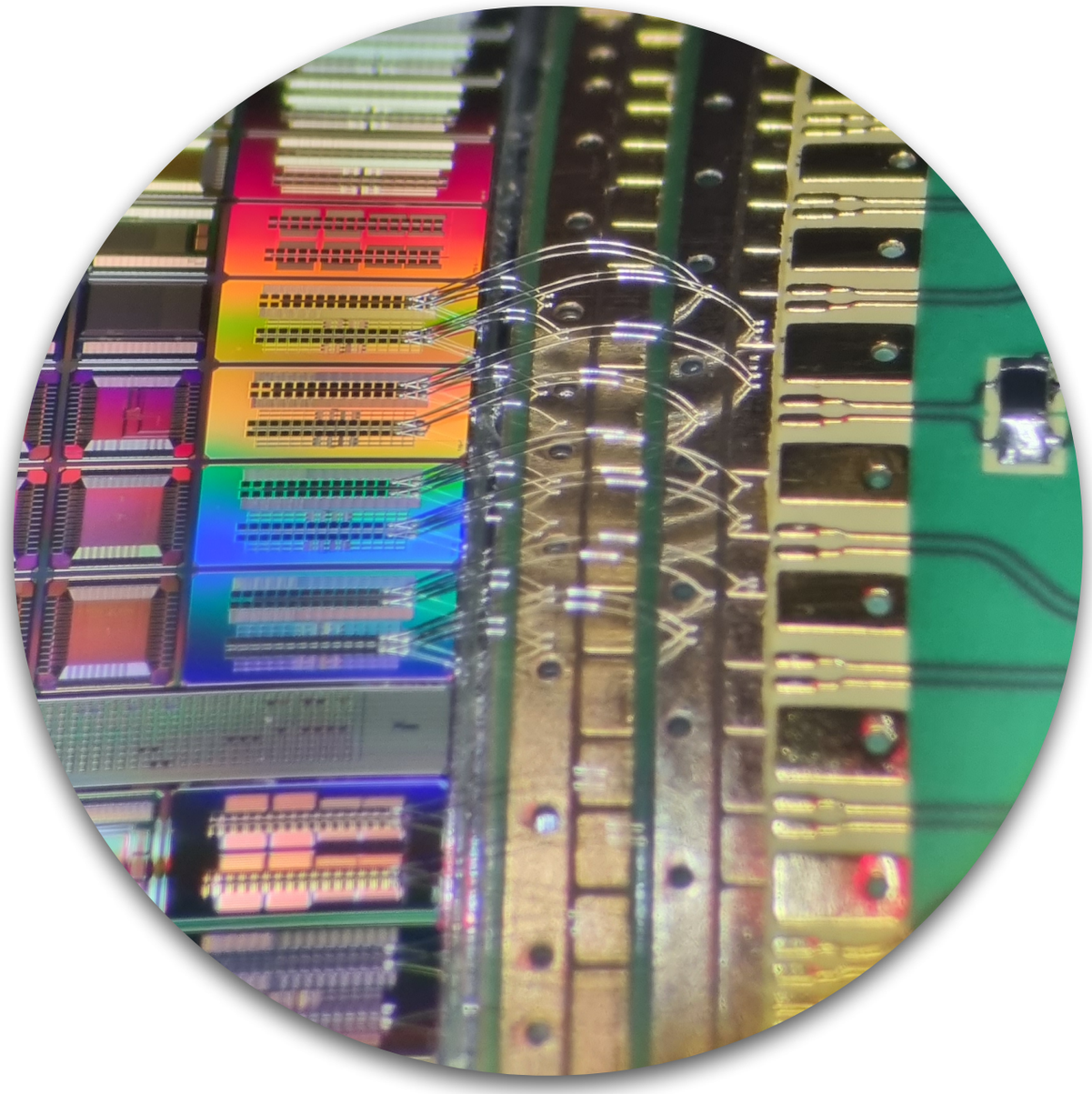
Magnus Mager (CERN)

on behalf of the ALICE collaboration

13th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD13), Vancouver, Canada



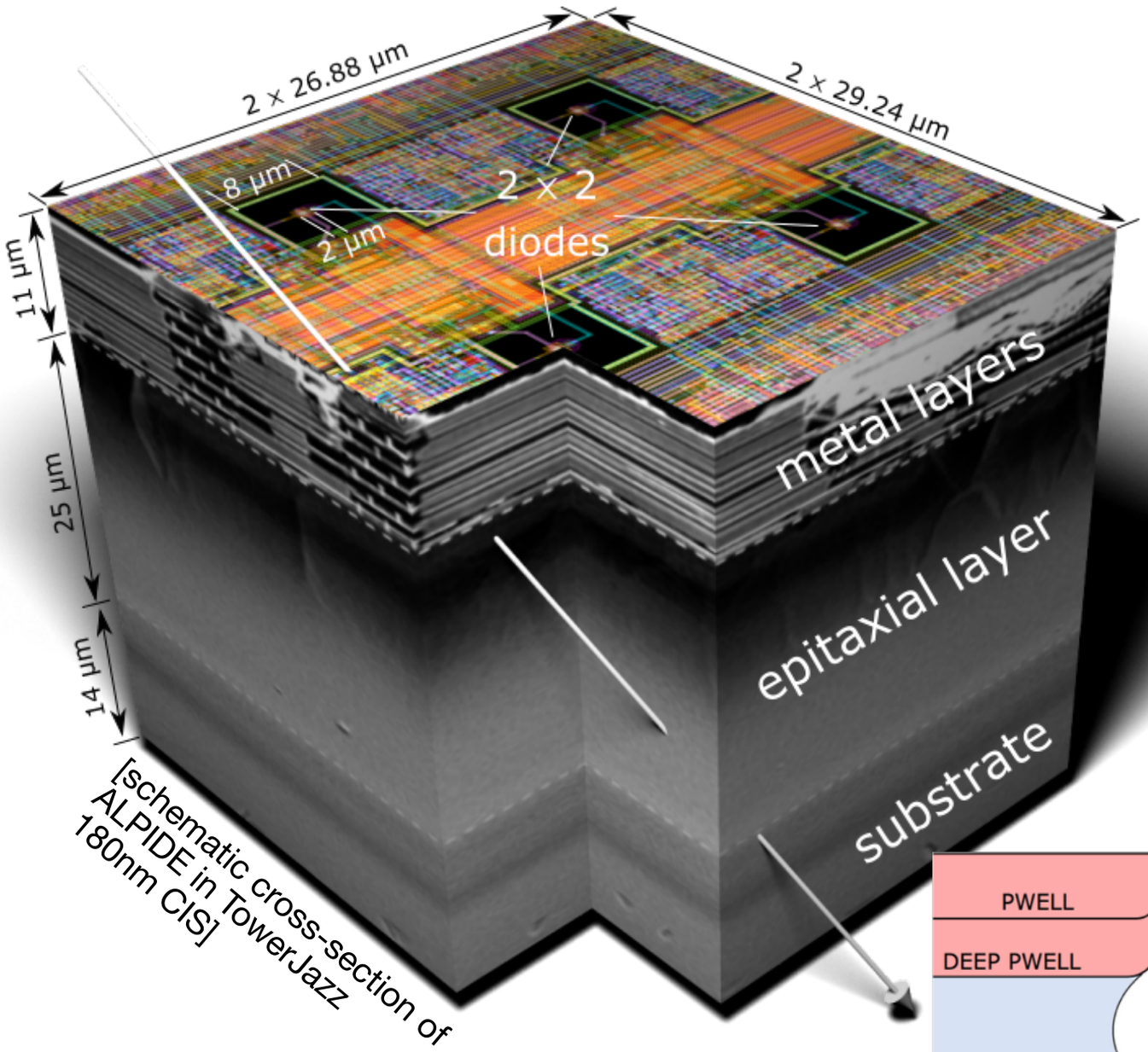
Overview



- **Introduction & Motivation**
  - Monolithic Active Pixel Sensors
  - stitching
  - bending
- **Challenges**
  - power (dissipation/distribution)
  - yield (mitigation strategies)
- **Two stitched prototypes**
  - design approaches
  - first characterisation results
- **Next steps**

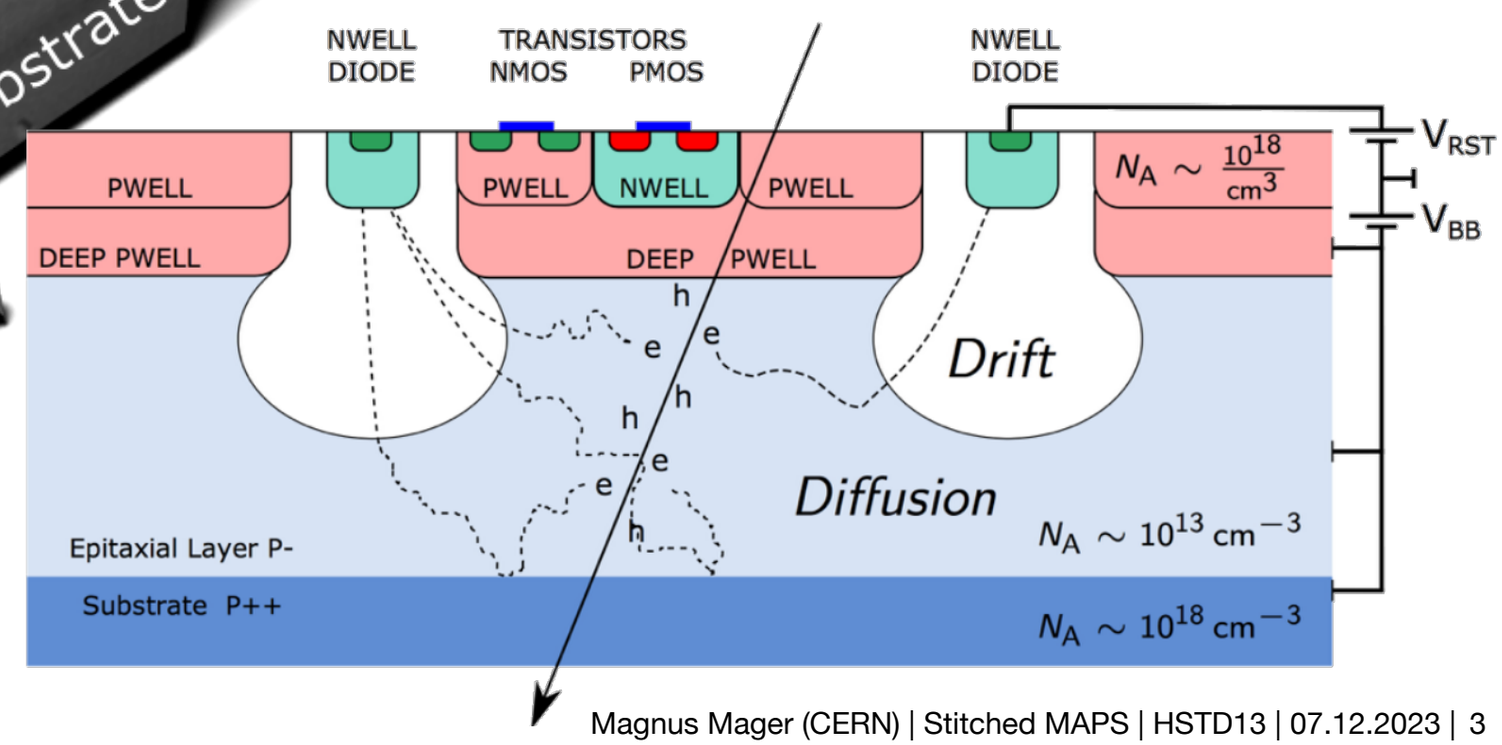
Monolithic Active Pixel Sensors (MAPS)

Reminder



[schematic cross-section of ALPIDE in TowerJazz 180nm CIS]

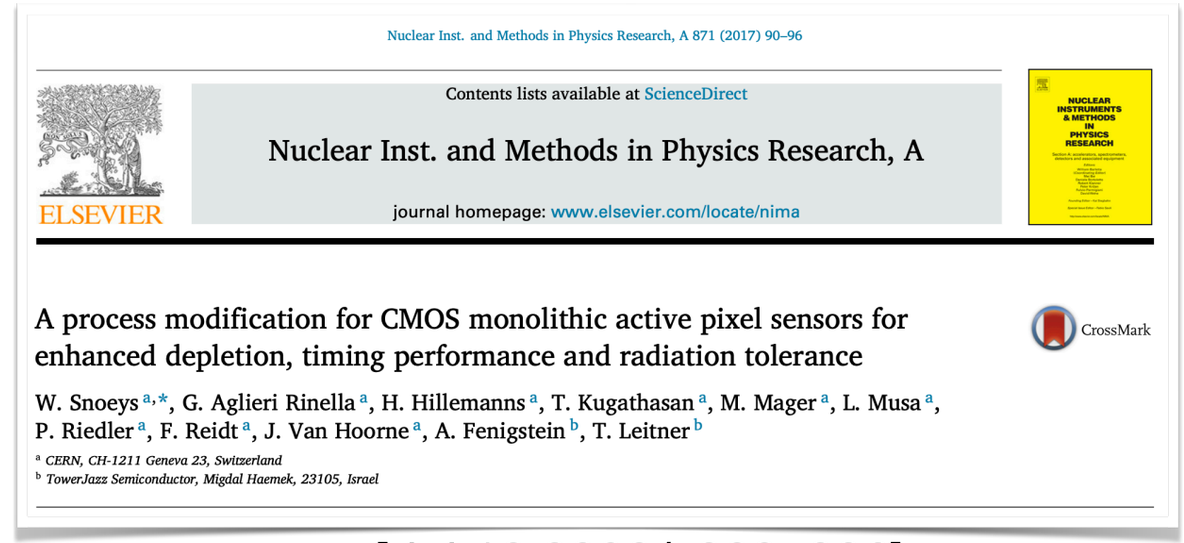
- **Quadruple well process:** deep p-well to allow CMOS circuitry inside matrix
- **Detection layer:** 10-30 µm high-resistive epitaxial
- **Small collection electrode:** large Q/C, low power consumption
- **Thickness:** ~50 µm (!)



Full depletion

faster and more radiation tolerant

- Addition of a **low-dose n-implant**
  - developed together with foundry
- Now crucial for the 65 nm development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A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance

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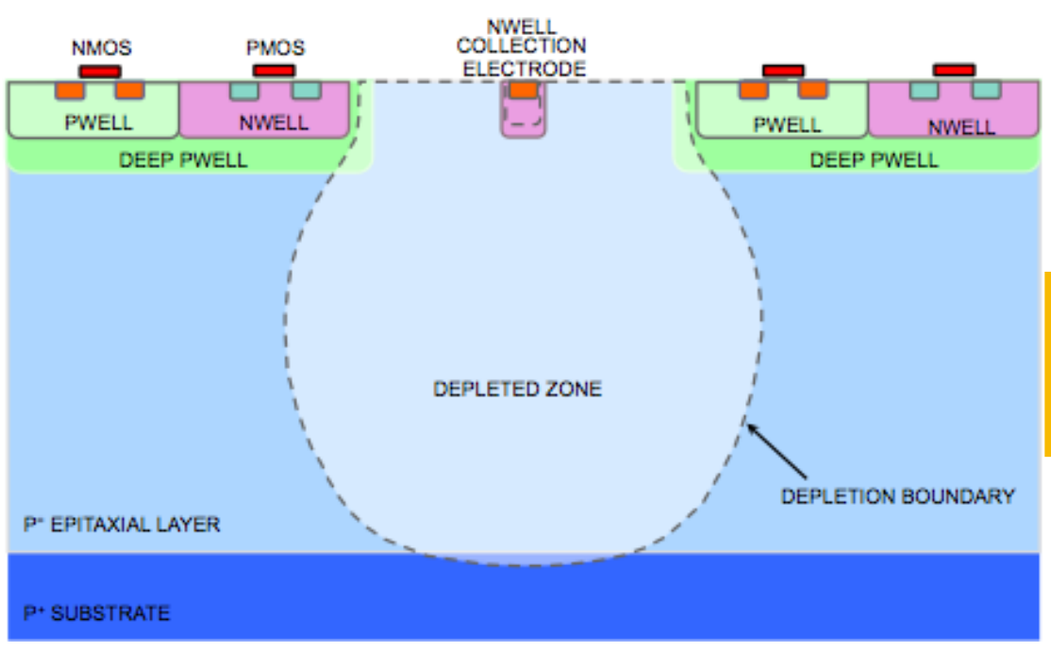
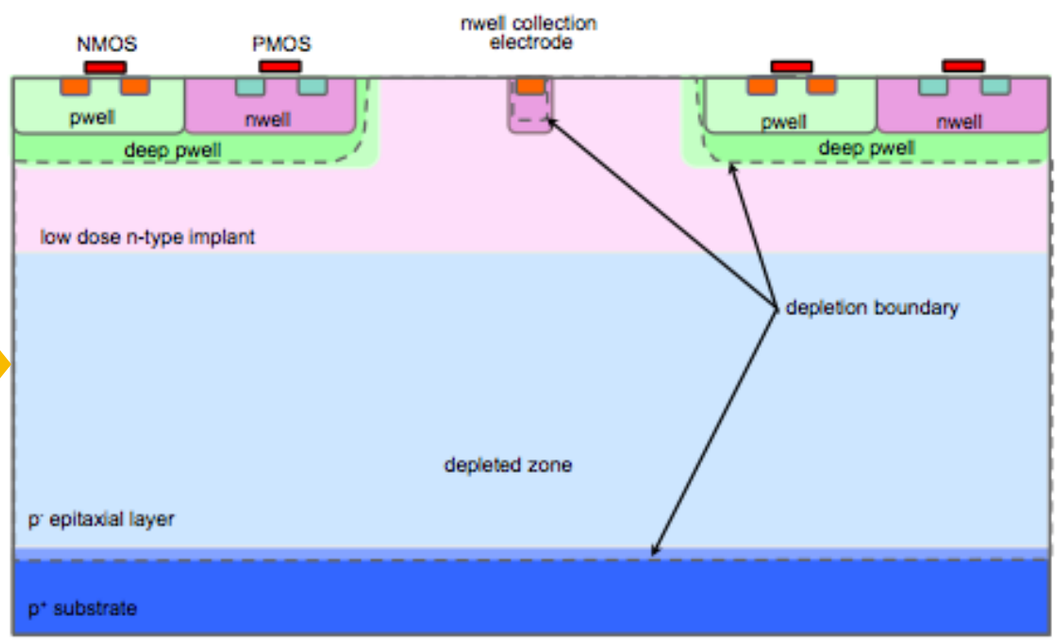


Developed and prototyped within ALPIDE R&D



Partially depleted epitaxial layer
Charge collection time < 30 ns
Operational up to 10^{14} 1 MeV n_{eq}/cm^2

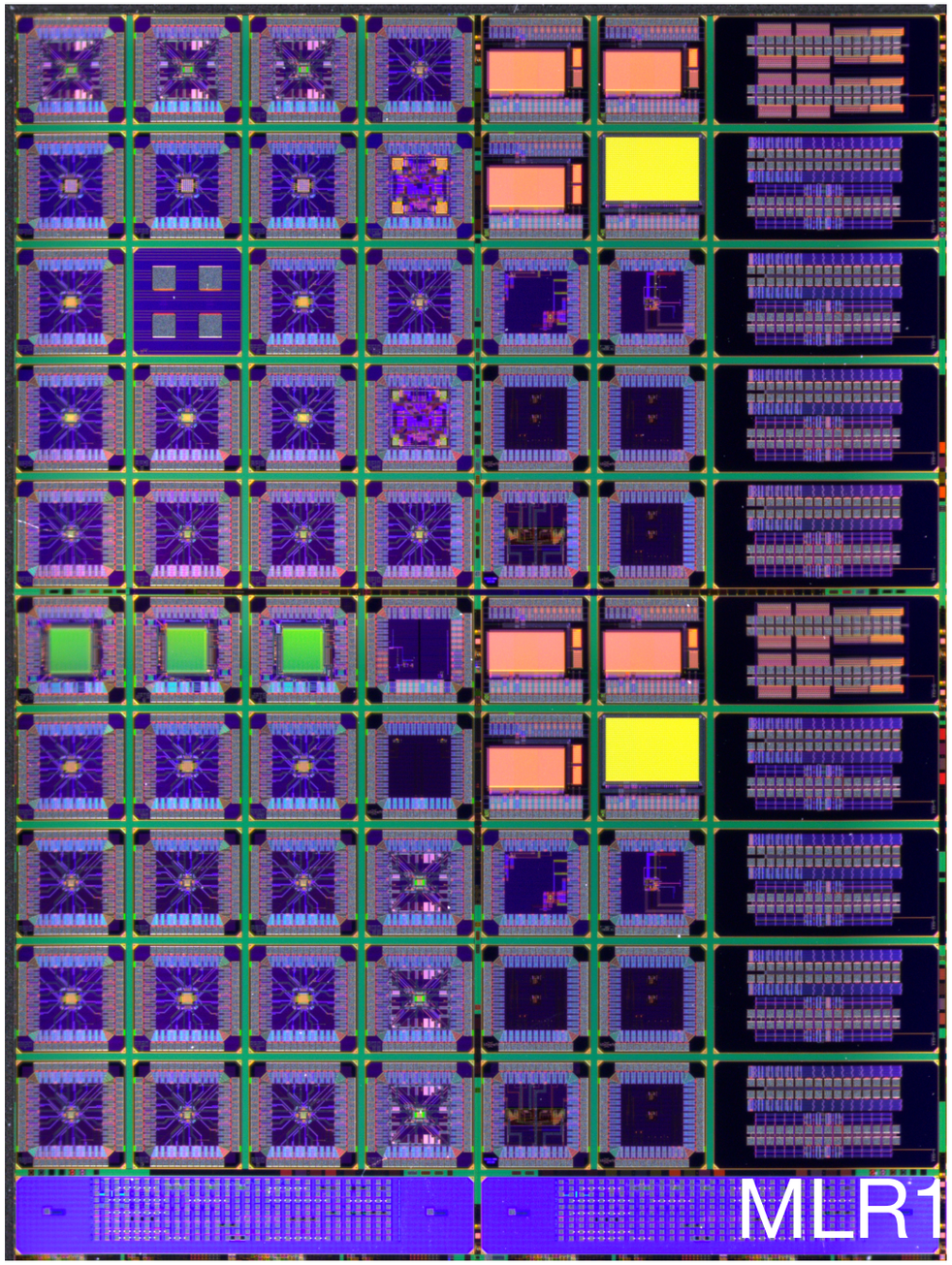
Fully depleted epitaxial layer
Charge collection time < 1 ns
after further improvements (outside ALICE):
operational up to 10^{15} 1 MeV n_{eq}/cm^2

→ recent R&D (MALTA, CLICpix, Monopix, 65nm)

Qualification of 65 nm CMOS

TPSCo 65 nm CMOS Imaging Technology

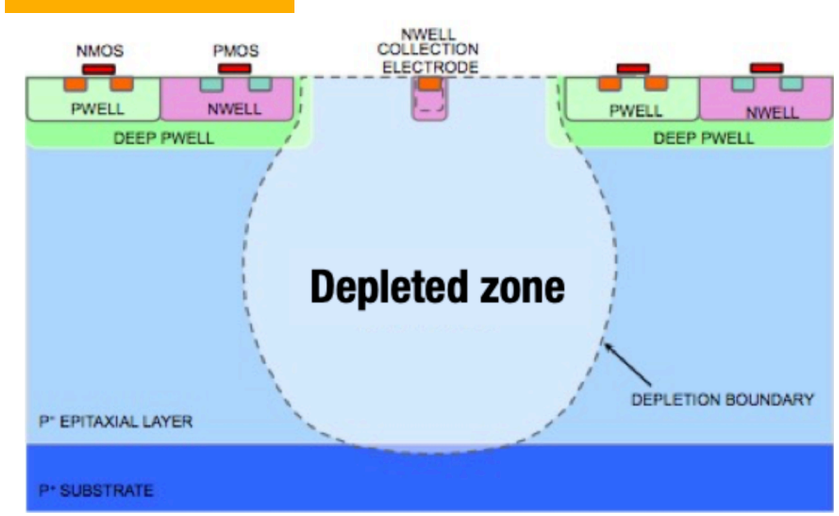
- Concentrated effort **ALICE ITS3** together with **CERN EP R&D**
- **Key benefits**
  - smaller features/transistors: higher integration density
  - smaller pitches
  - lower power consumption
  - **larger wafers** (200→300 mm)
- **Verification:**
  - comprehensive *first* submission: **55** prototype chips
  - goal: qualify the technology for radiation hardness and particle detection (achieved)



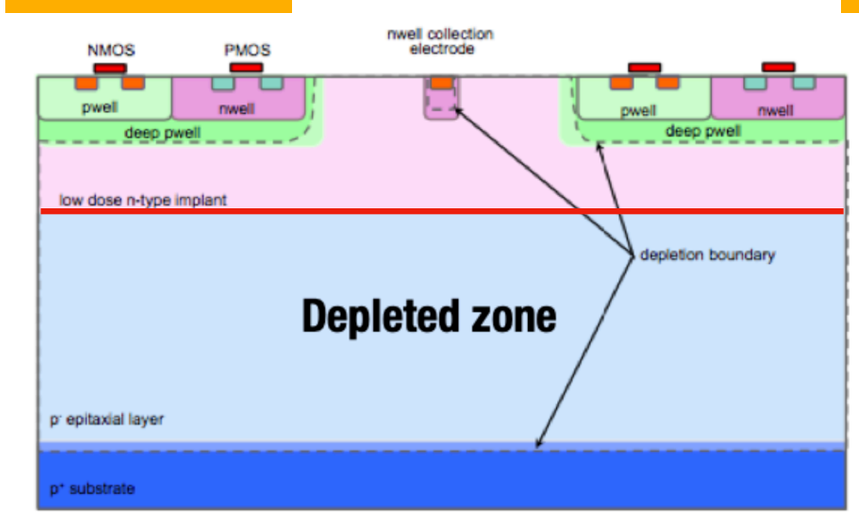
Qualification of 65 nm CMOS
process variants

- Following the experience with 180 nm, the 65 nm CIS process could be modified
- Three different designs “standard”, “modified”, “modified with gap” are tried
  - modified with gap is the default for the next developments
- Largely increases the charge collection speed and radiation hardness
- Lowers the charge spread / cluster size → more signal per pixel

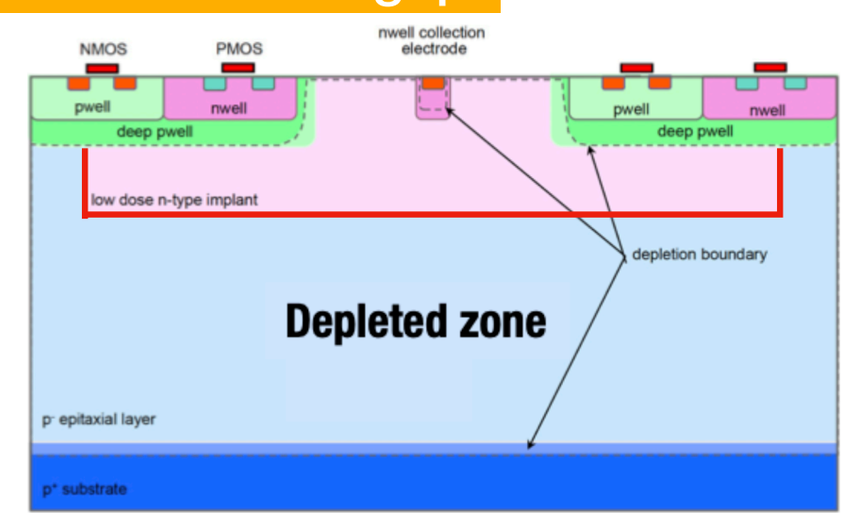
“standard”



“modified”

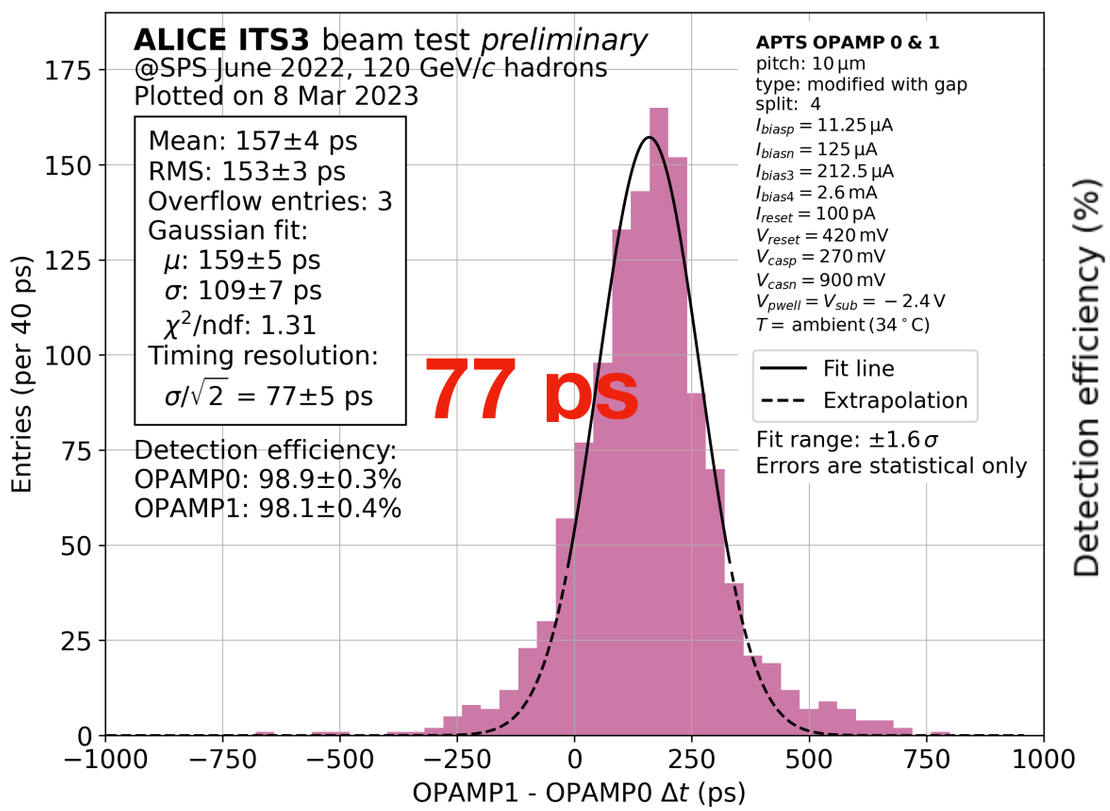


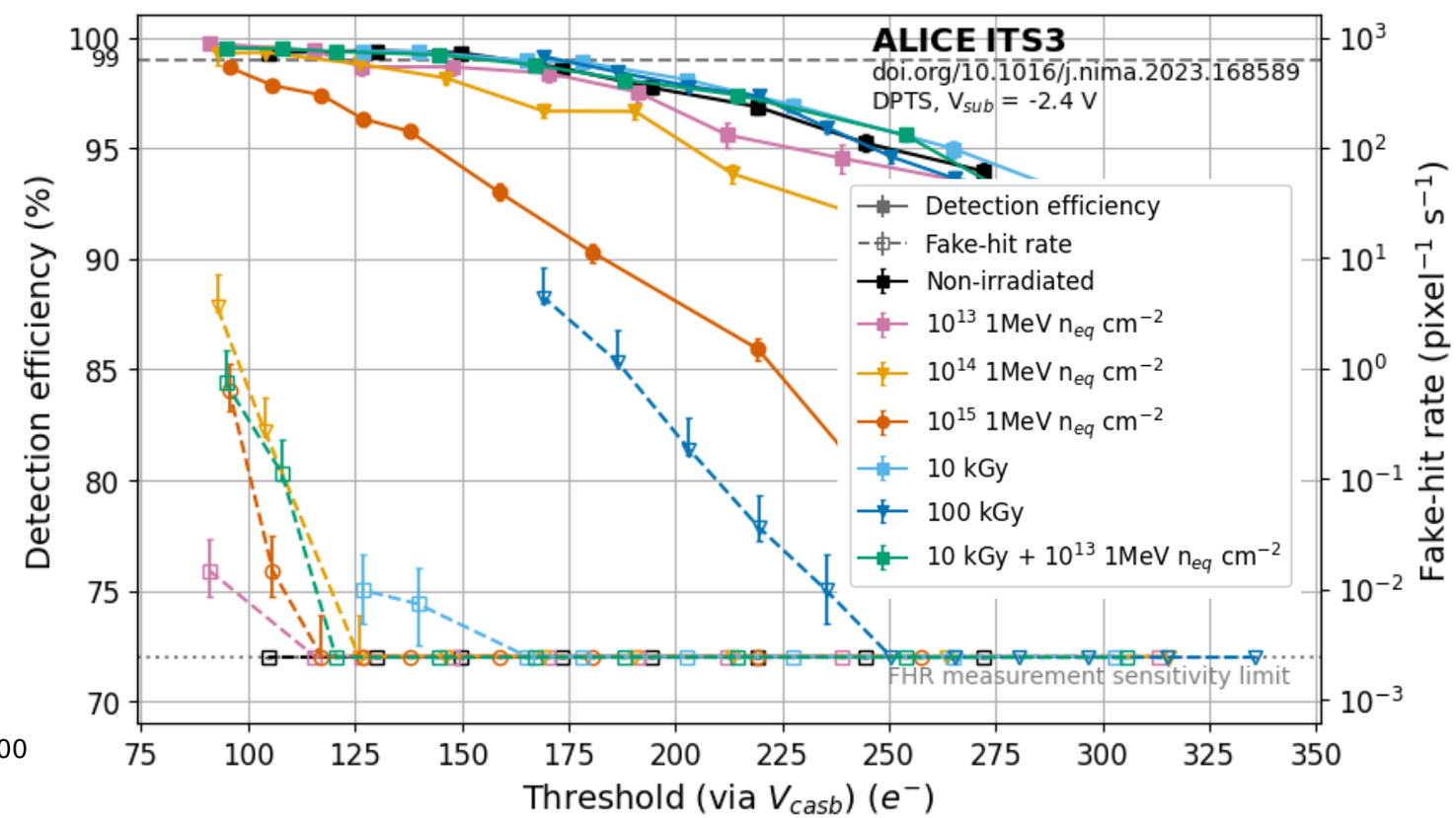
“modified with gap”



Qualification of 65 nm CMOS
selected results

- Intrinsic time resolutions of 77 ps for 10 μm pixels
- >99% detection efficiency even after 10^{15} NIEL for 15 μm pixels at room temperature



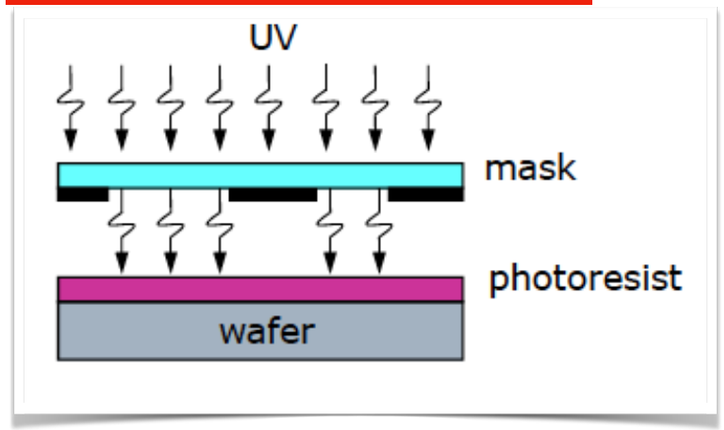


Excellent performances of the 65 nm technology have been established experimentally

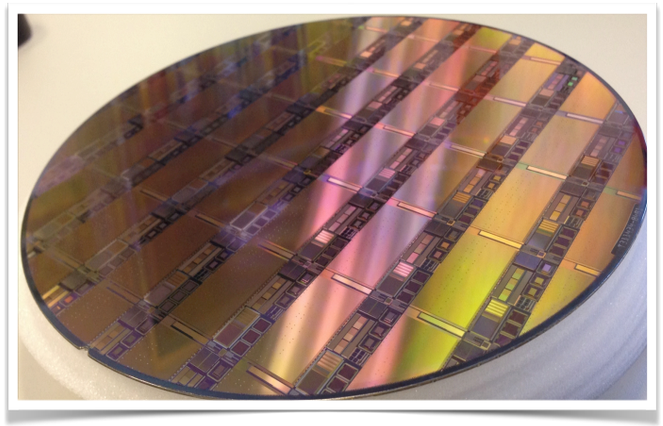
Wafer-scale sensors: stitching
introduction

- Chip size is traditionally limited by CMOS manufacturing ("reticle size")
  - typical sizes of few cm²
  - modules are tiled with chips connected to a flexible printed circuit board

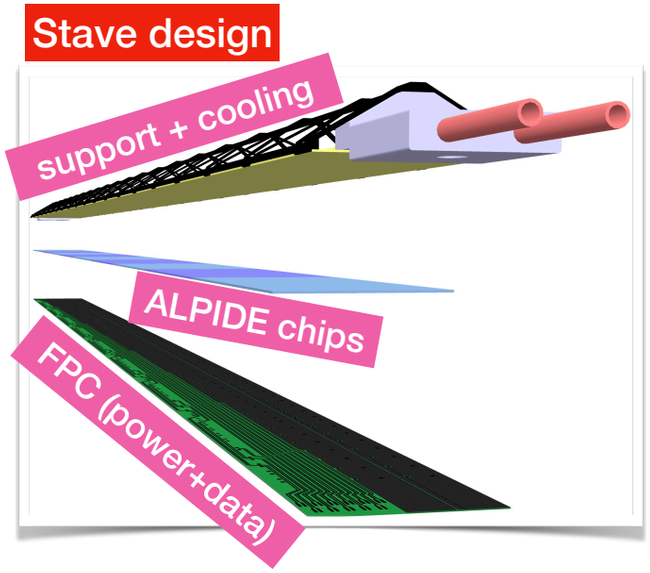
Principle of photolithography



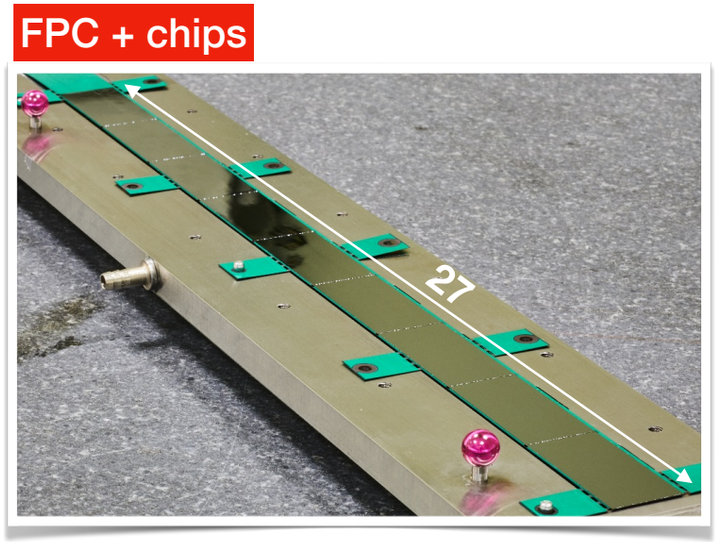
200 mm ALPIDE prototype wafer



Stave design



FPC + chips



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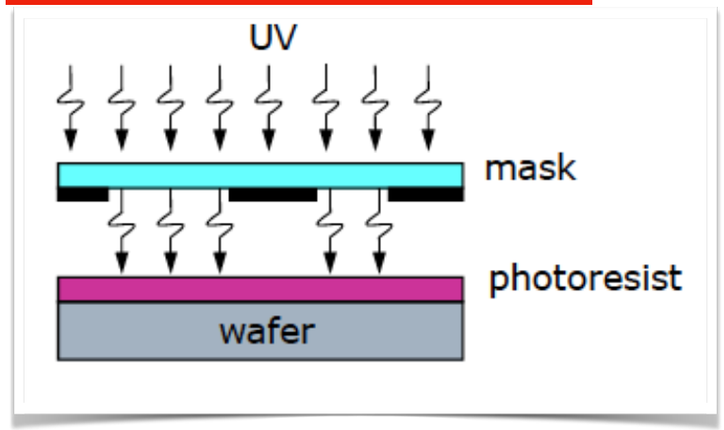
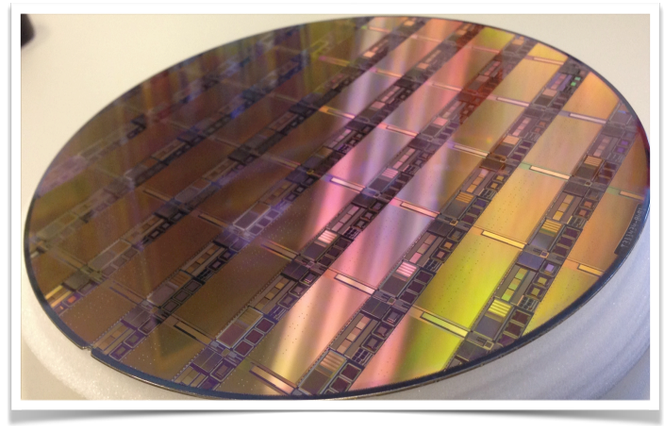
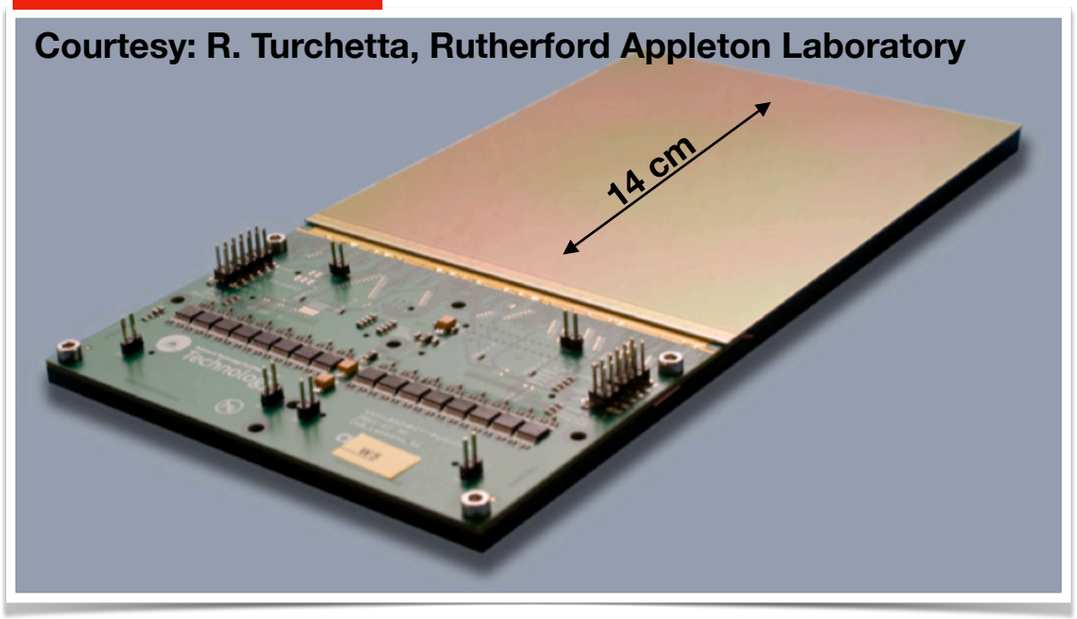


200 mm ALPIDE prototype wafer

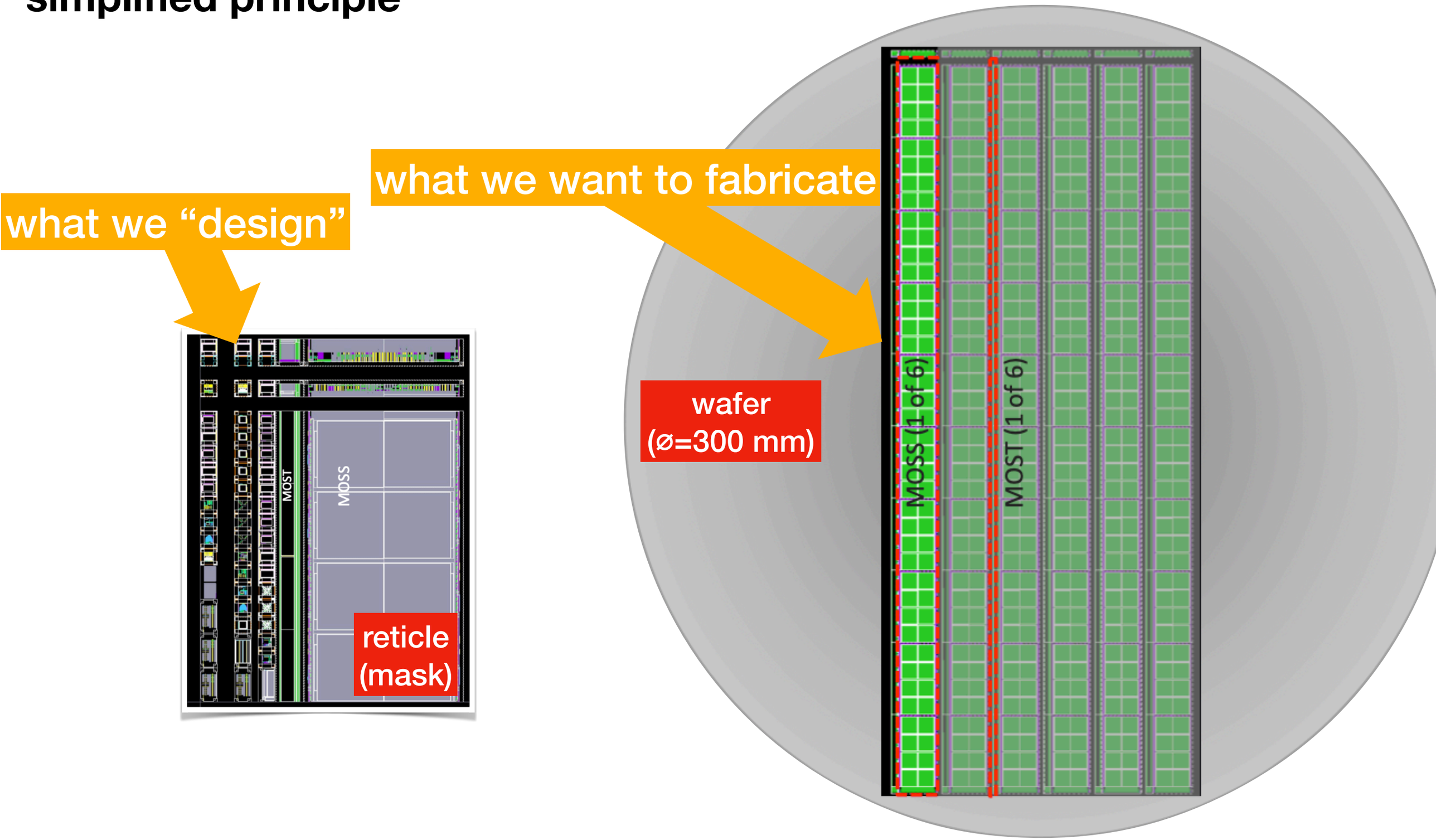


- New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  - actively used in industry
  - a 300 mm wafer can house a chip to equip a full half-layer
  - *requires dedicated chip design*

Wafer-scale sensor

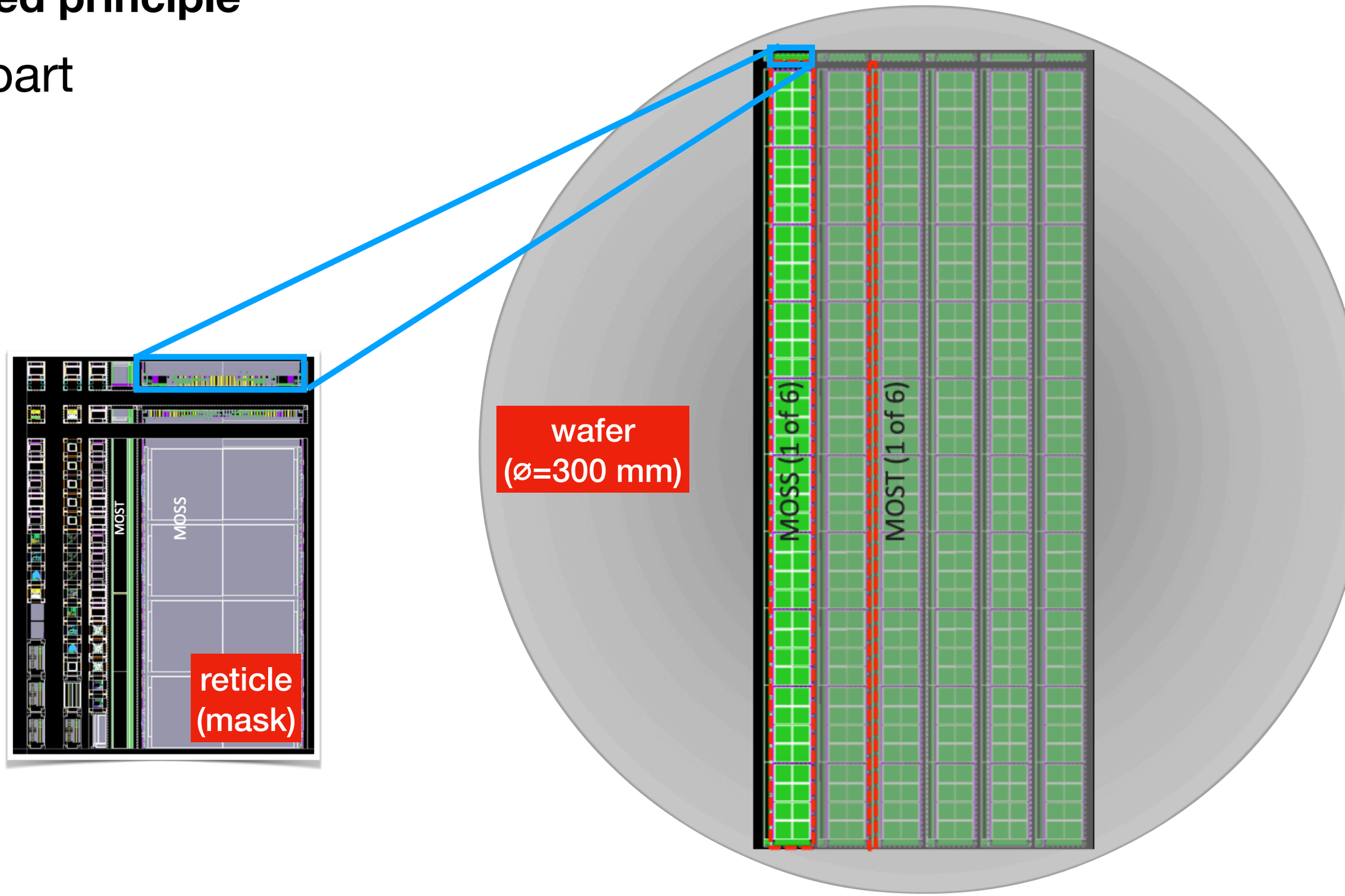


Stitching
simplified principle



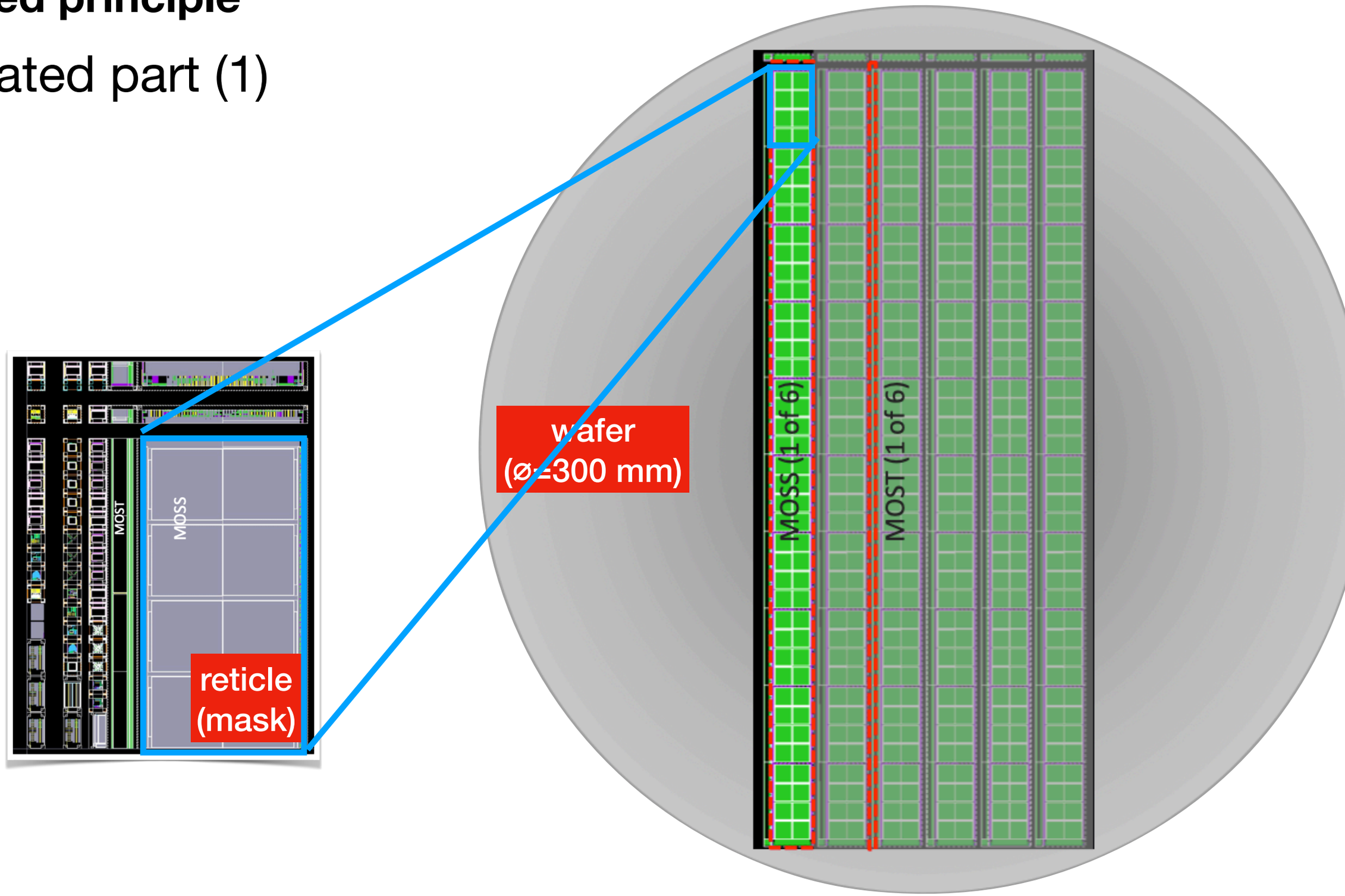
Stitching
simplified principle

- top part



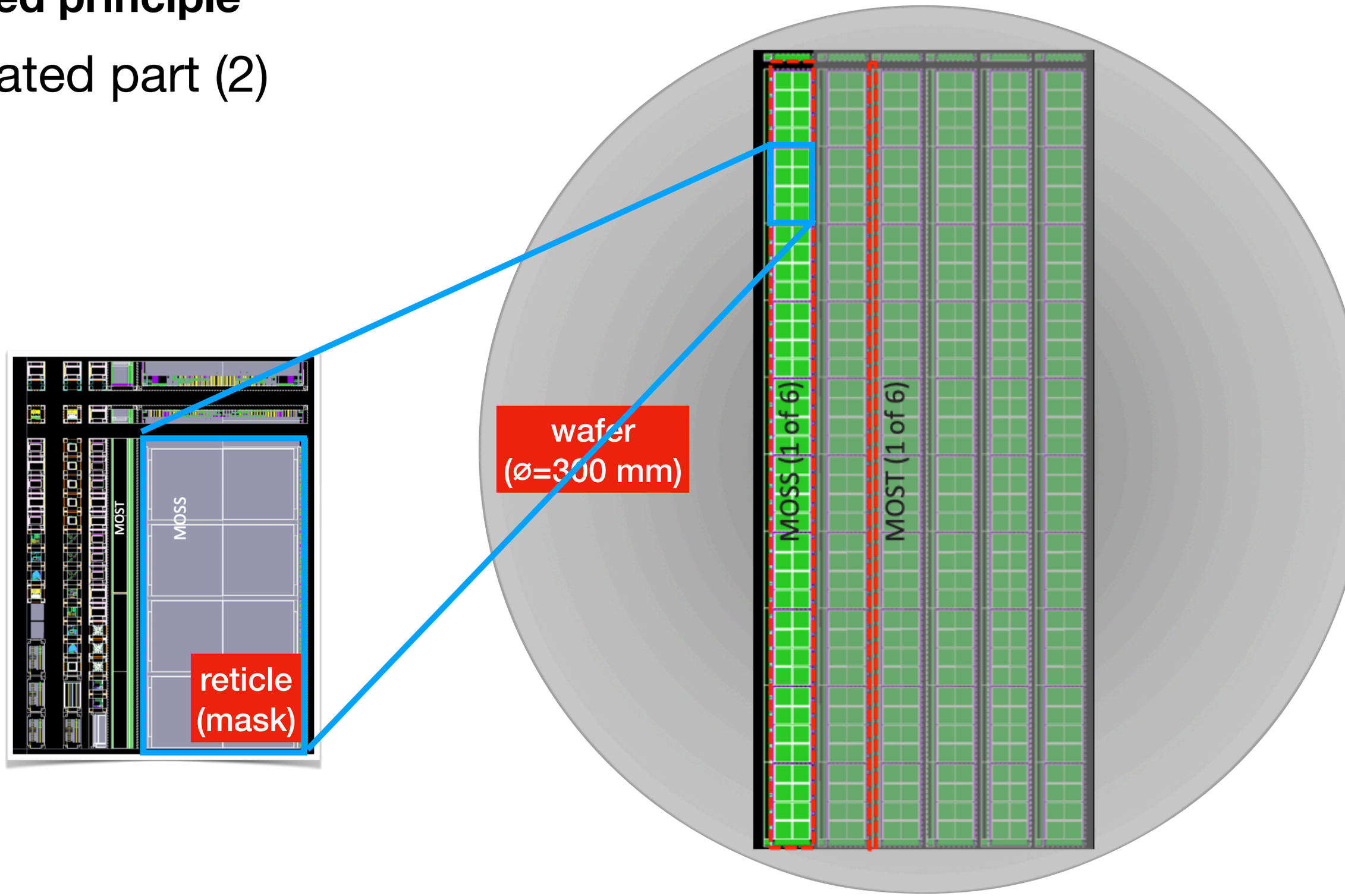
Stitching
simplified principle

- repeated part (1)



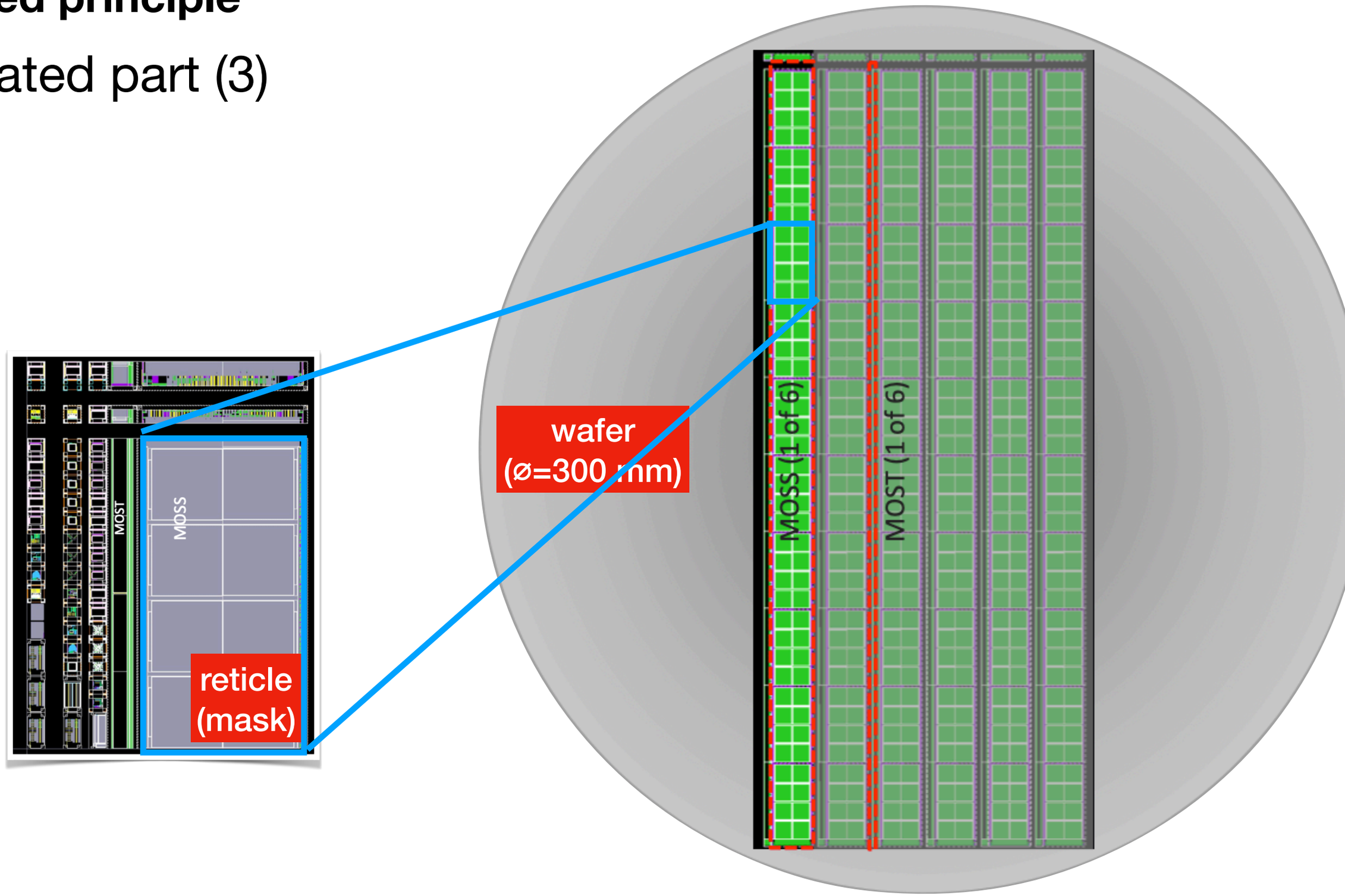
Stitching
simplified principle

- repeated part (2)



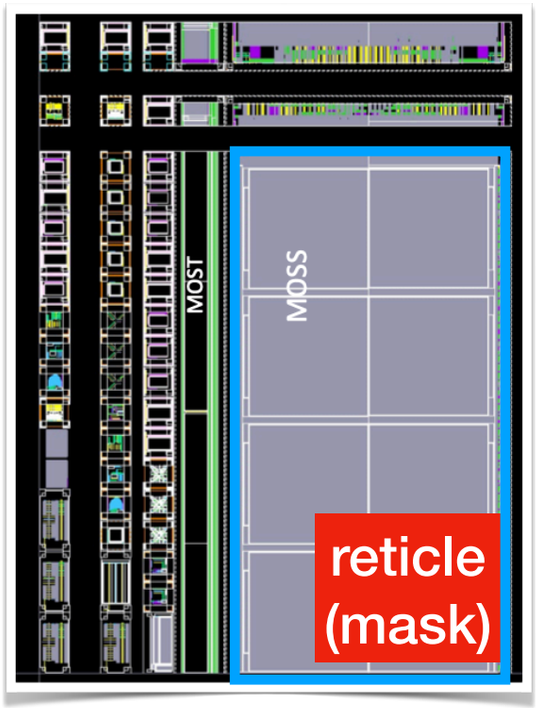
Stitching
simplified principle

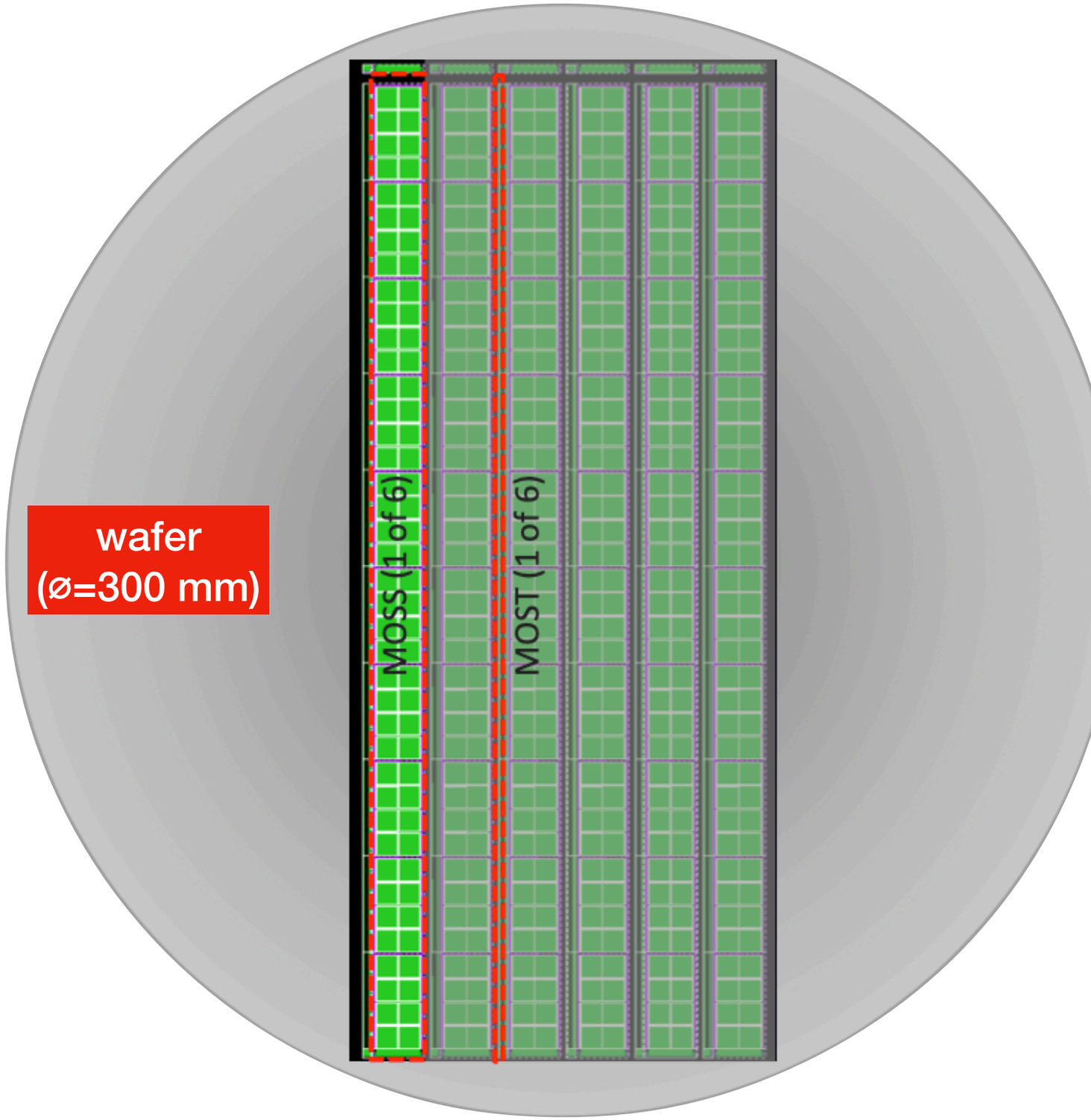
- repeated part (3)



Stitching
simplified principle

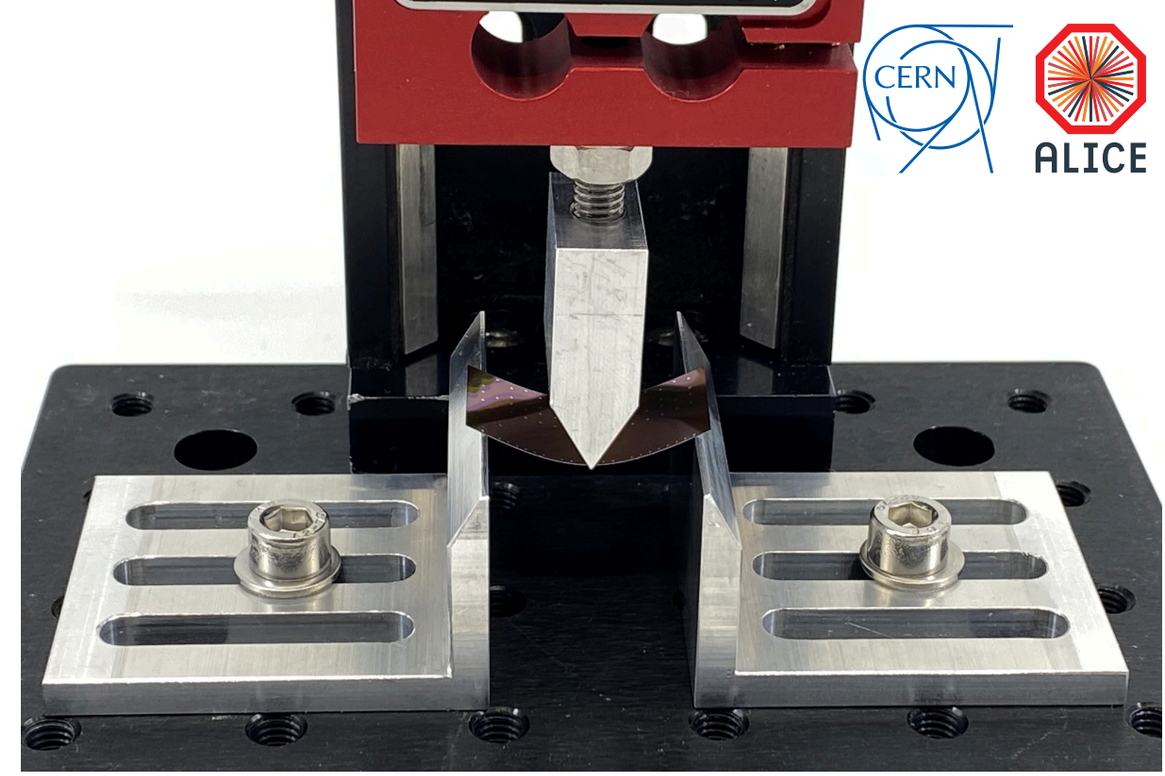
- final circuit is a concatenation of different parts of the masks

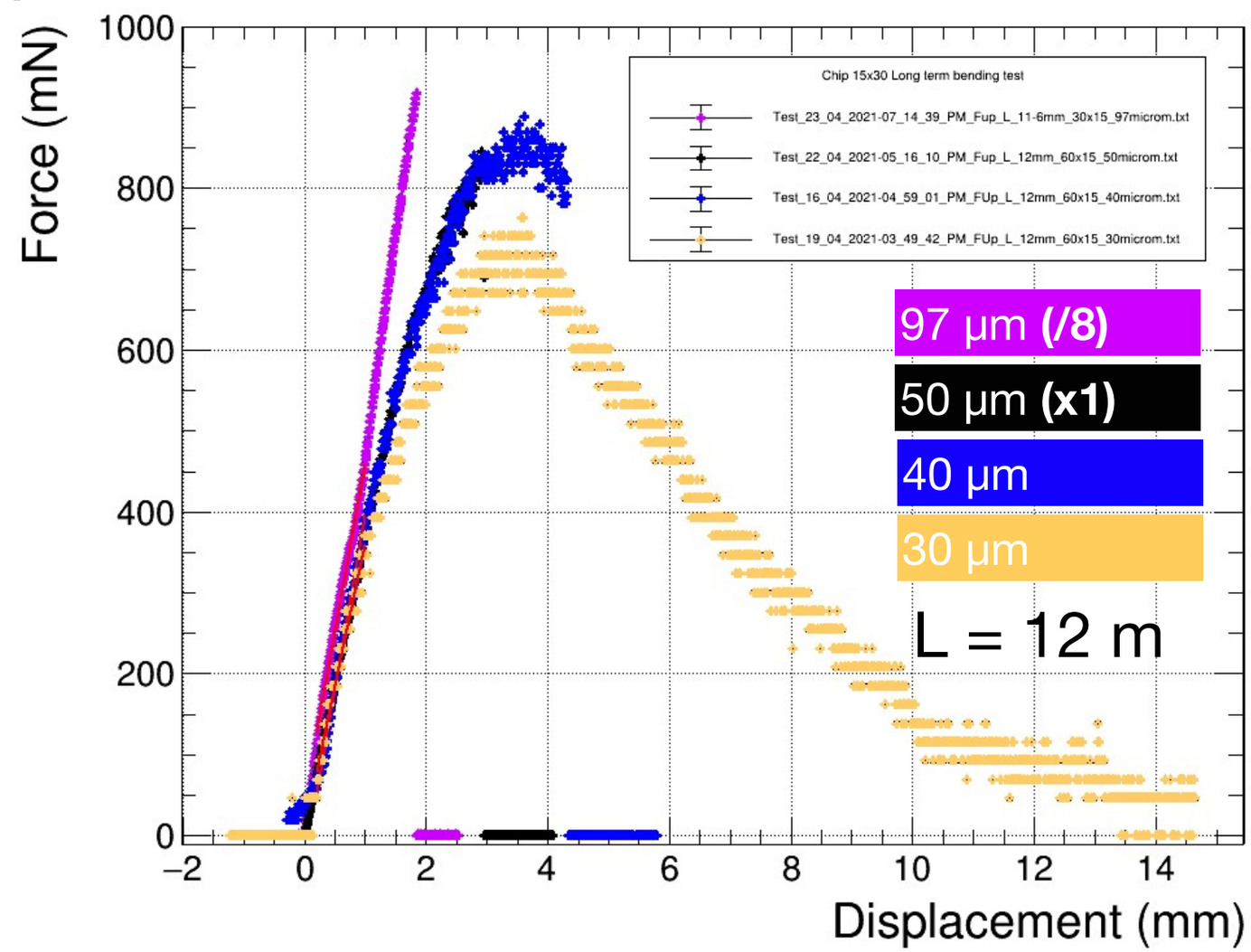




Flexibility of silicon
systematically

- **Monolithic** Active Pixel Sensors are quite flexible
- Bending force scales as (thickness)$^{-3}$
  - large benefit from thinner sensors





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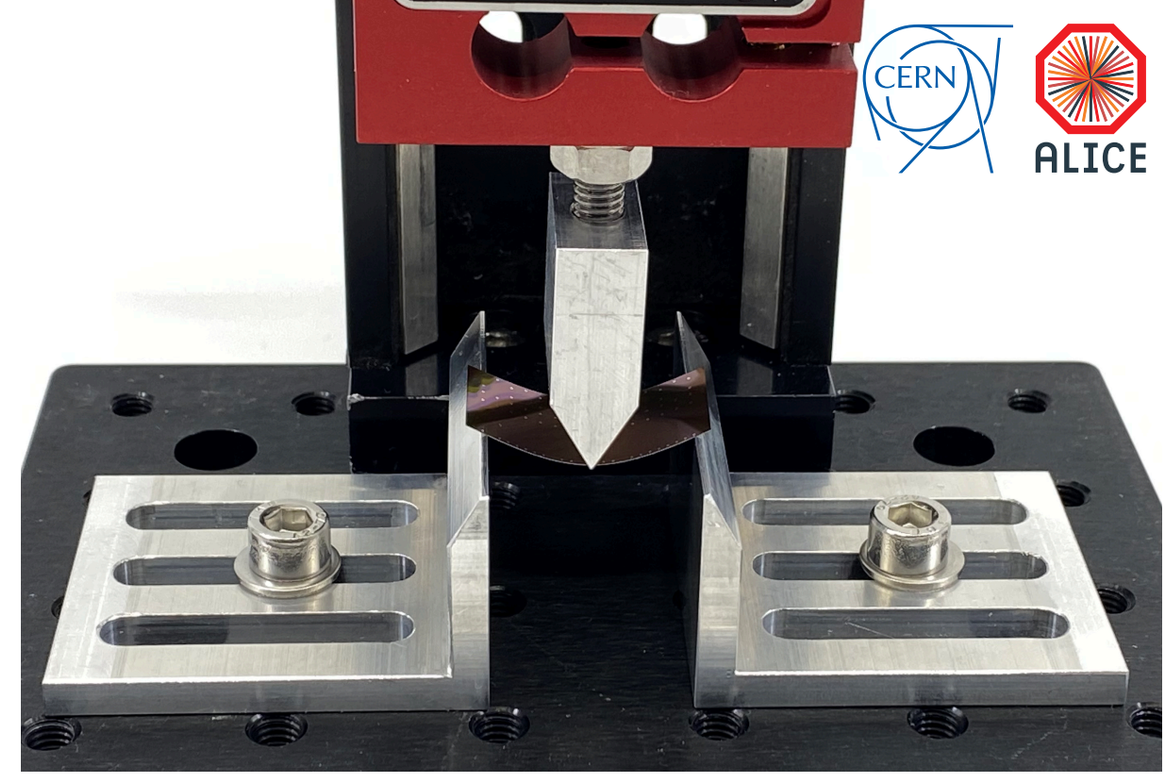

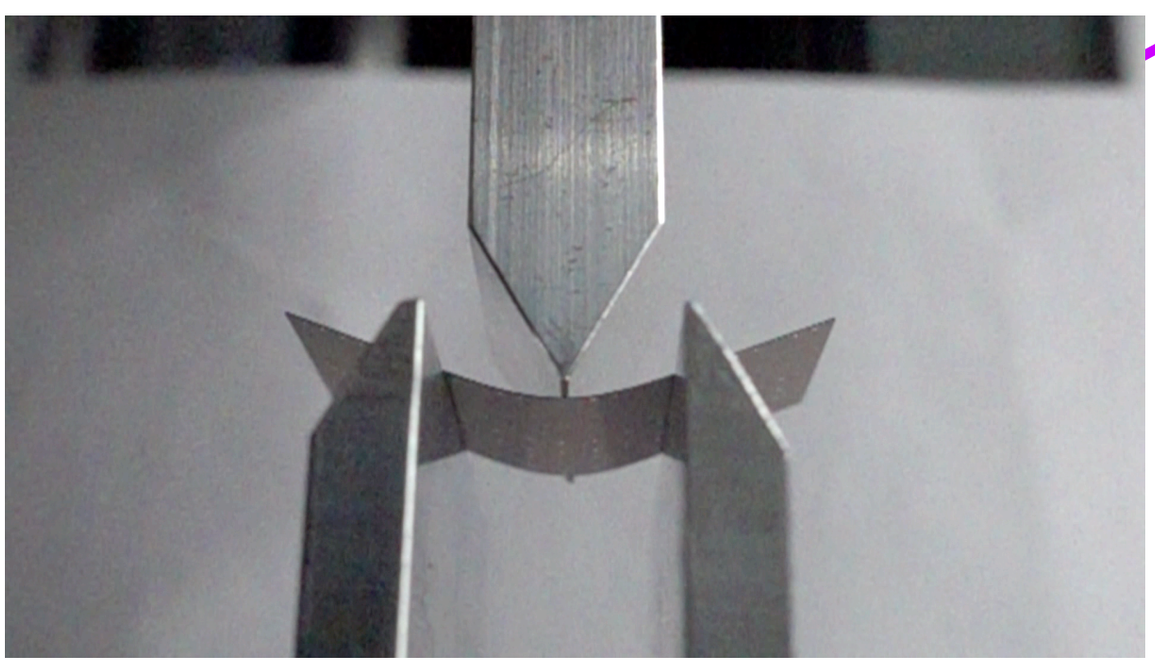

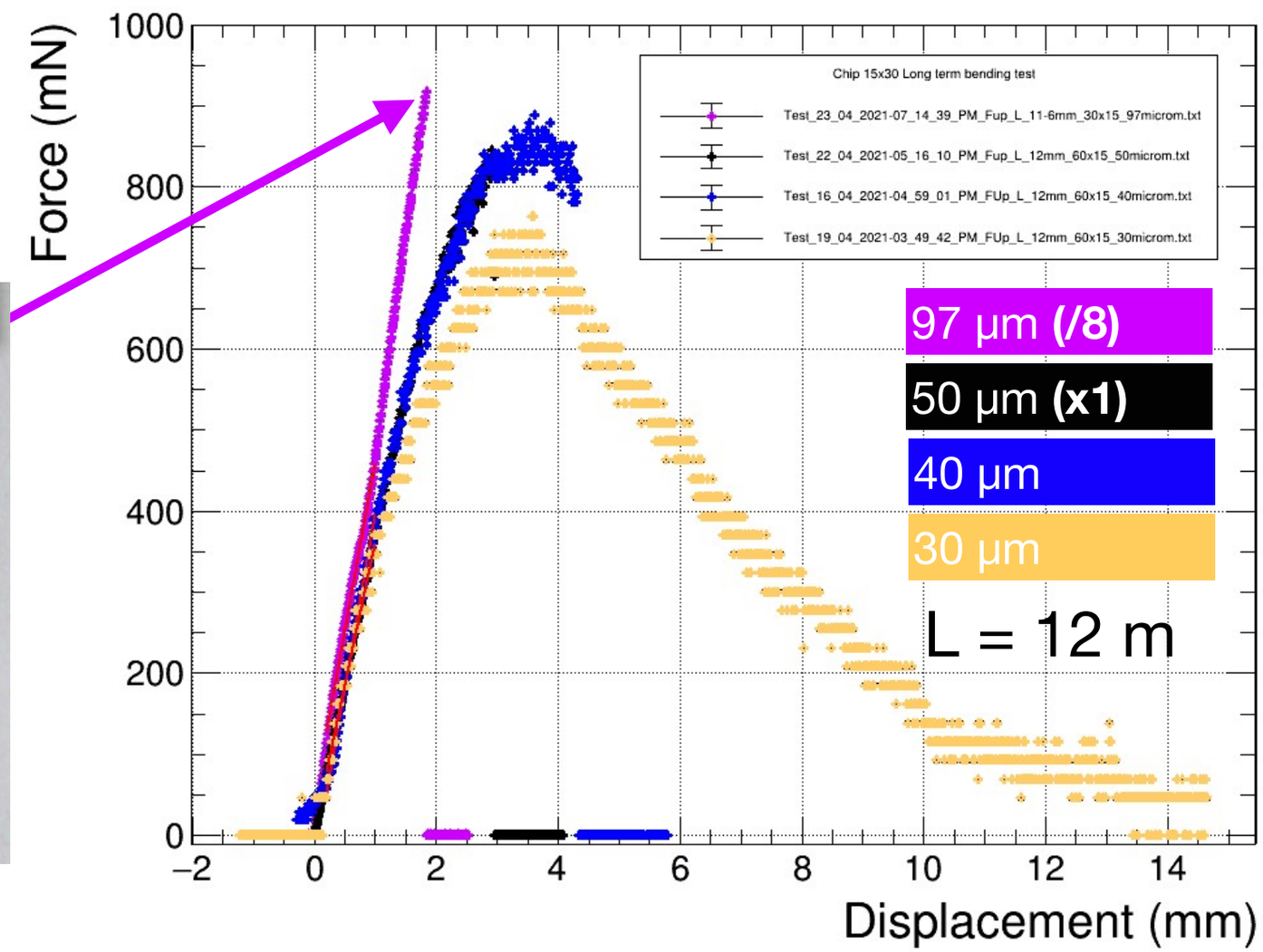

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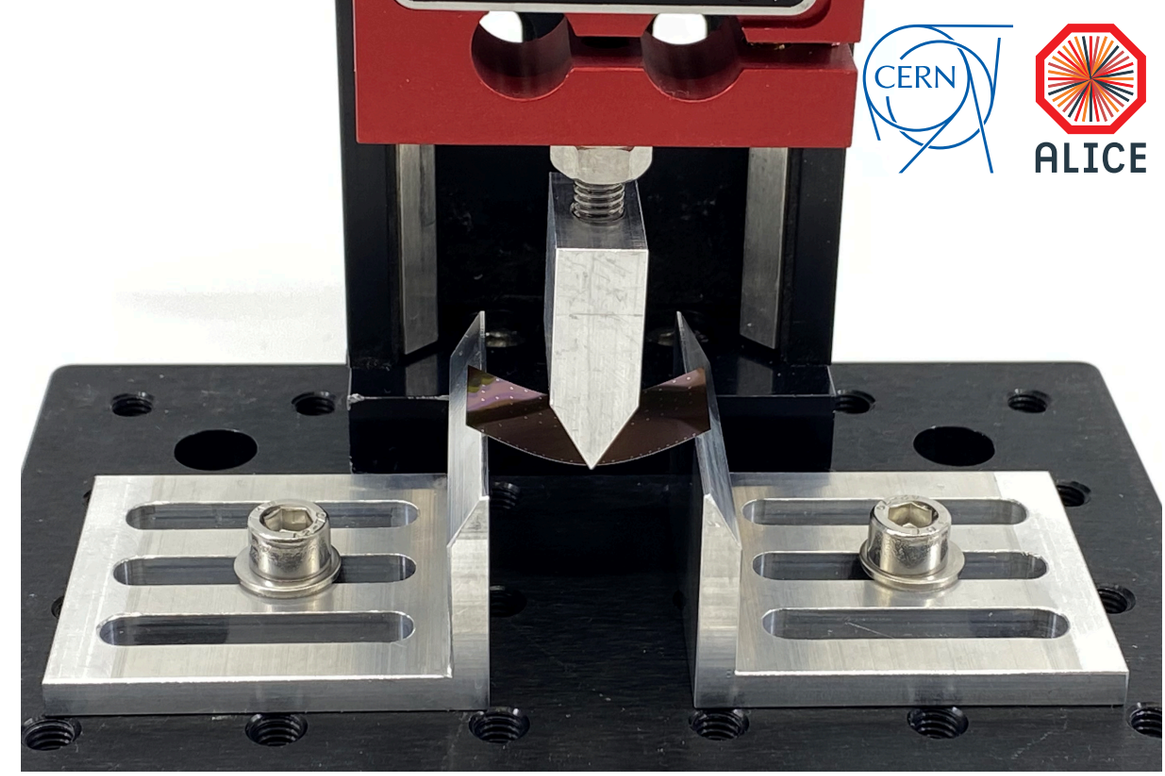

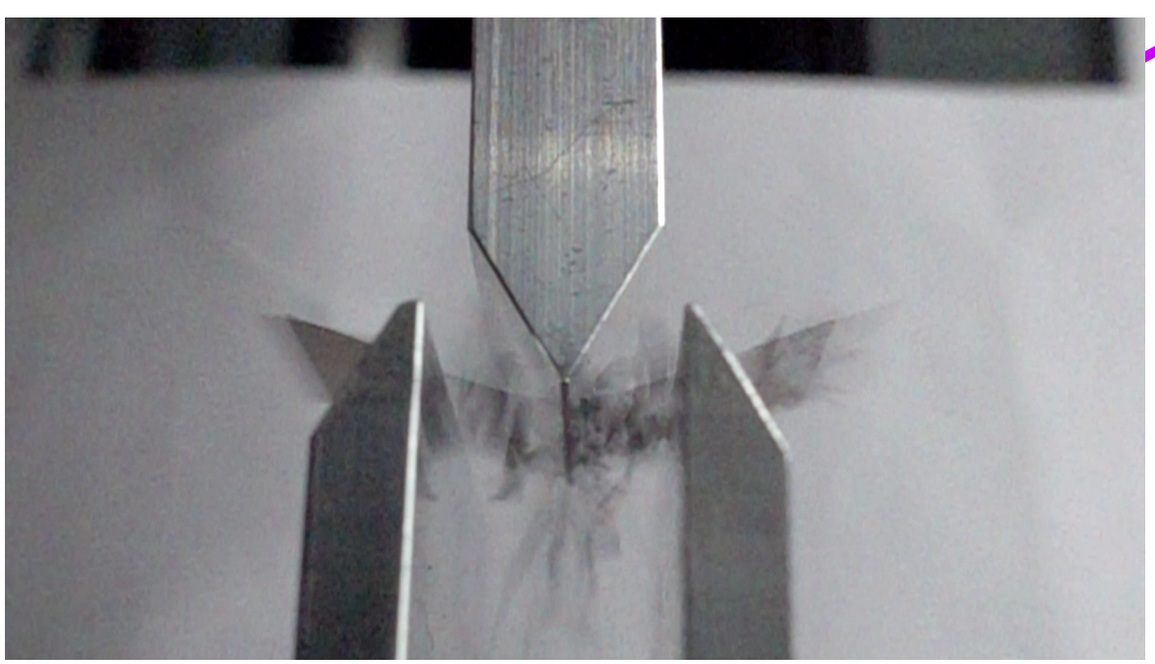

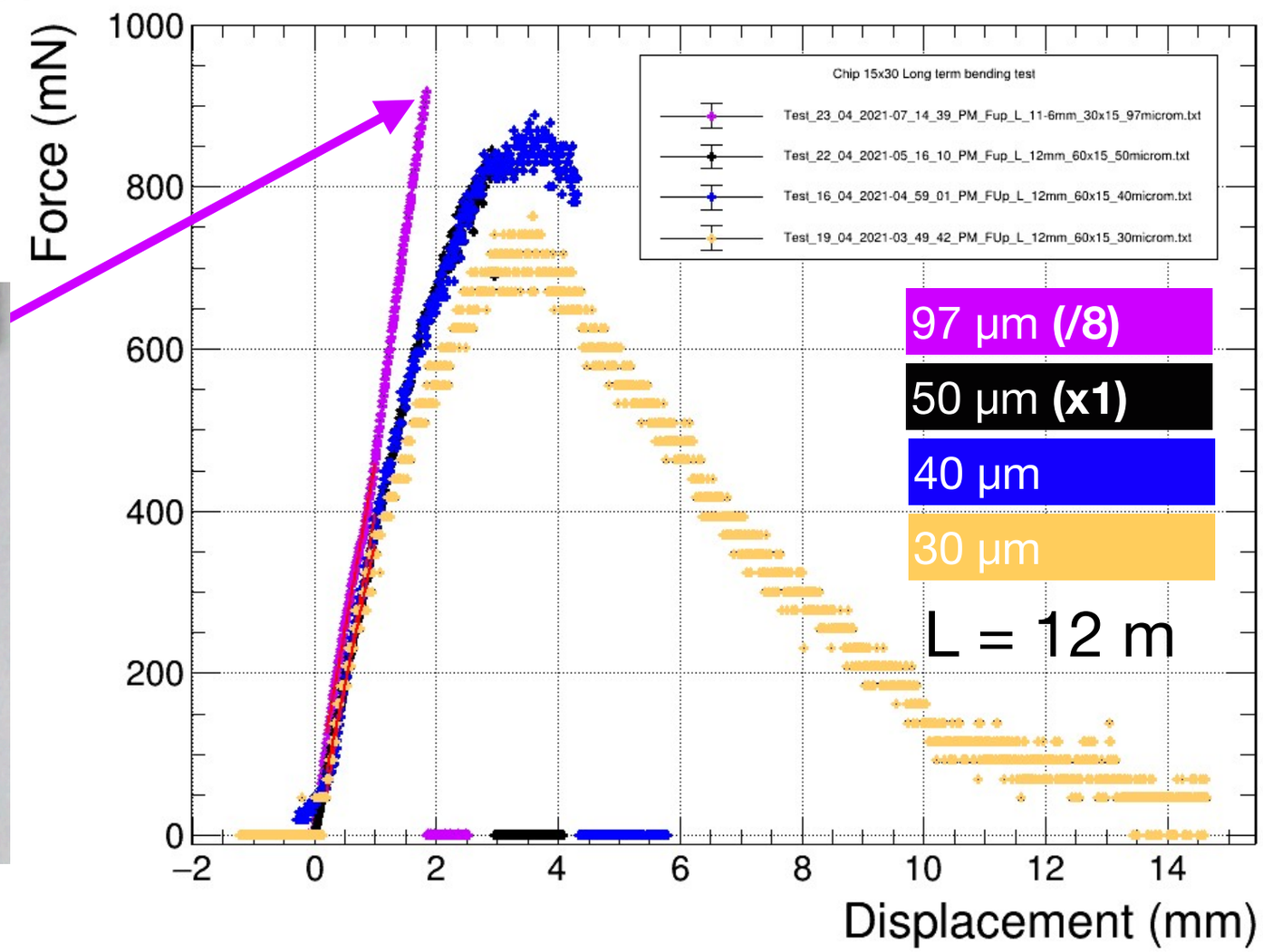

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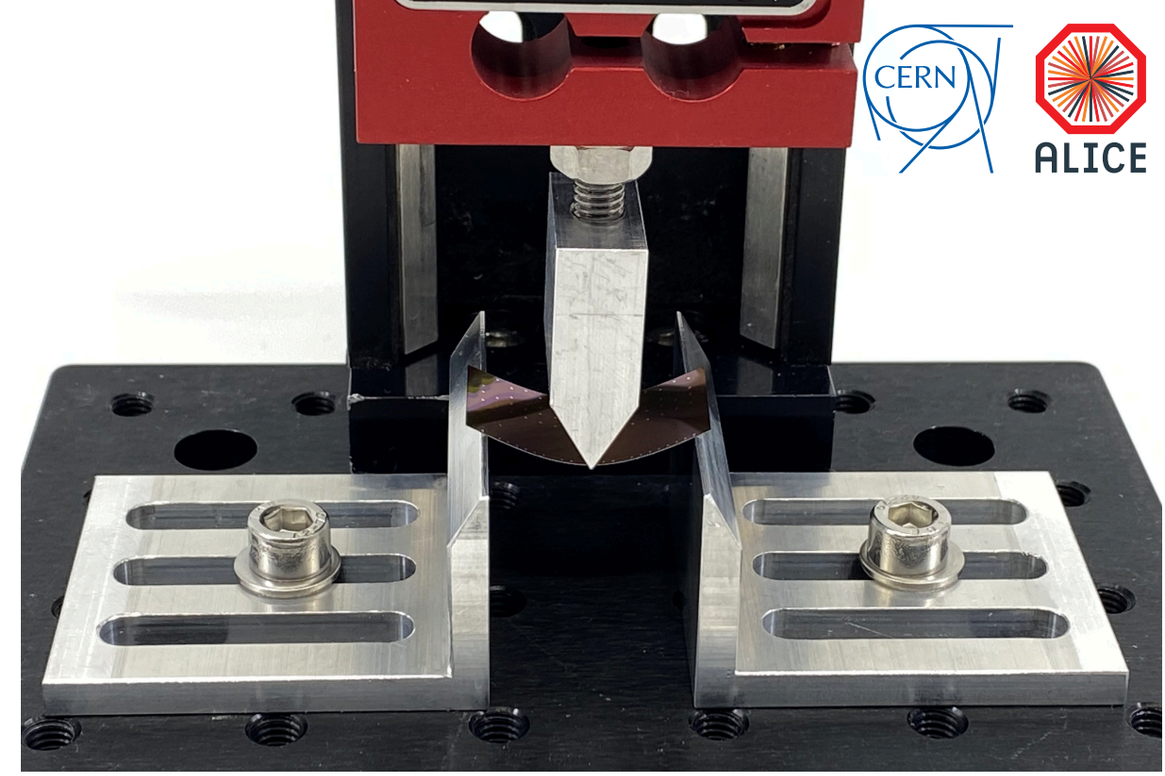

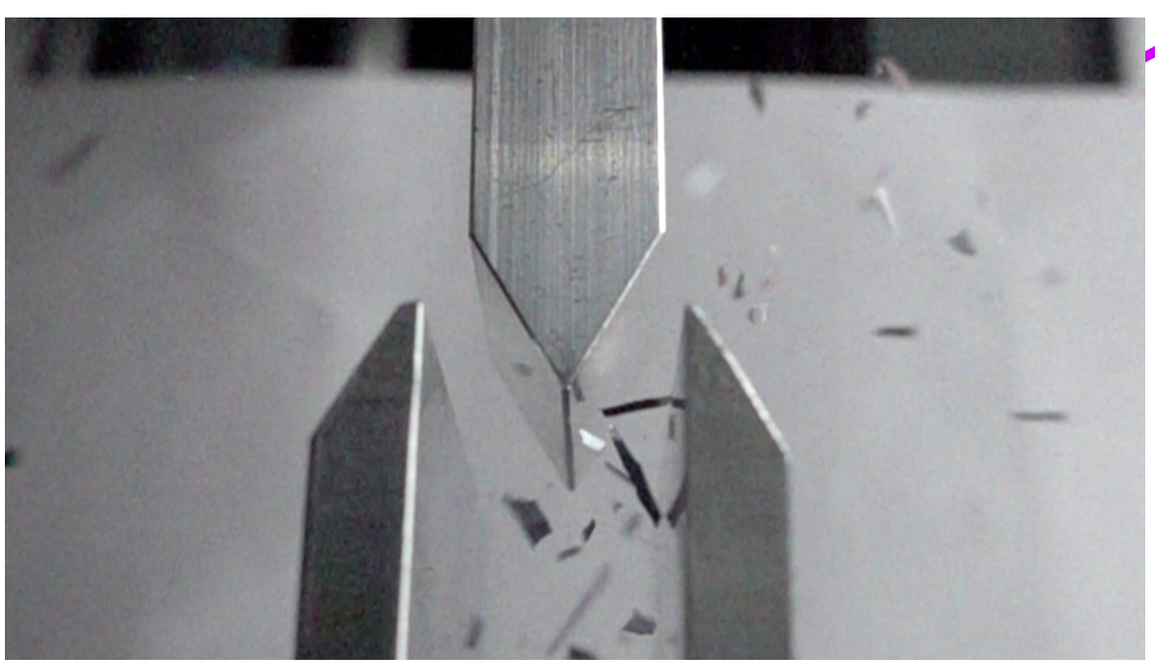

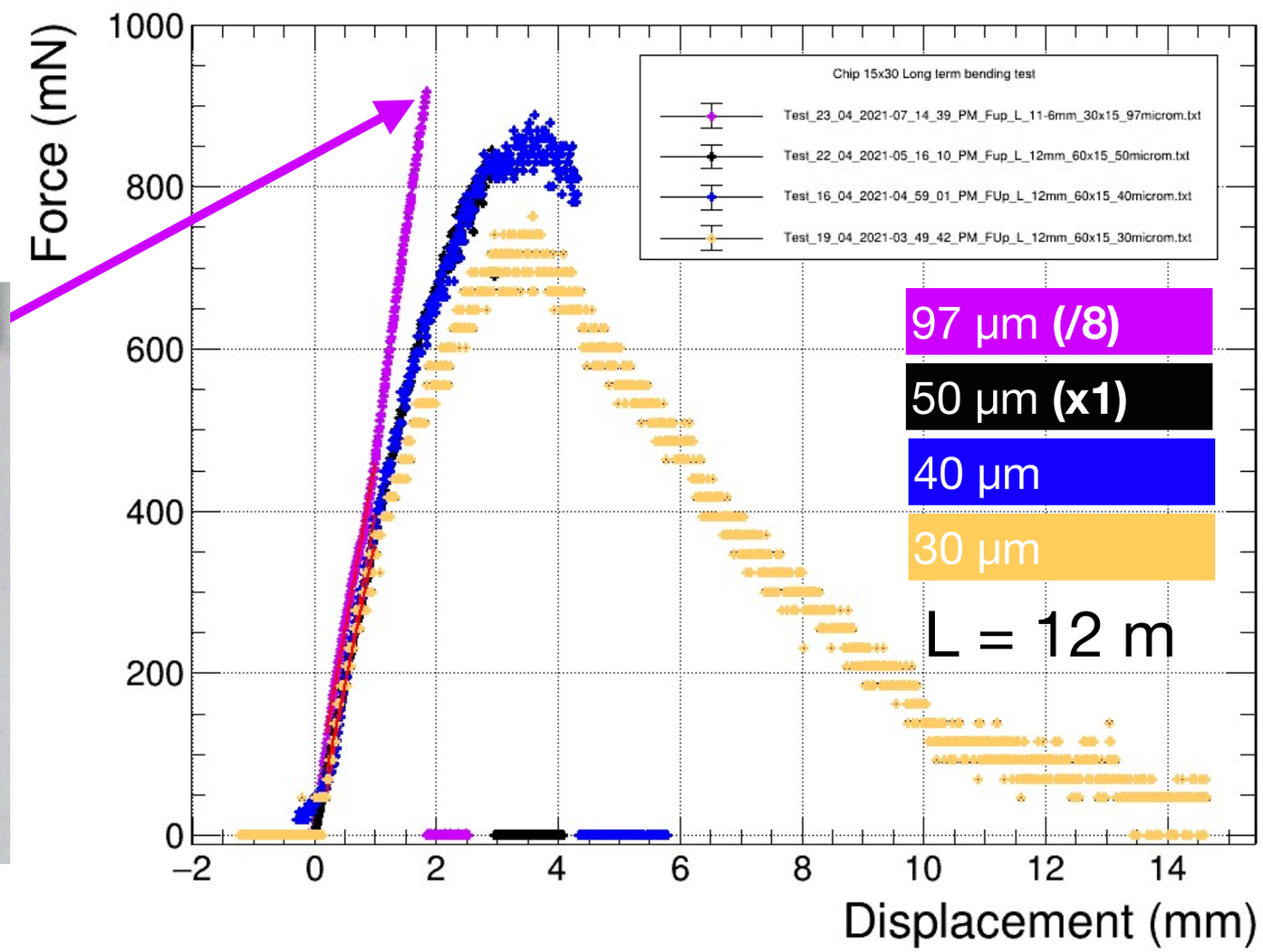

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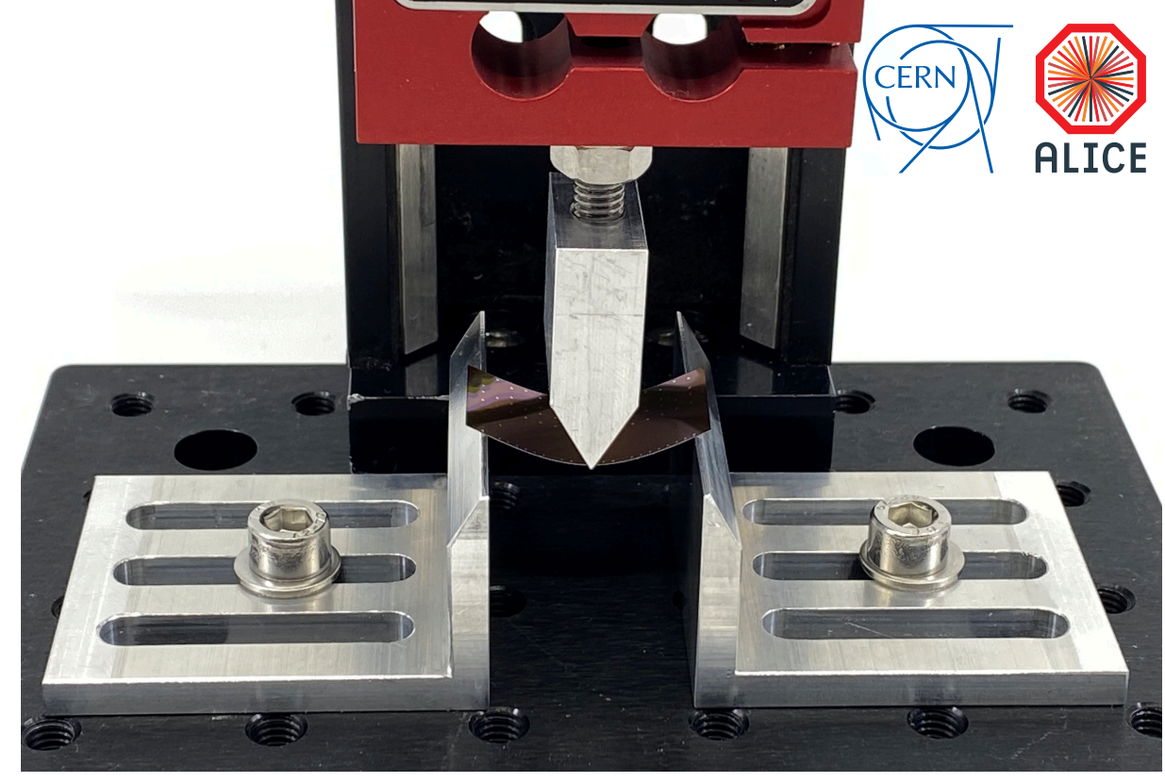

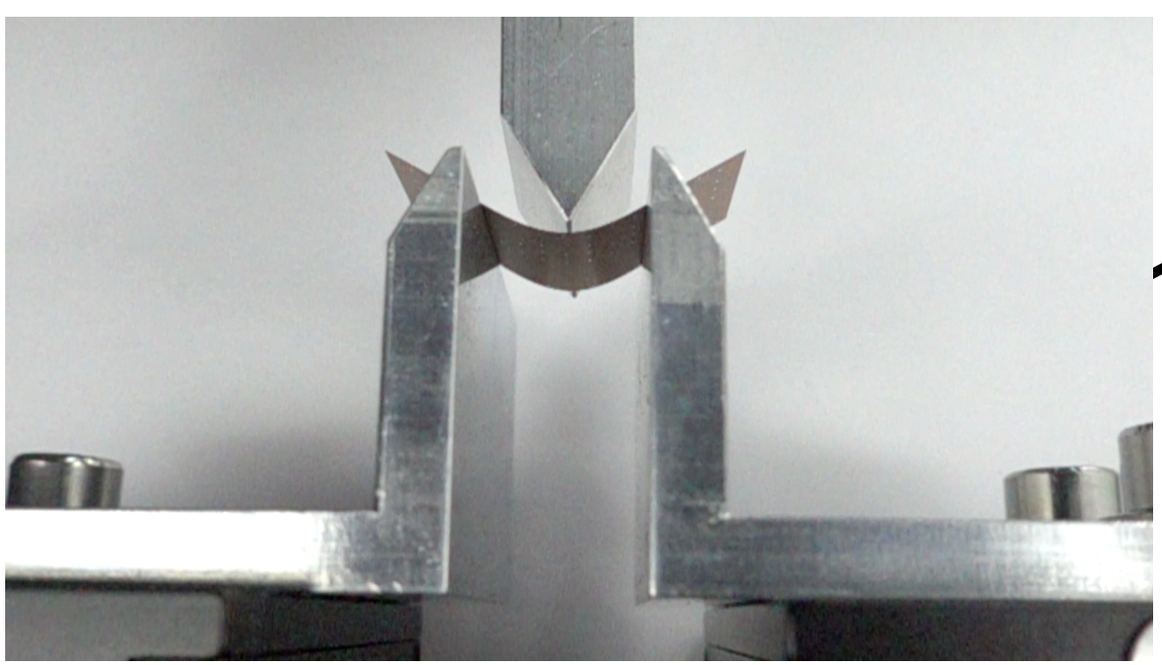

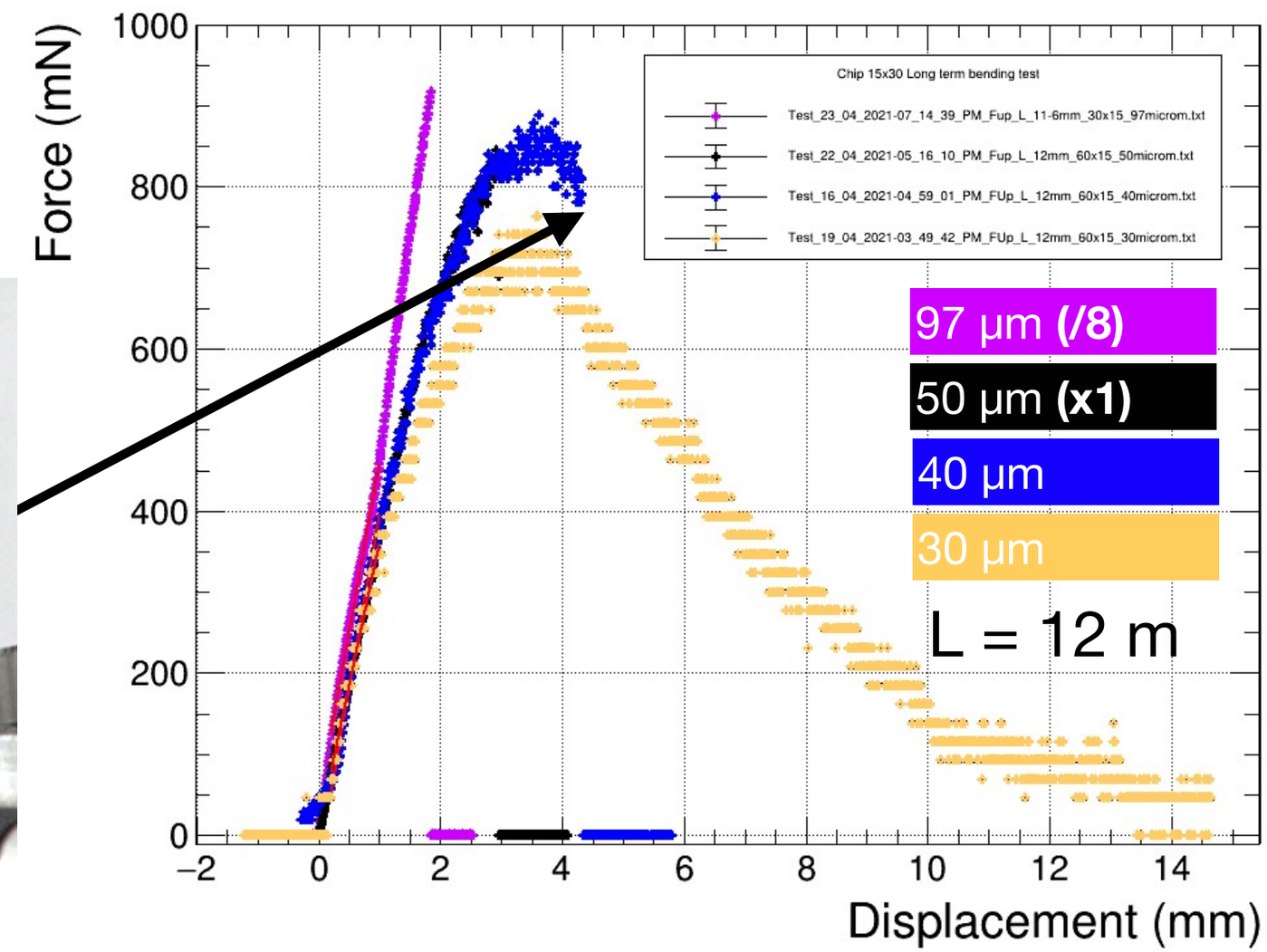

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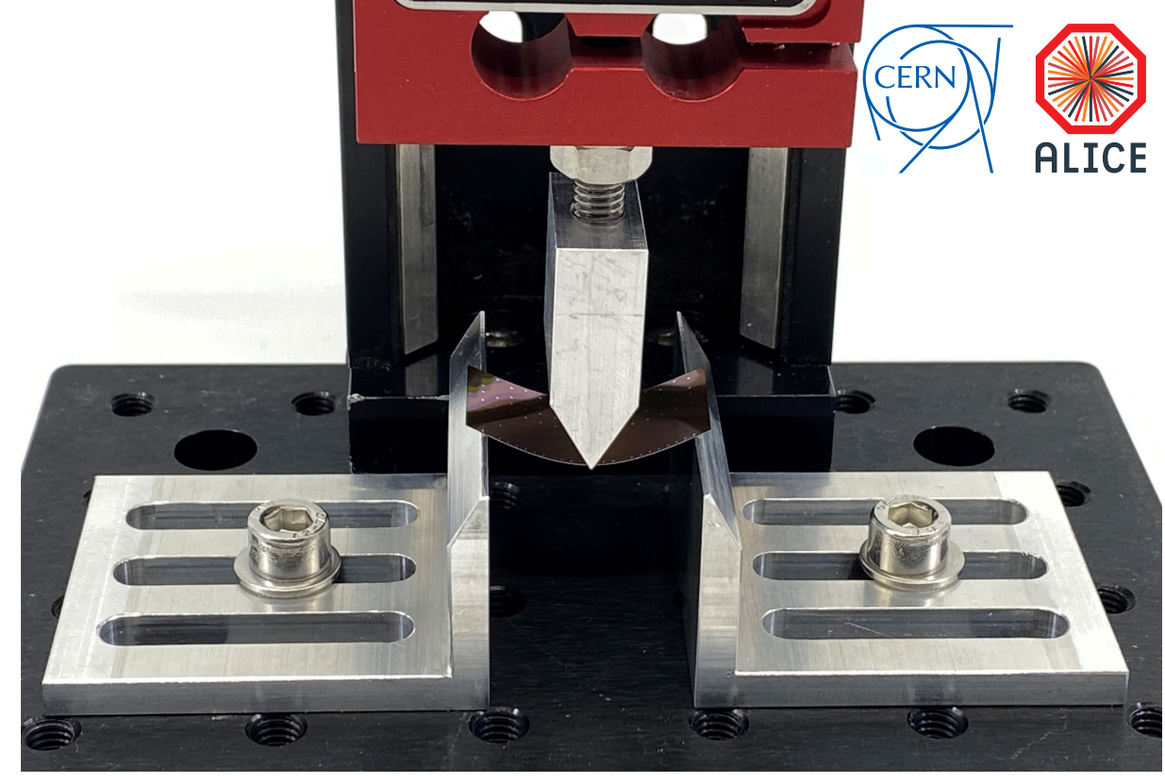

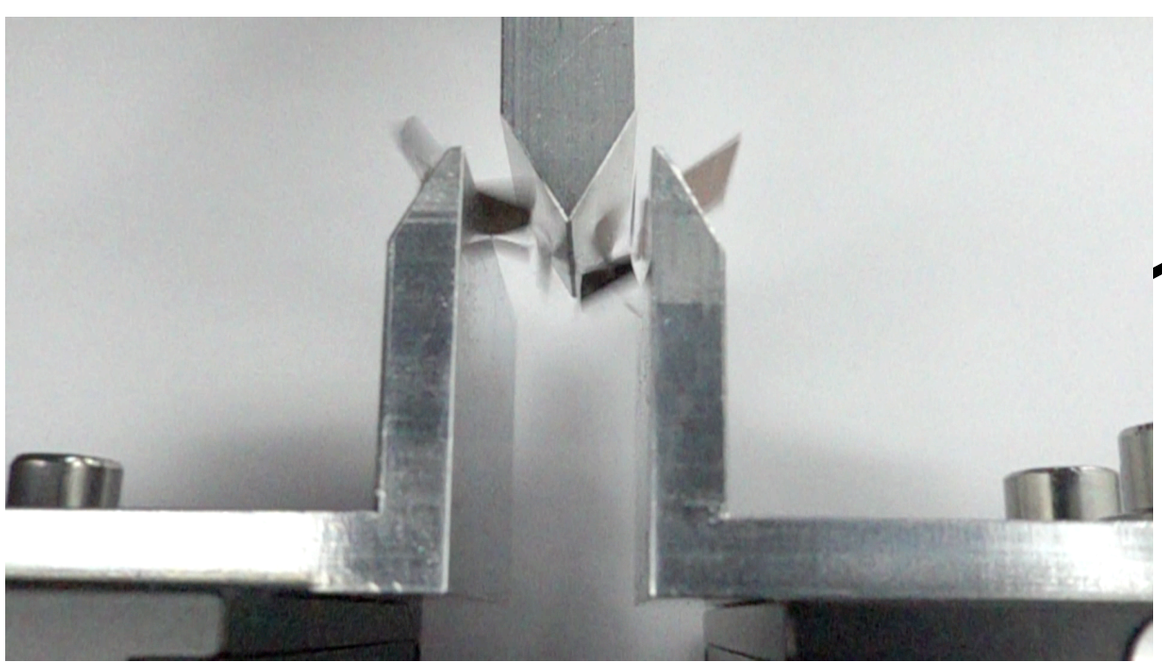

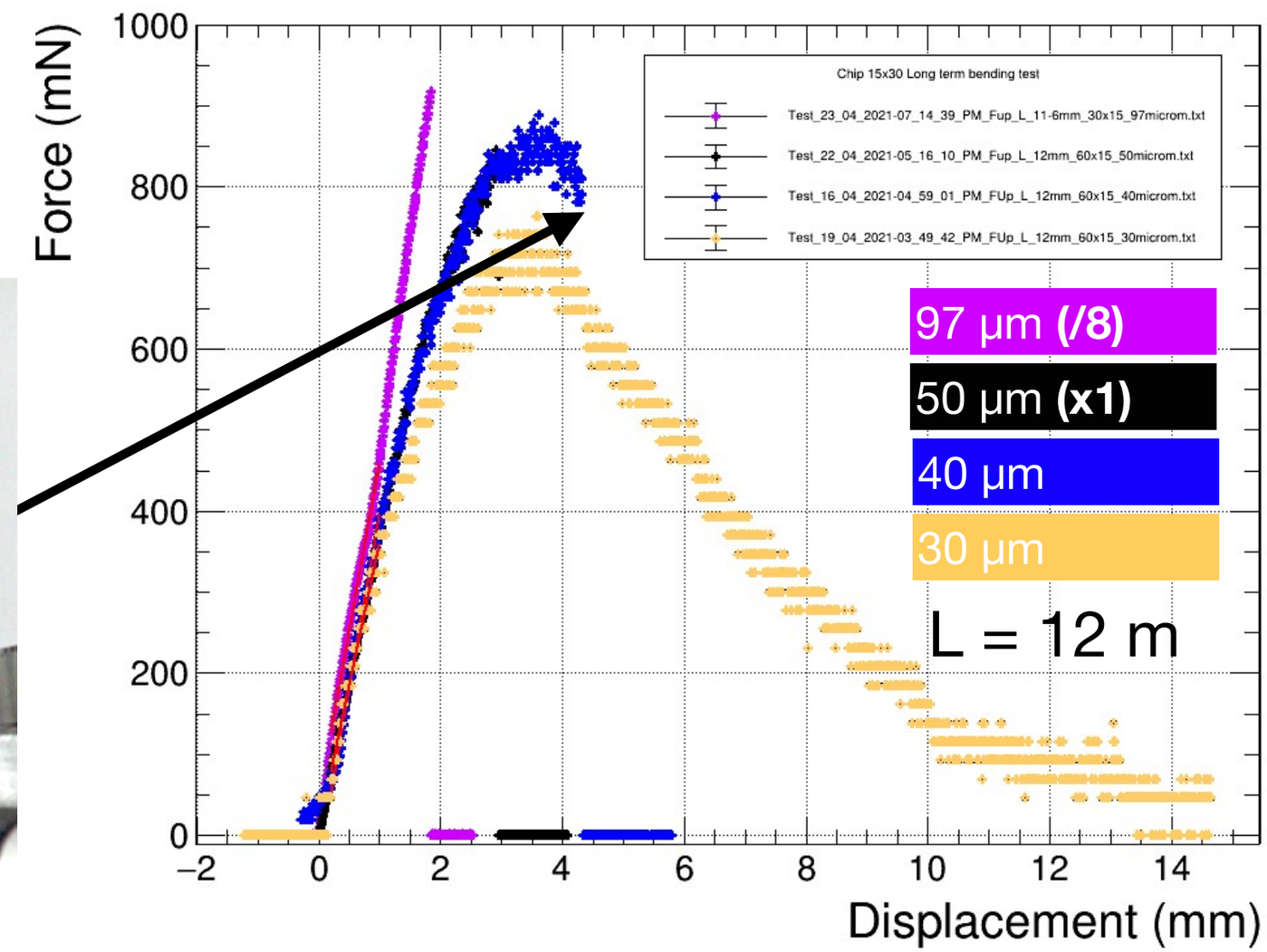

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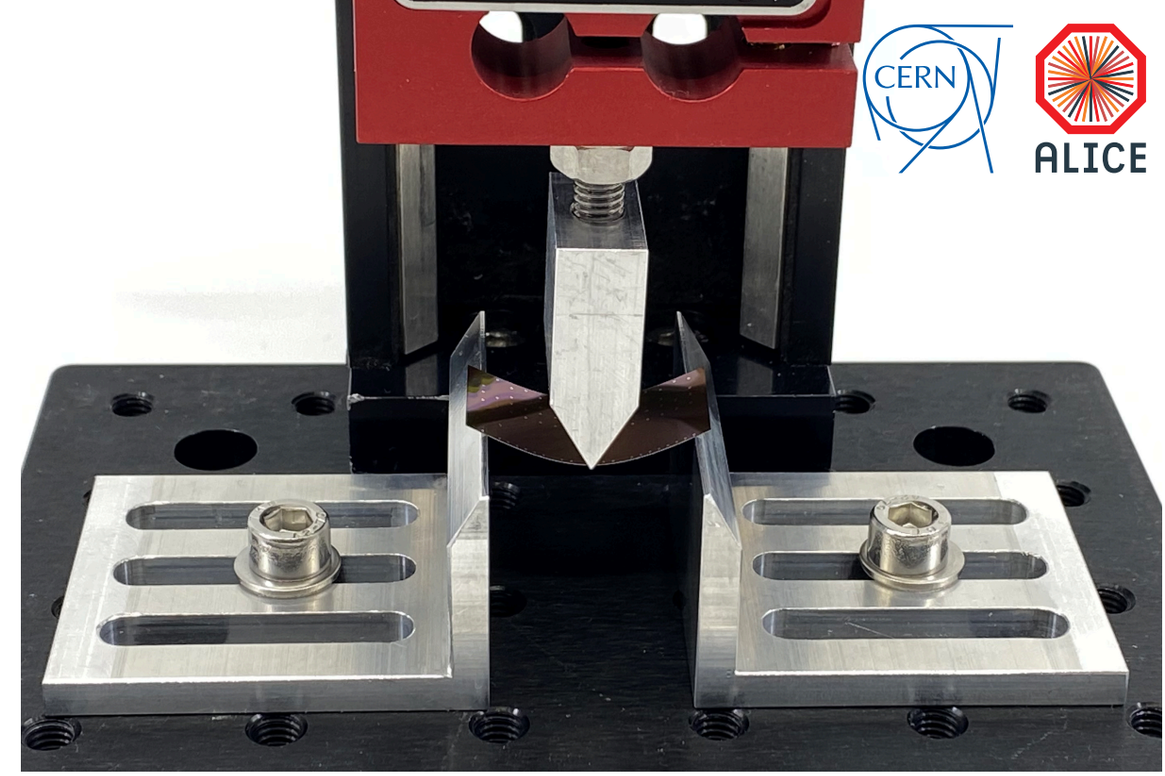
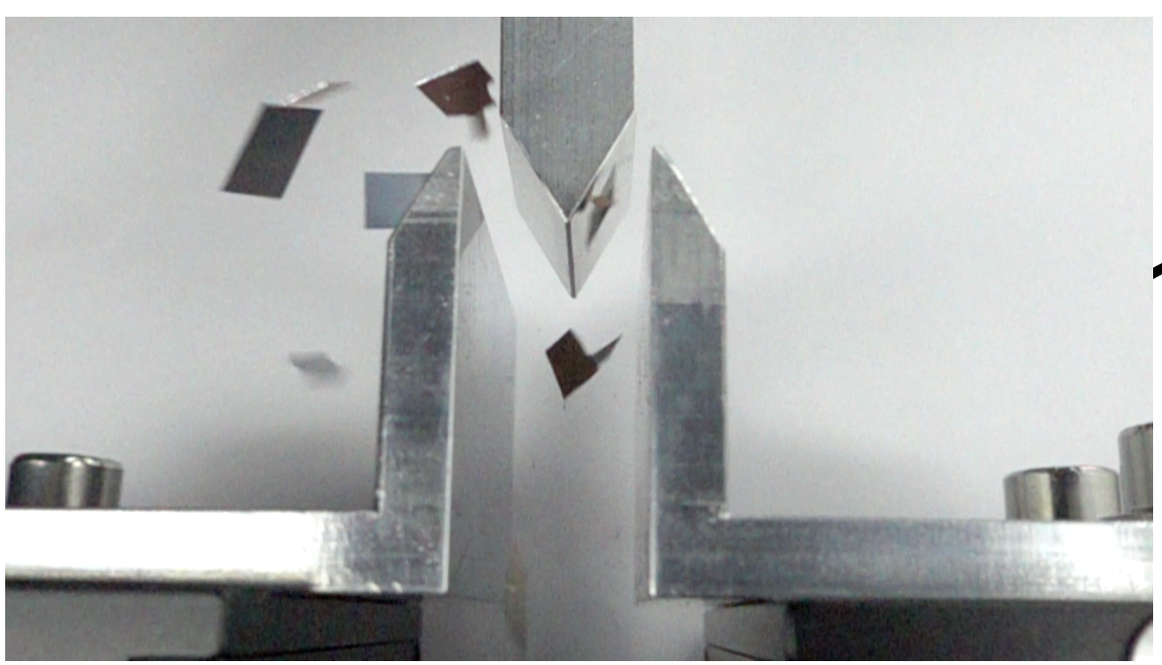
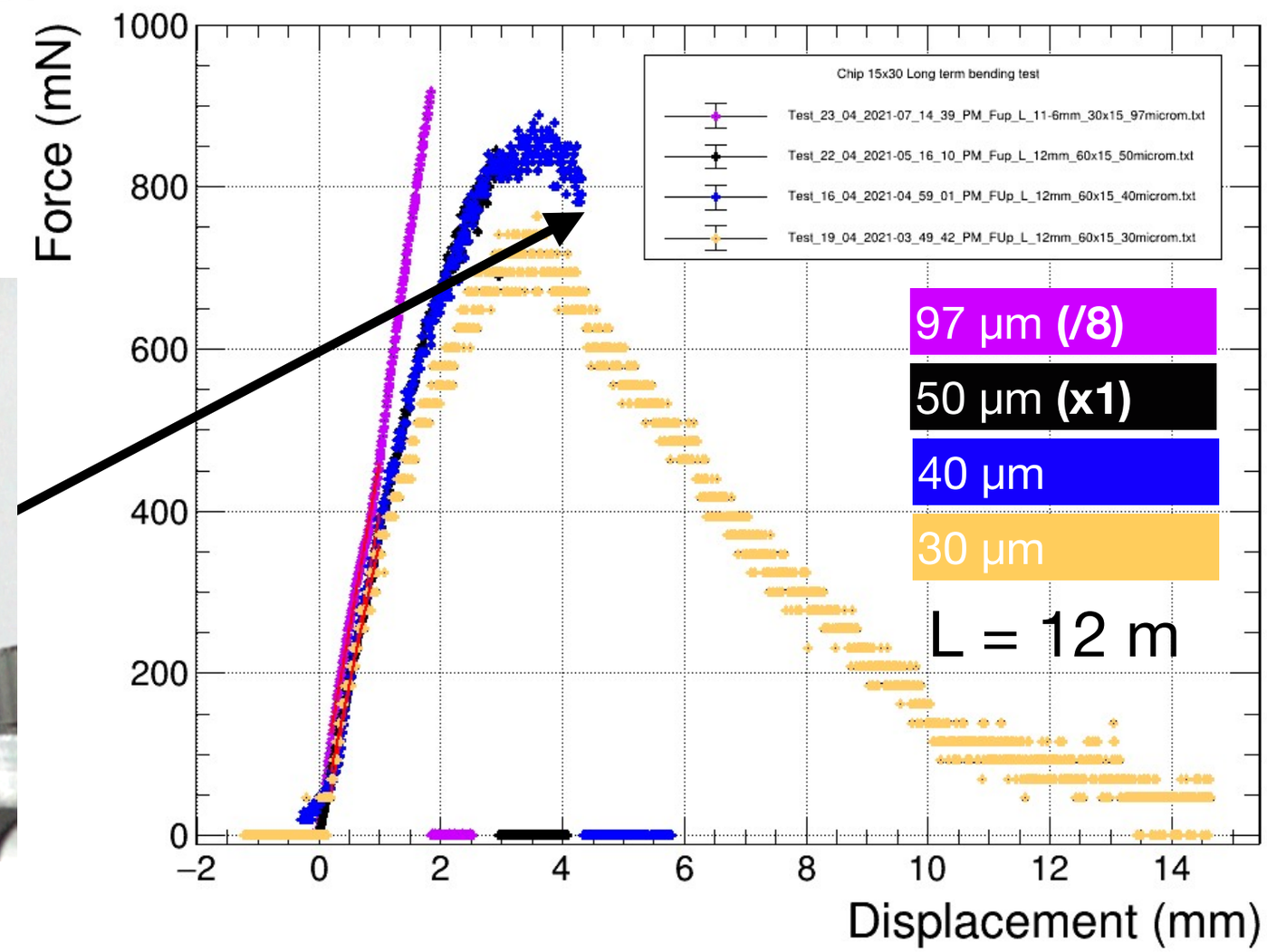
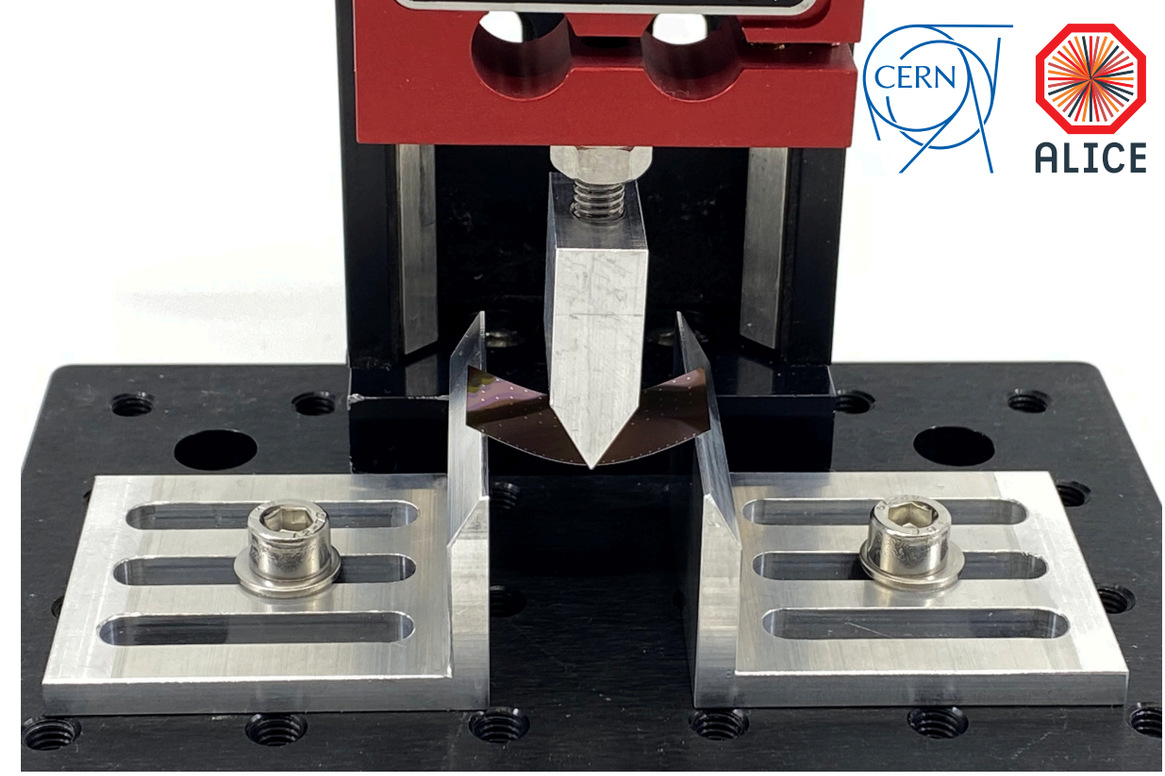


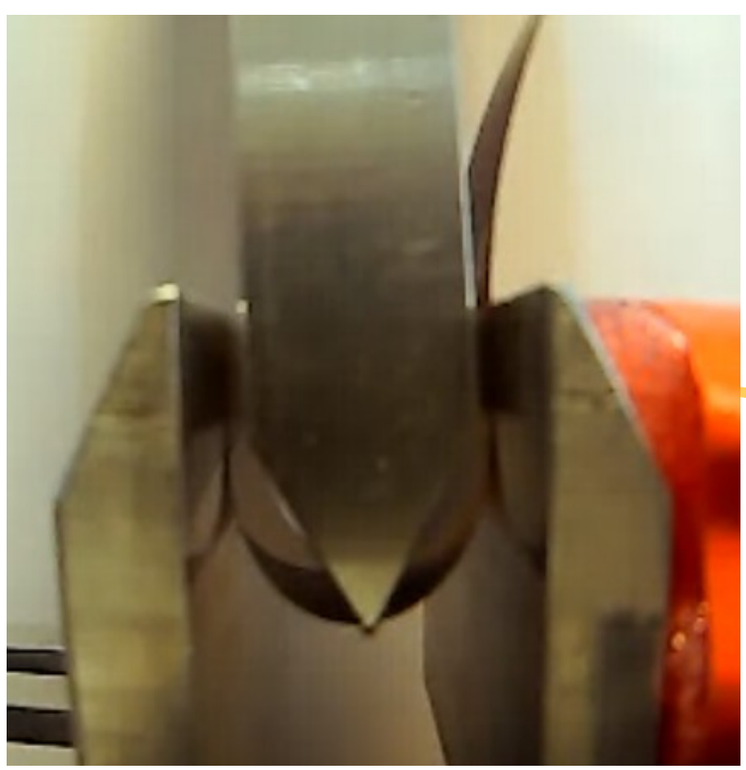


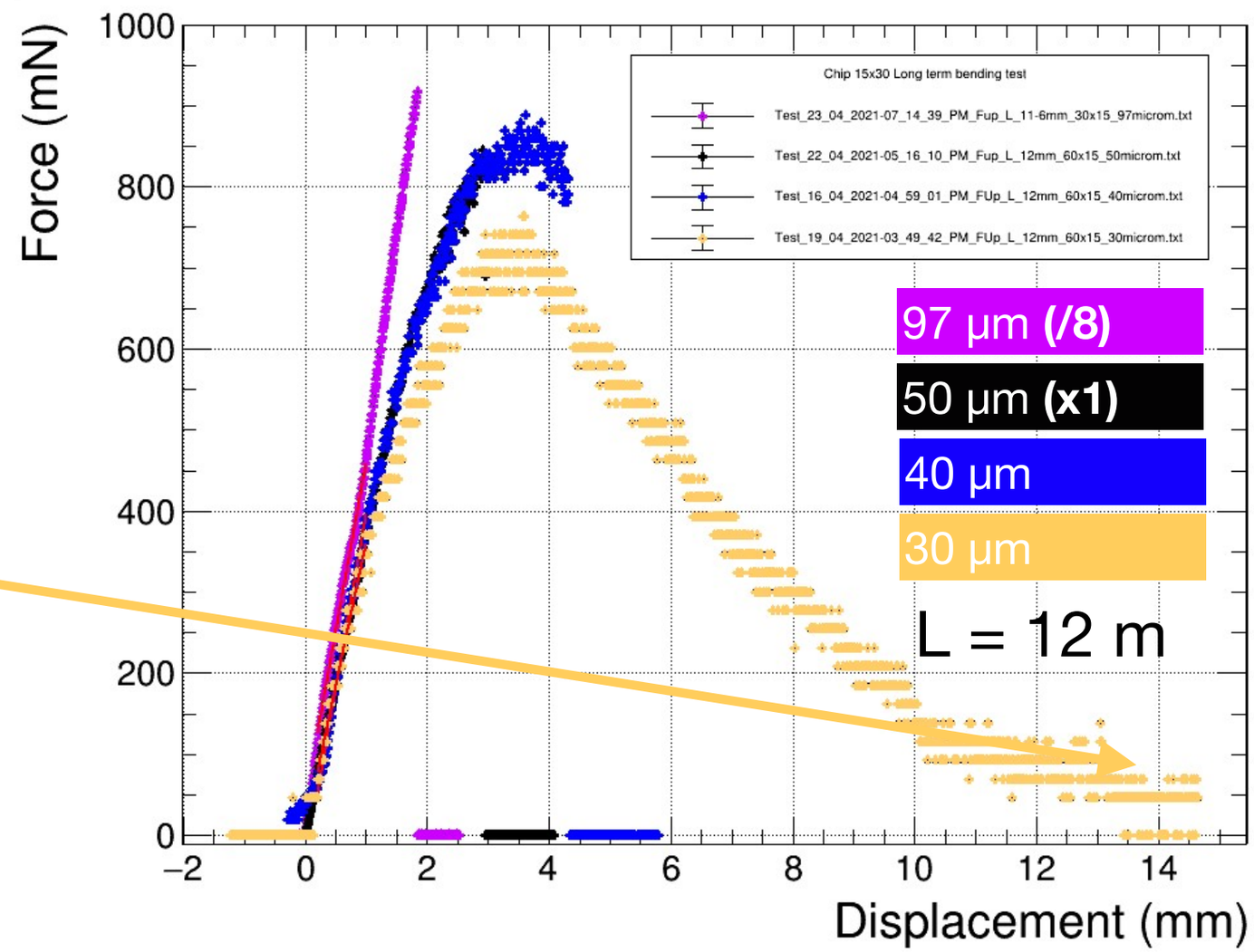


Flexibility of silicon

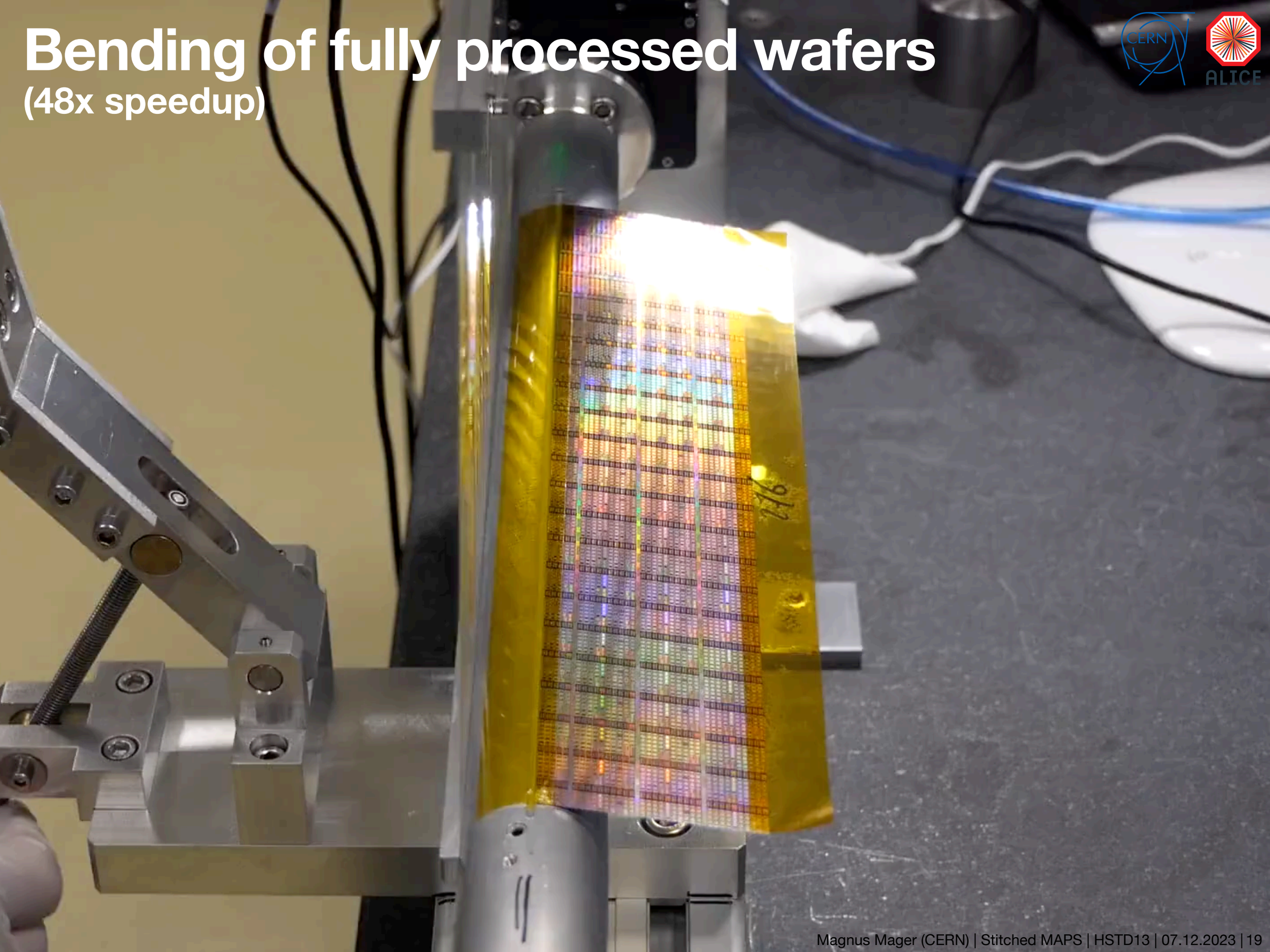
- **Monolithic** Active Pixel Sensors are quite flexible
- Bending force scales as (thickness)$^{-3}$
  - large benefit from thinner sensors





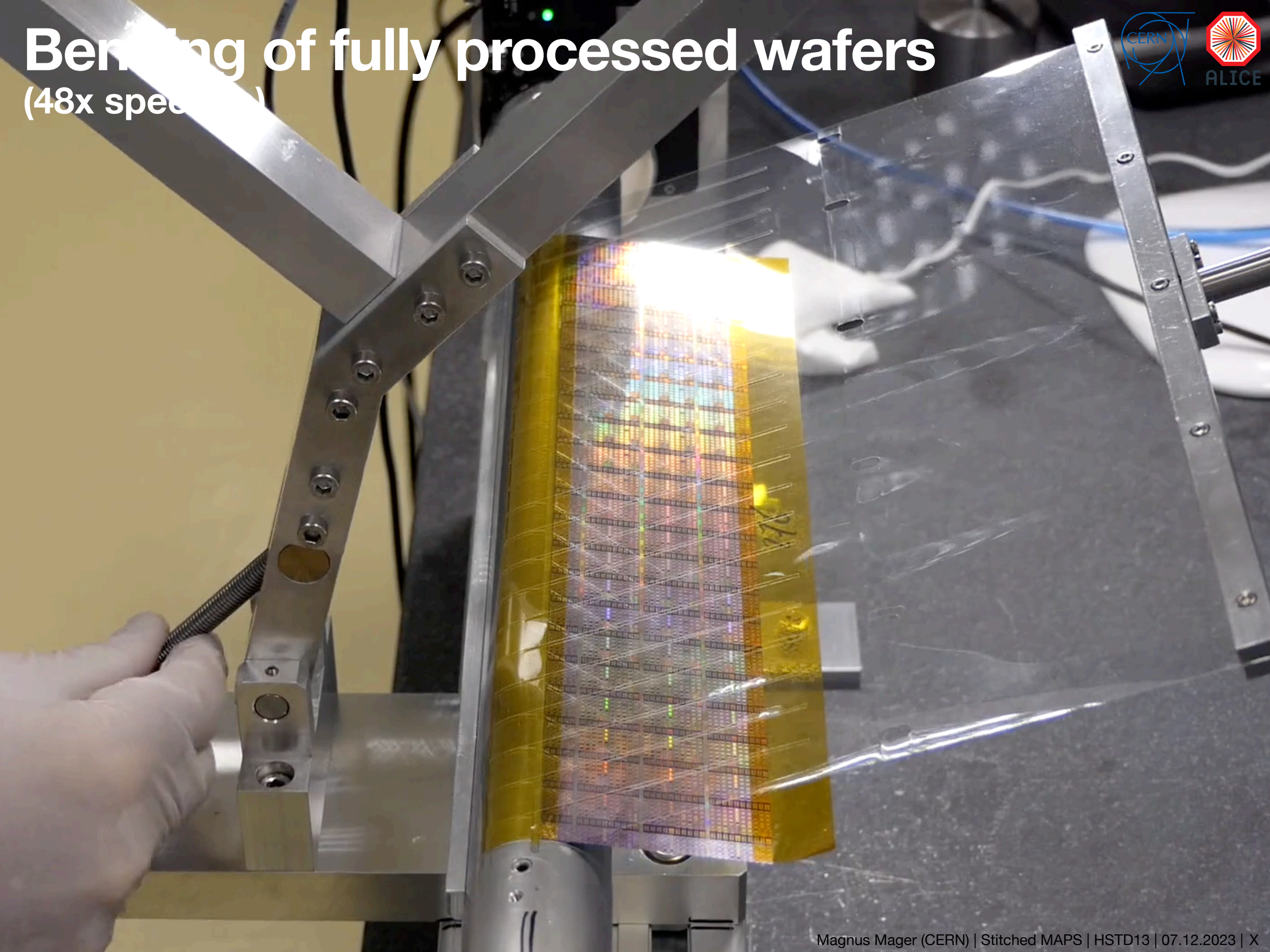


Bending of fully processed wafers
(48x speedup)



Bending of fully processed wafers

(48x speed)



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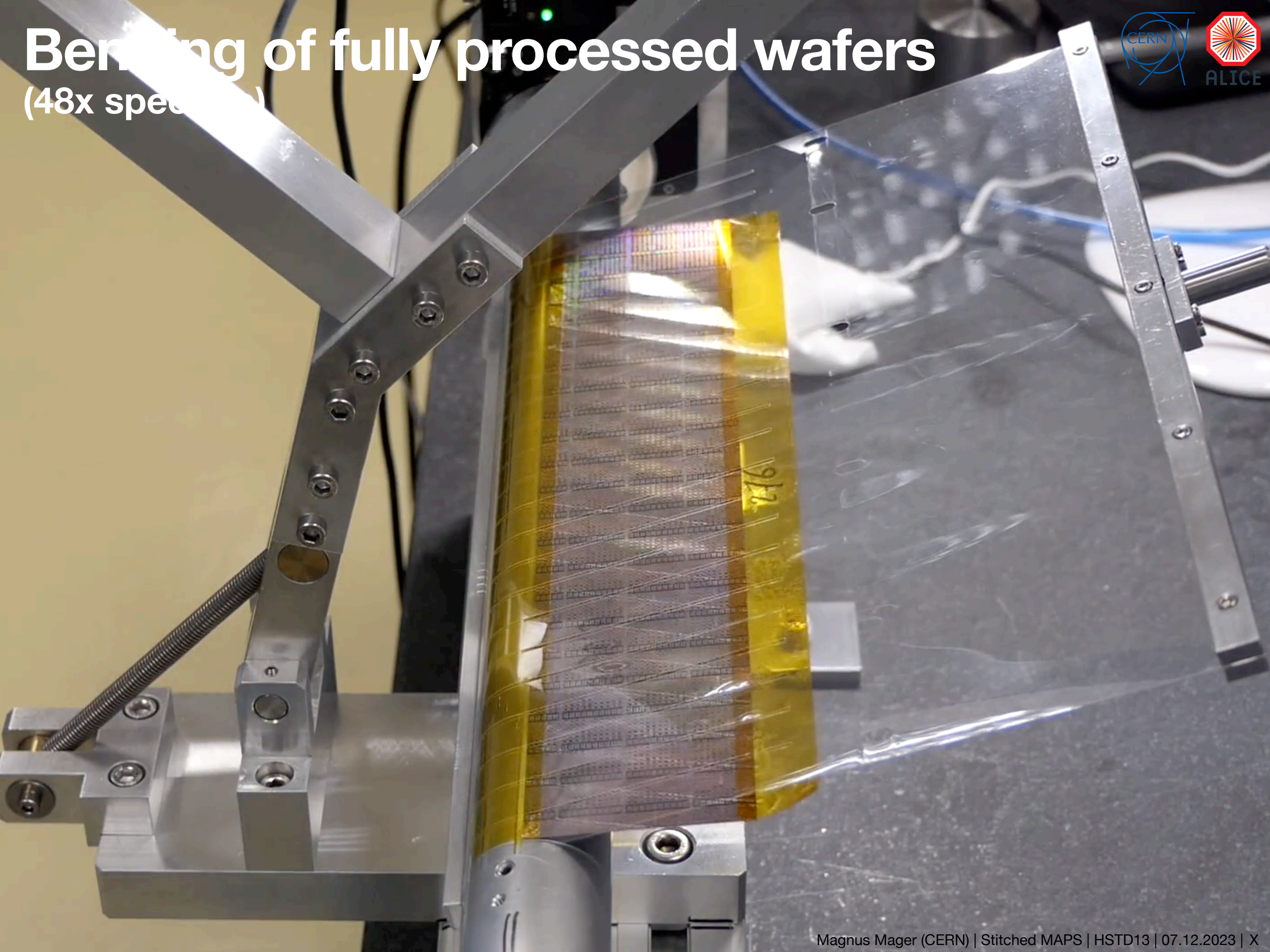

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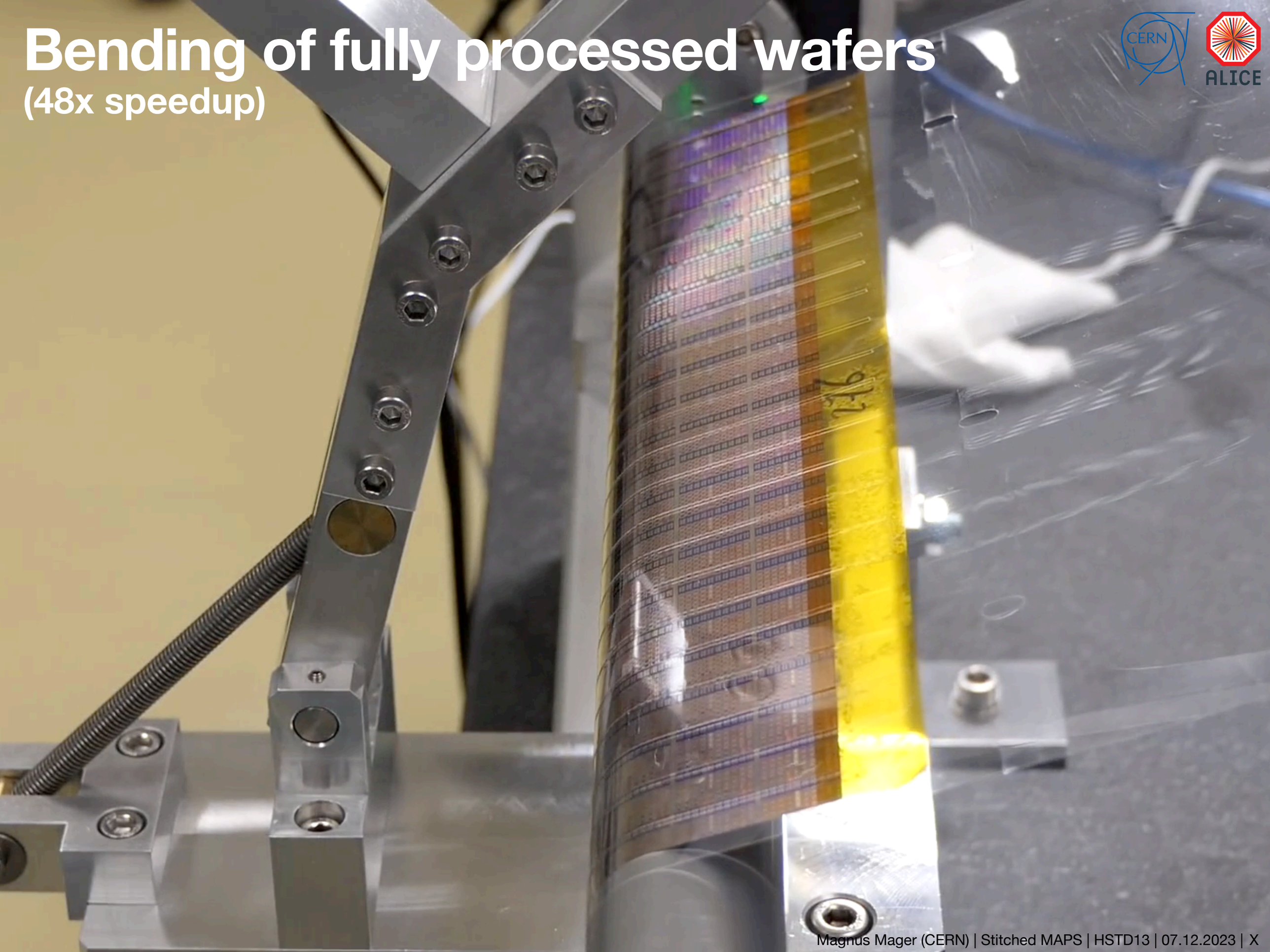
(48x speedup)



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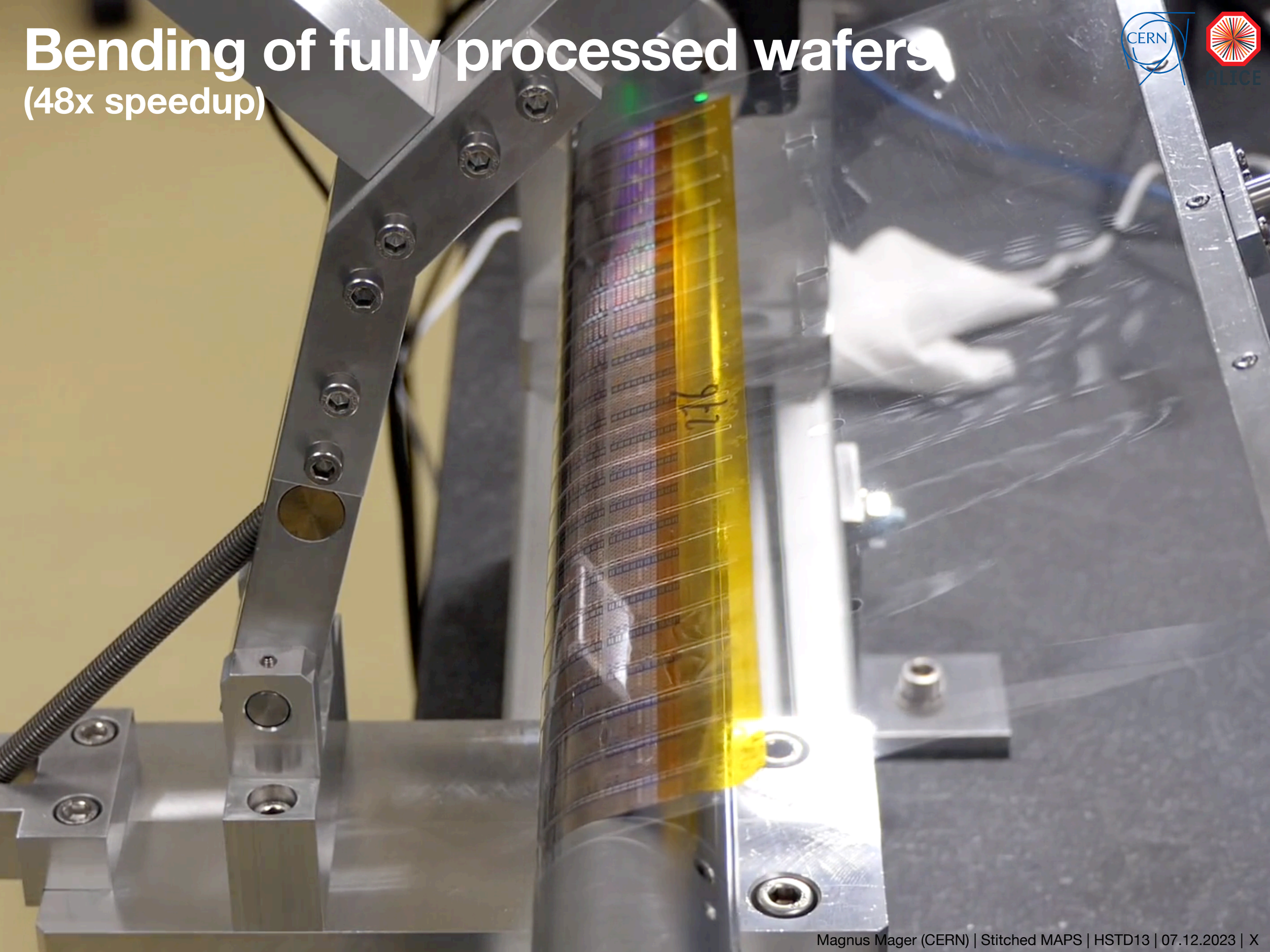

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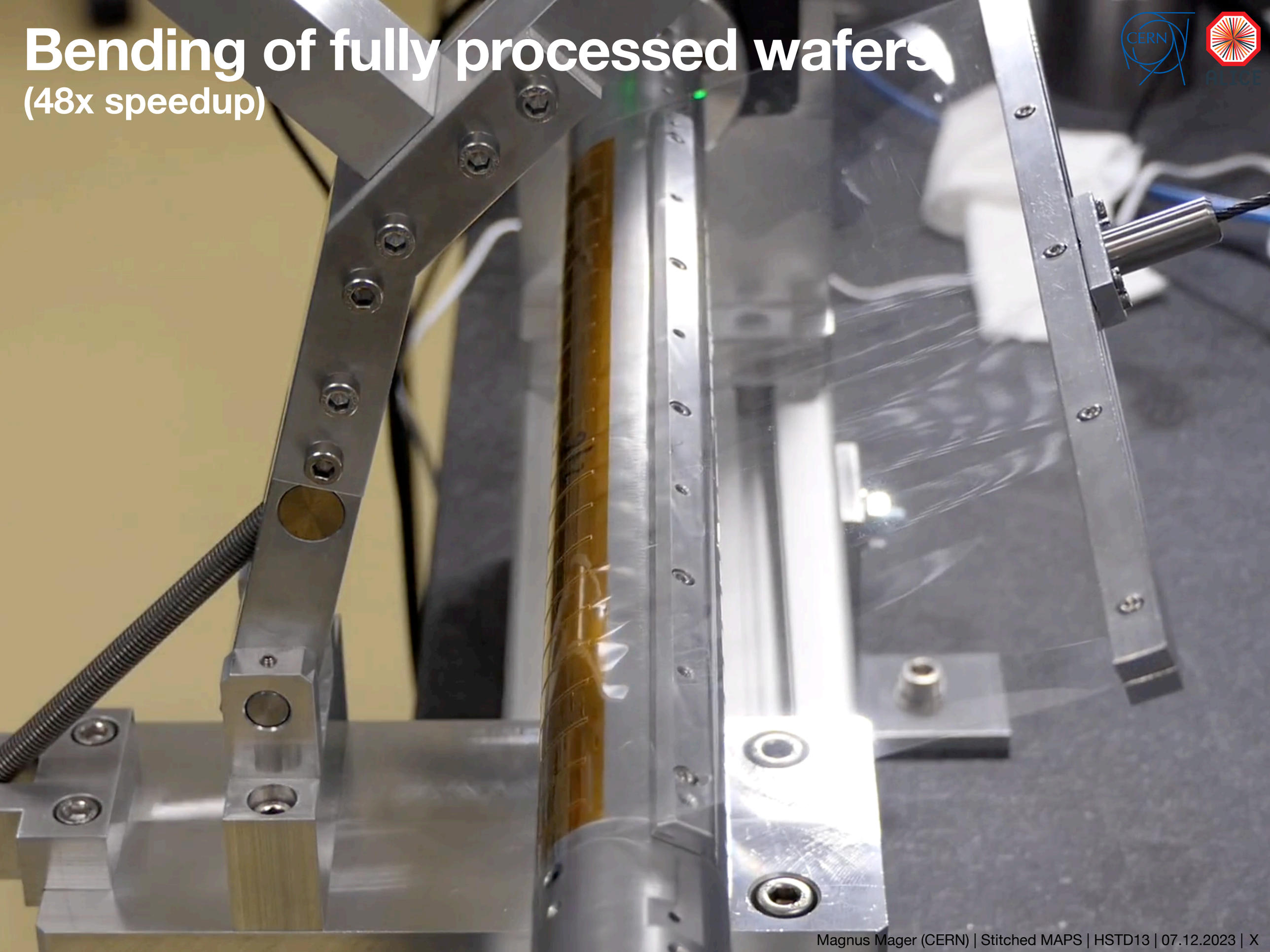

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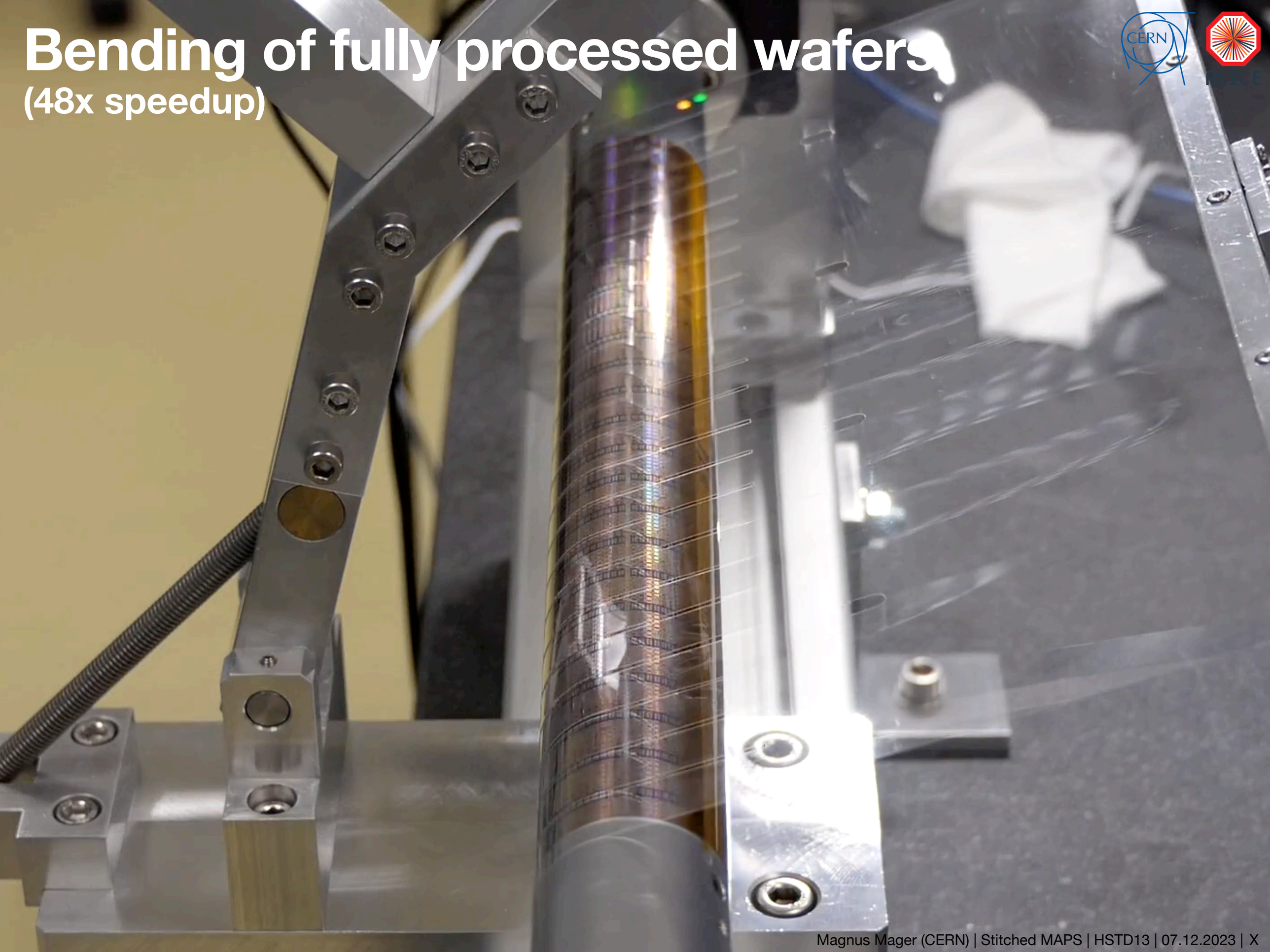
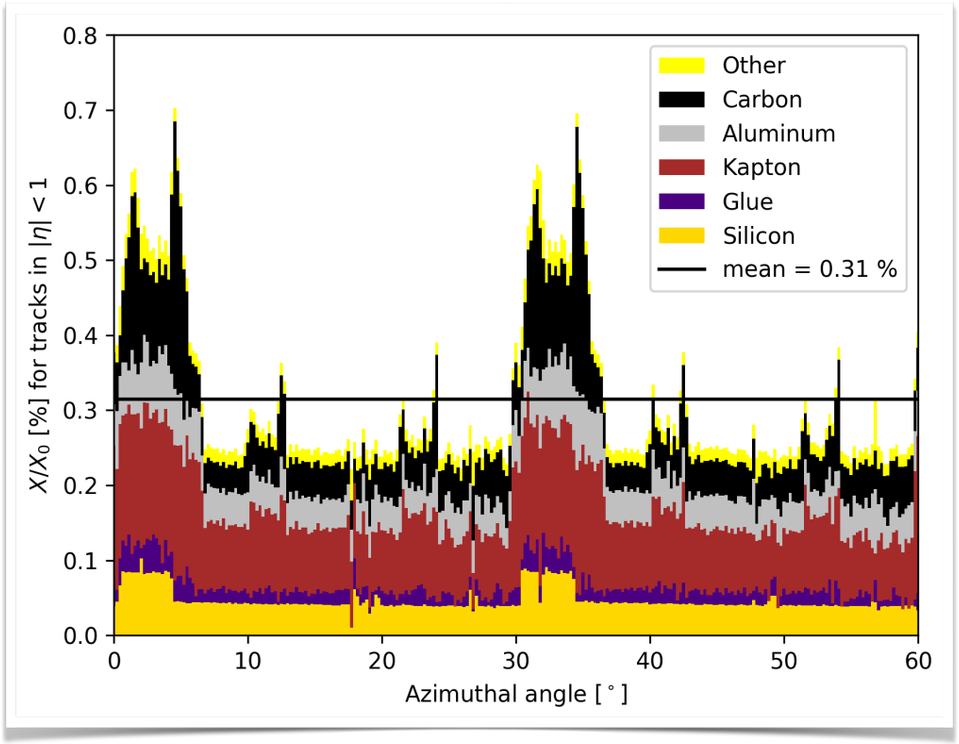
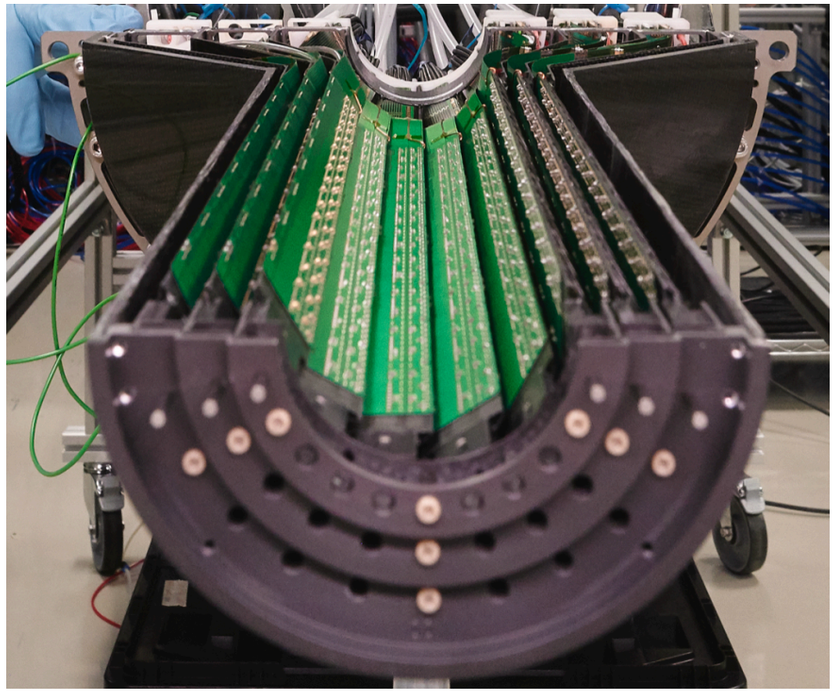
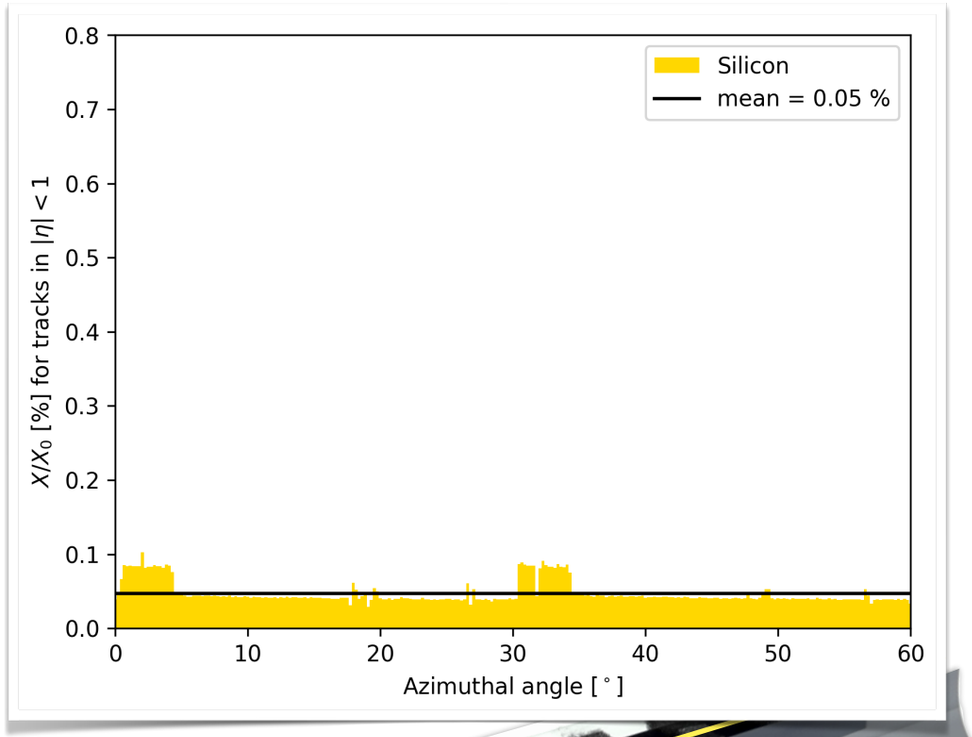


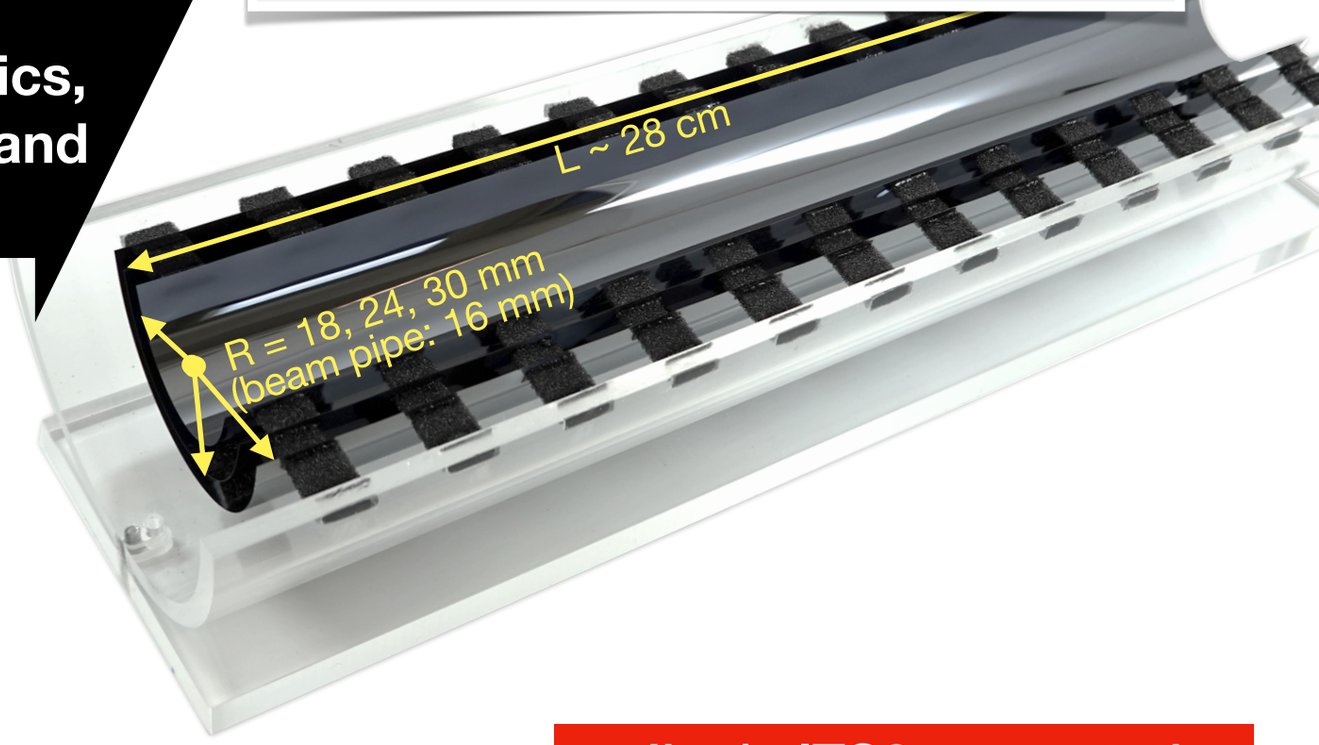
Motivation: material budget





reduction to 1/7th by removing support mechanics, colling, and FPC





→ Jian's ITS3 presentation

Challenges: powering
power consumption

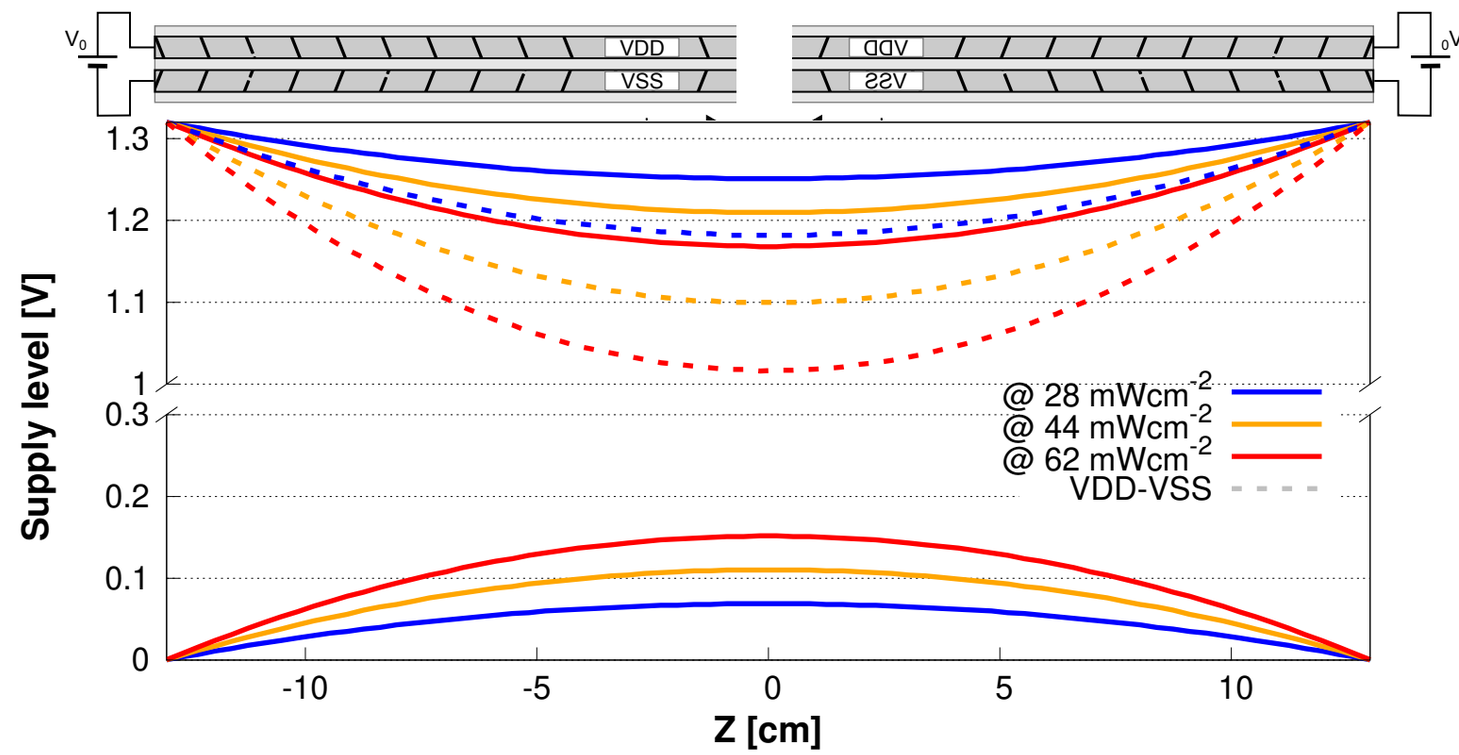
- Power consumption directly impacts material budget
  - power supply (metal, possibly circuit boards)
  - cooling (pipes, water, …)
- To take full advantage of the stitching, an operation with air cooling is wanted, setting a limit around 20-40 mW/cm²
- Off-state leakage is crucial in 65 nm
  - dedicated versions of standard cells are being designed
  - operating temperature needs to be contained
- Also worst process corners are to be watched out very carefully

	Power density [mW cm^{-2}]		
	Expected 25 °C	Max 25 °C	Max 45 °C
Left End Cap (LEC)		791	
Active area (RSU)	28	44	62
Pixel matrix	15	32	51
Biasing	168	168	168
Readout peripheries	432	457	496
Data backbone	719	719	719

Challenges: powering
power distribution

- 65 nm has a core voltage of 1.2 V
  - low power consumption
  - little voltage margin
- Sensor is ideally connected only at the short sides
- Local voltage regulators:
  - possible, but overall power consumption will increase
- Conductivity of metal layers is imposing a limit

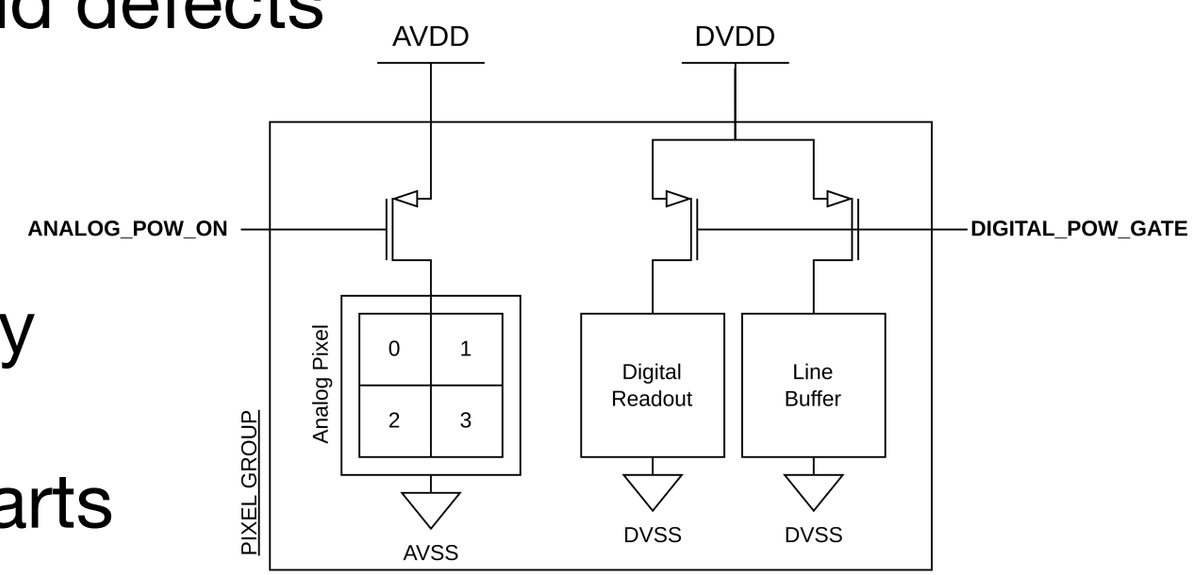
$$\Delta V = k\,(\rho/t)\,J z^2 = k\left(\frac{\rho}{t}\right)\frac{P_\Sigma}{V_0} z^2$$



Low-power design is key!

Challenges: yield
defect density and mitigation

- A wafer with a reasonably complex designs and w/o defects does not exist
- It is key to deal with imperfections and defects smartly
- Twofold strategy:
  - design critical (global) circuits very cautiously (large spacing)
  - allow to disable malfunctioning parts (masking, power-off)



- First prototypes to address the sensitivity and density of faults on different circuit plots *(more on next slides)*
  - MOSS: separate power domains for large pieces of a sensor
  - MOST: switches per small groups of pixels

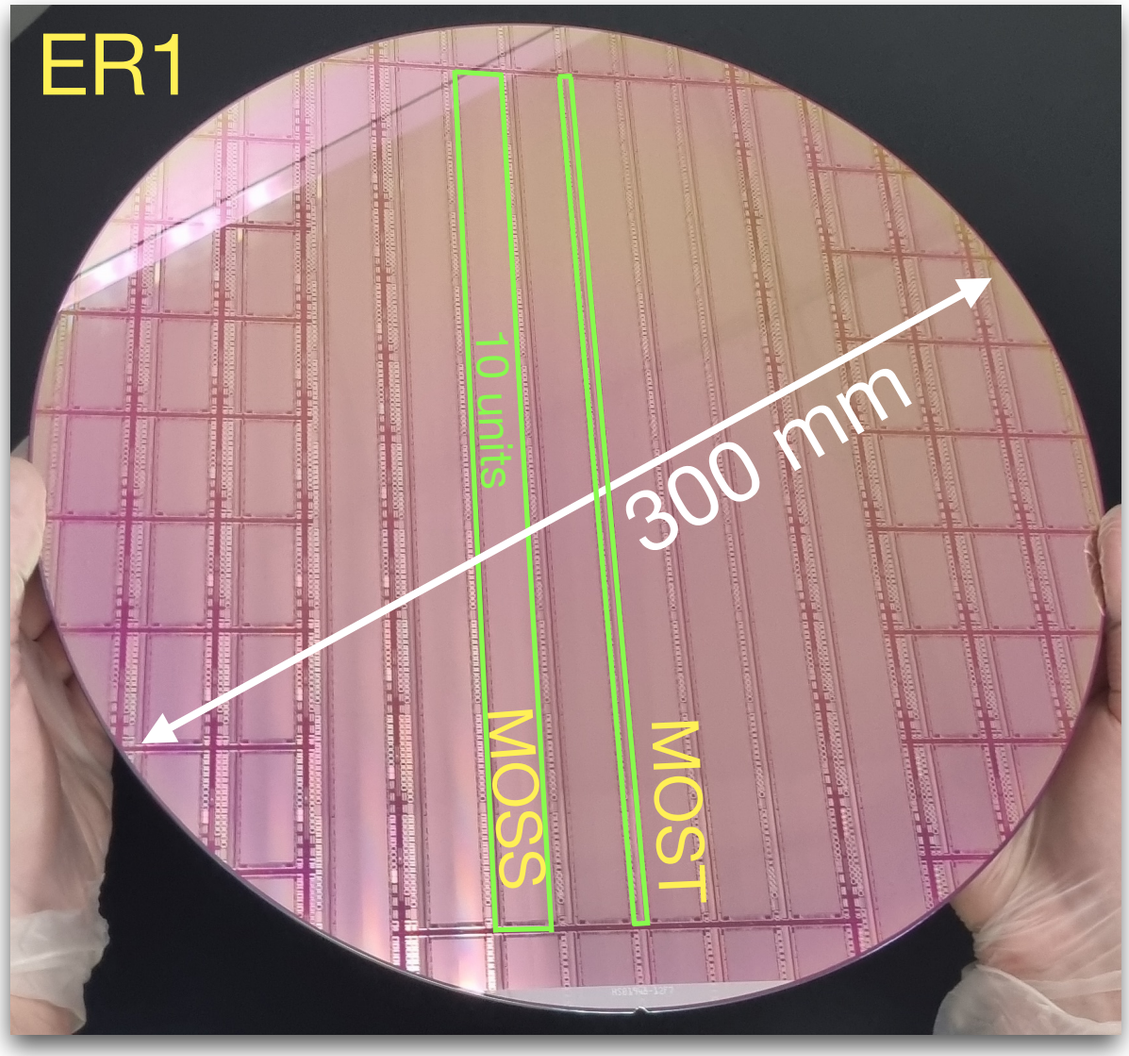
Chip development roadmap
status and plans

past

- **MLR1: first MAPS in TPSCo 65nm** (2021)
  - successfully qualified the 65nm process for particle detectors

present

- **ER1: first stitched MAPS** (2023)
  - large design “exercise”
  - “**MOSS**”: 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 μm²): conservative design, different pitches
  - “**MOST**”: 2.5 x 259 mm, 0.9 MPixel (18 x 18 μm²): more dense design



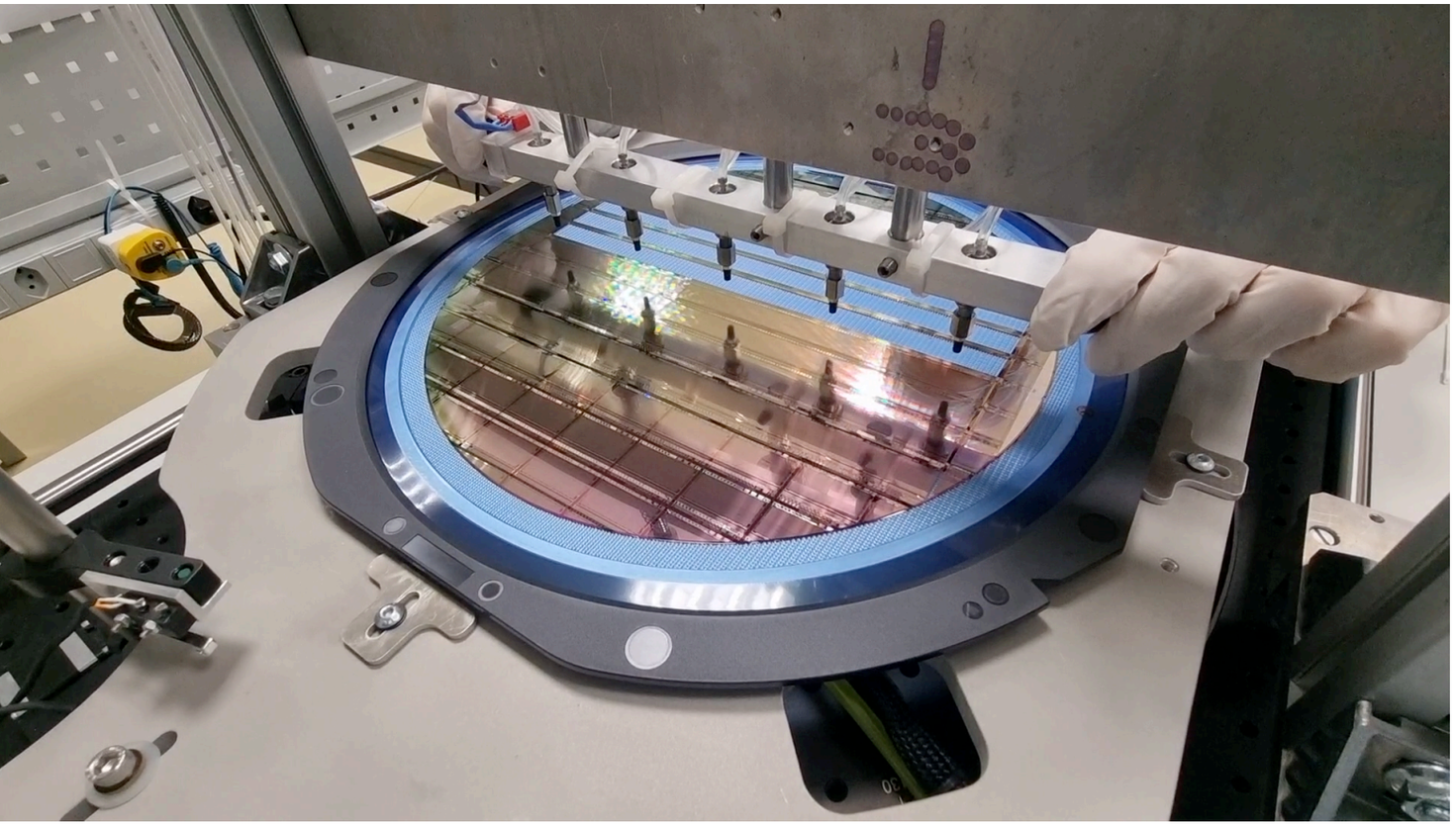
future

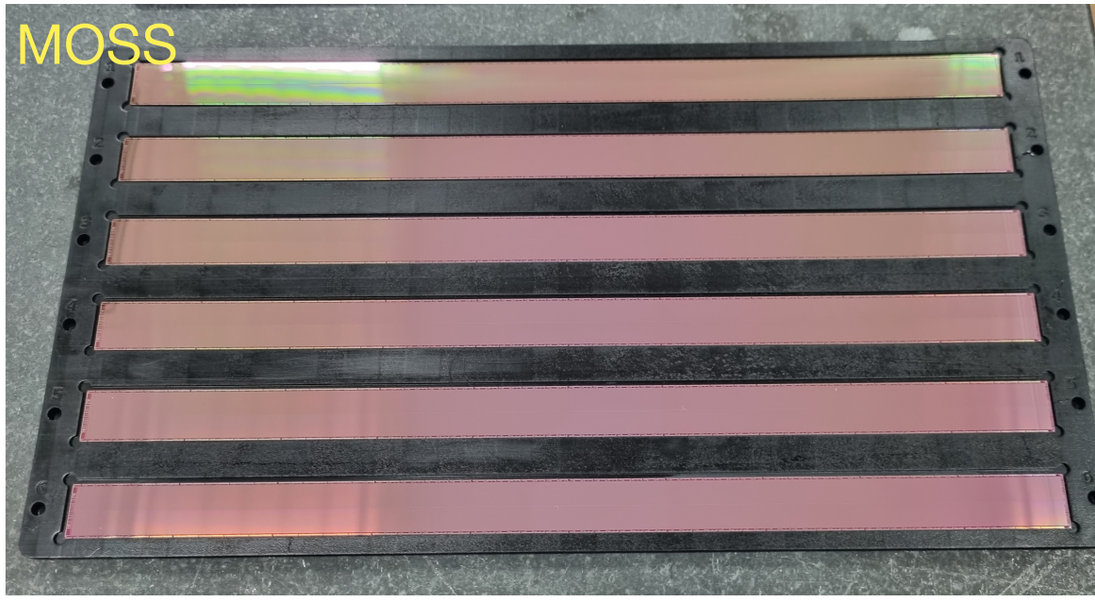
- **ER2: first ITS3 sensor prototype** (2024)
- **ER3: ITS3 sensor production** (2025)

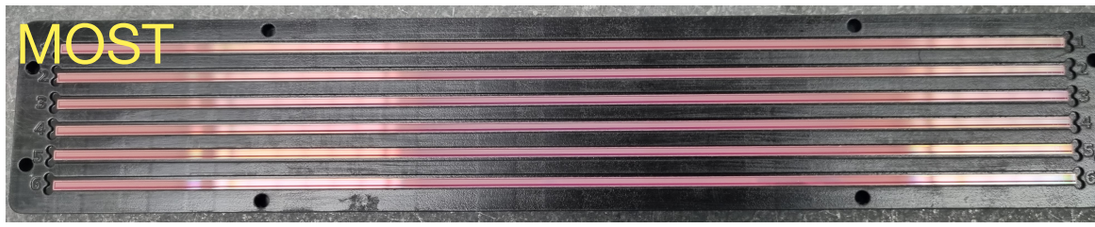
Prototypes: handling

ER1

- ER1 wafers are thinned down to 50 μm
- Tools to pick, handle and ship chips have been developed







A set of dedicated tools have been developed — handling is under control

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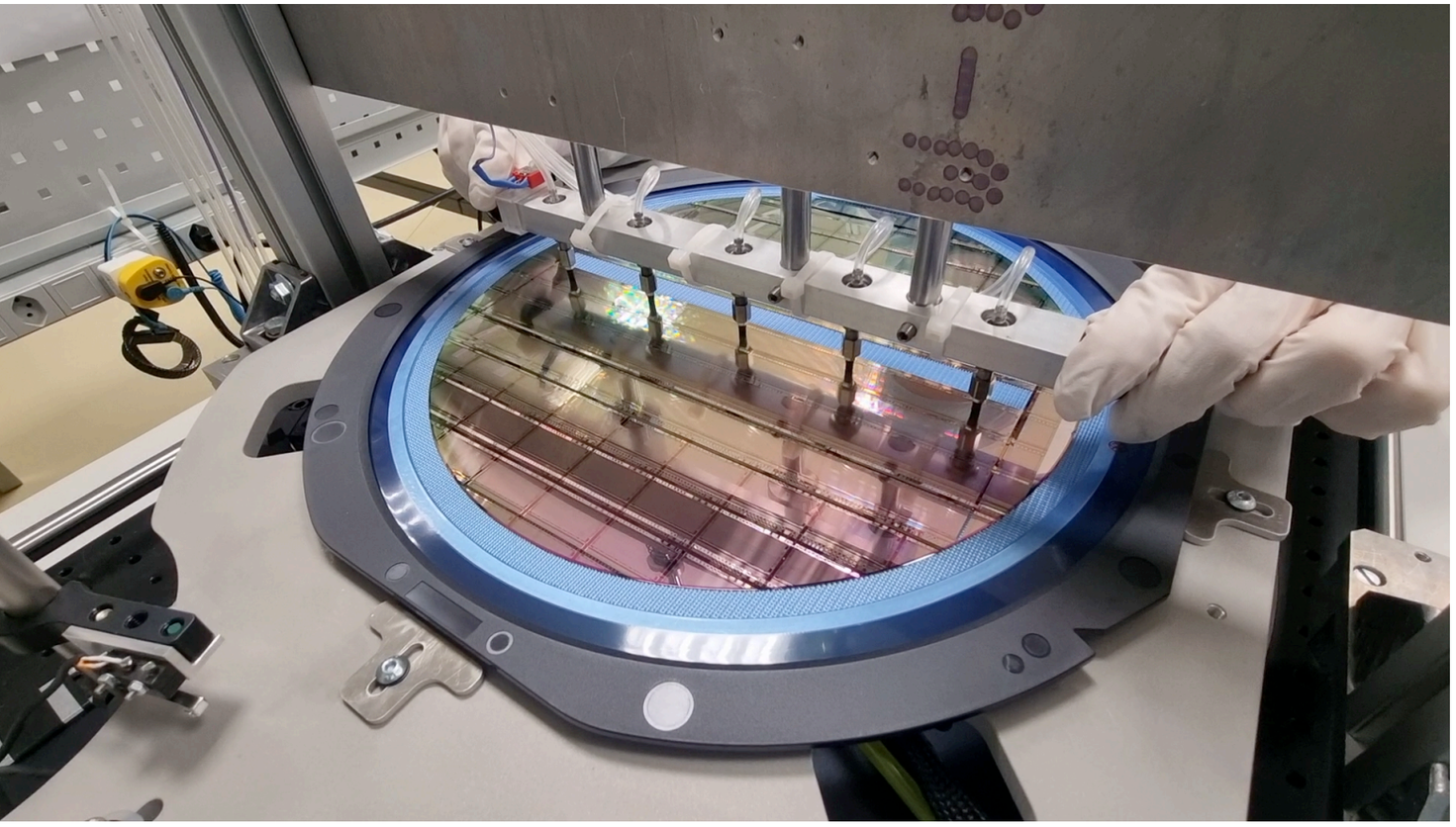

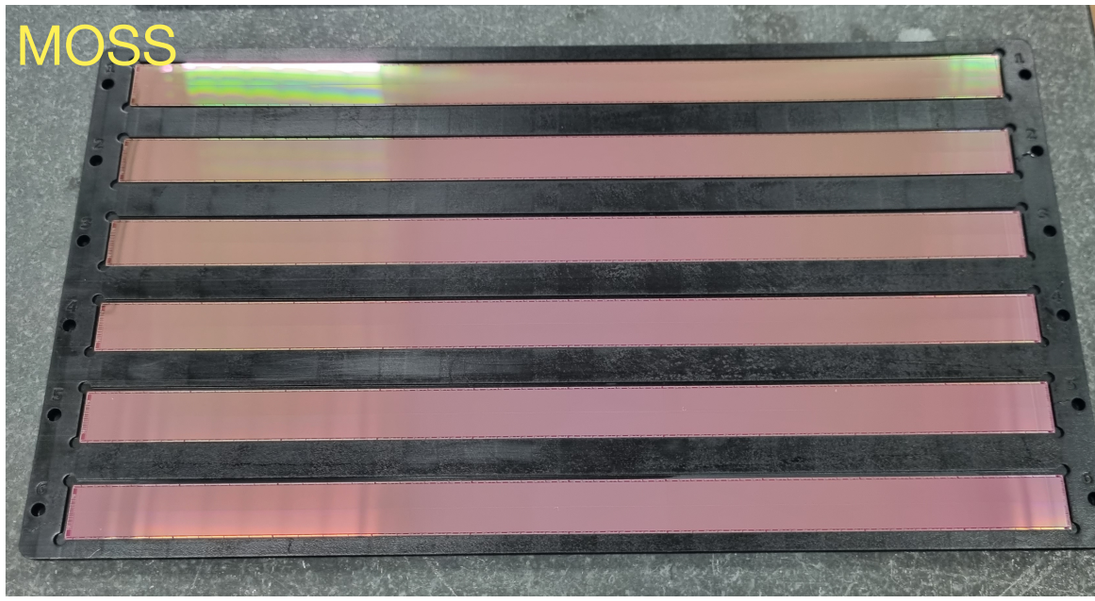

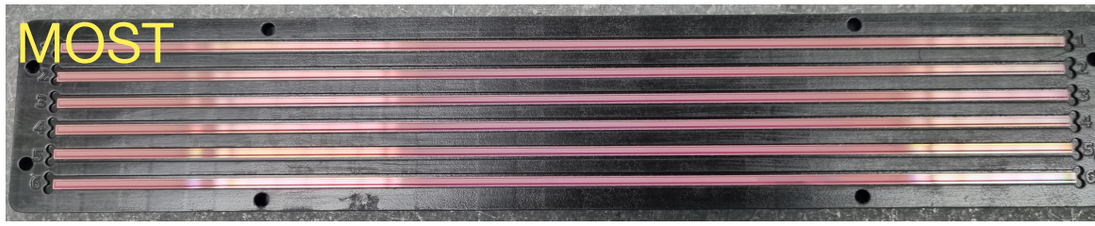

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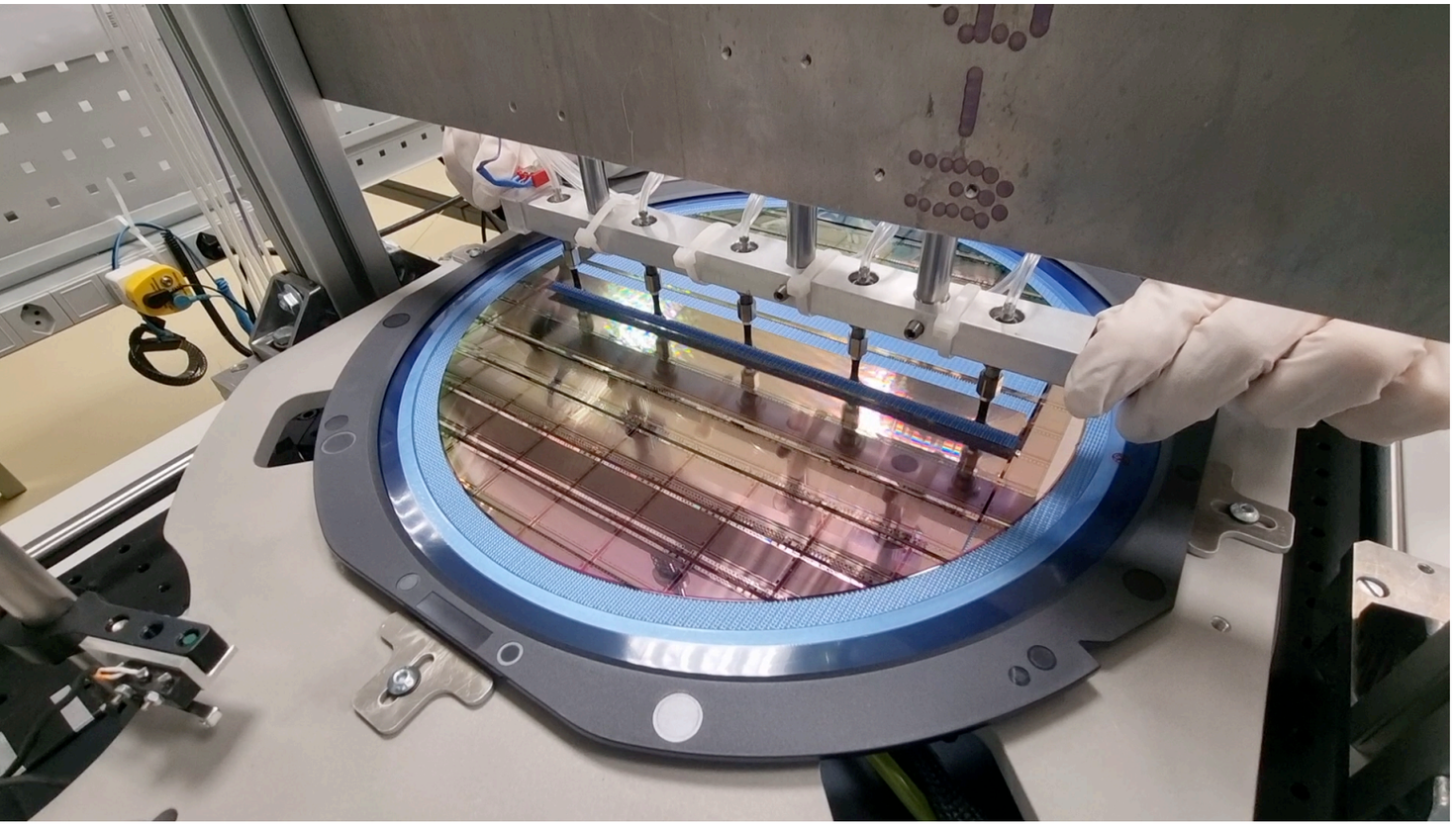

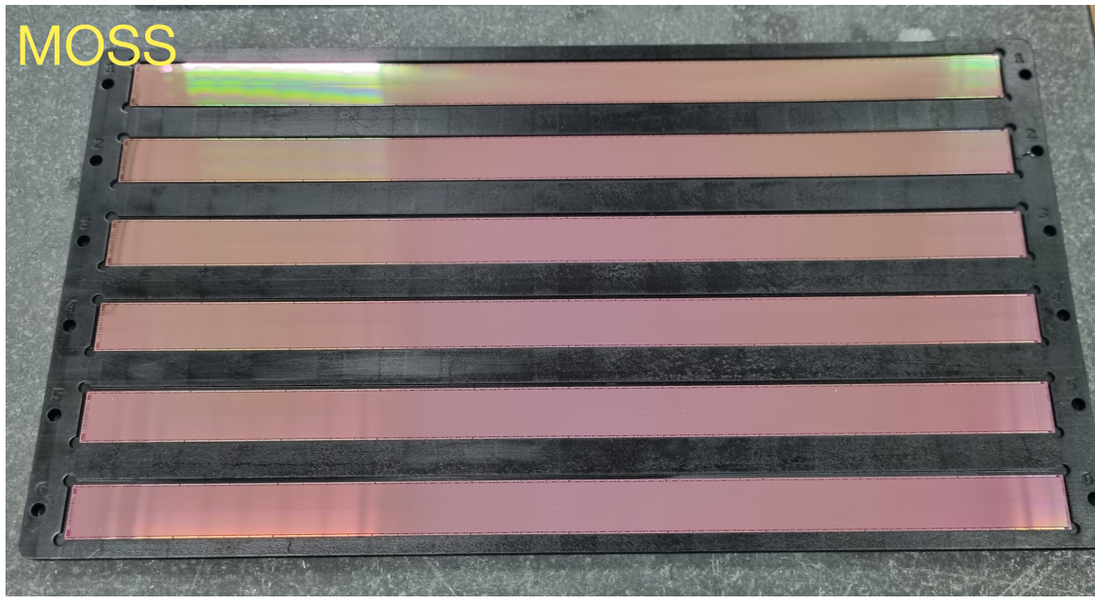

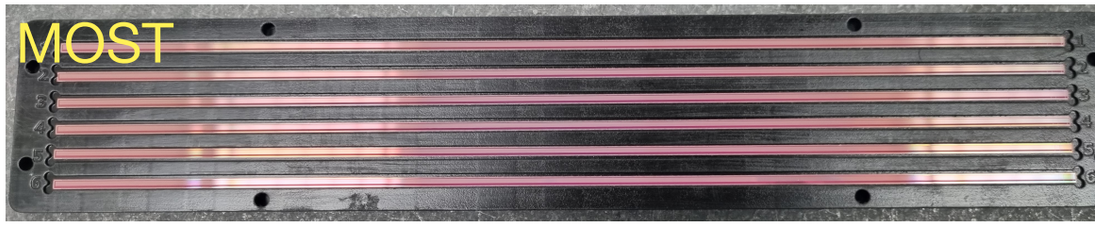

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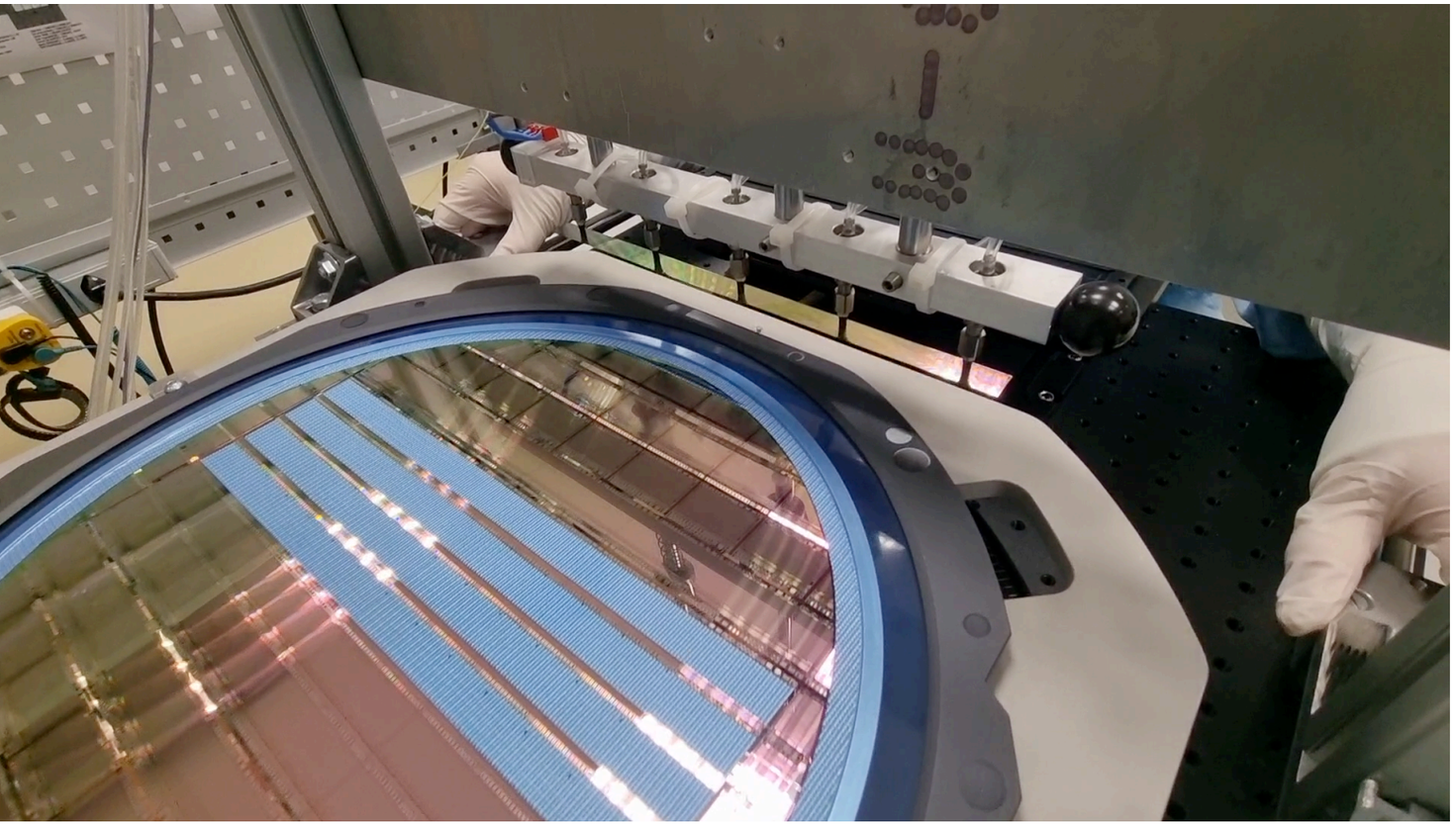

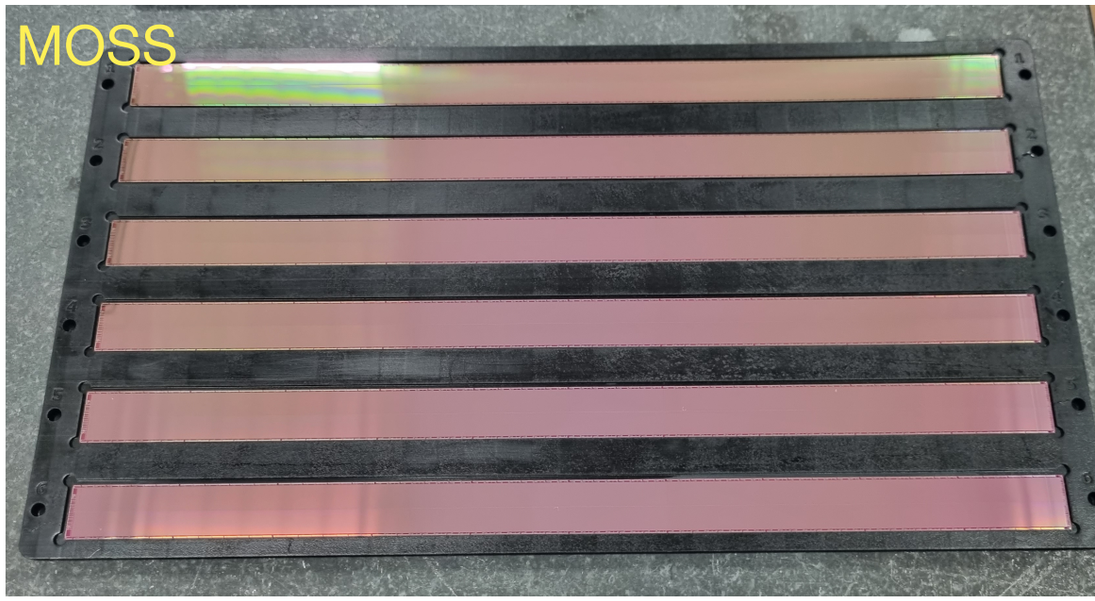

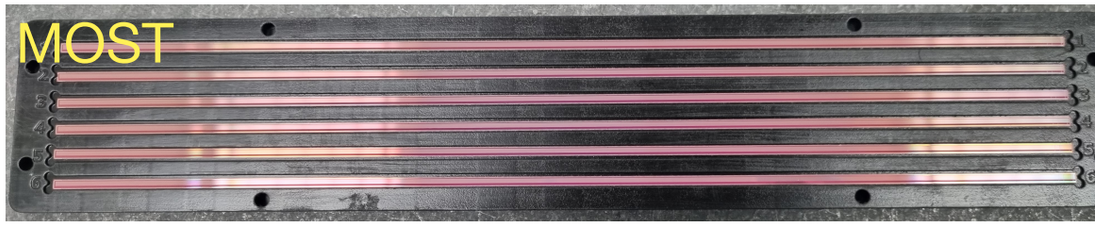

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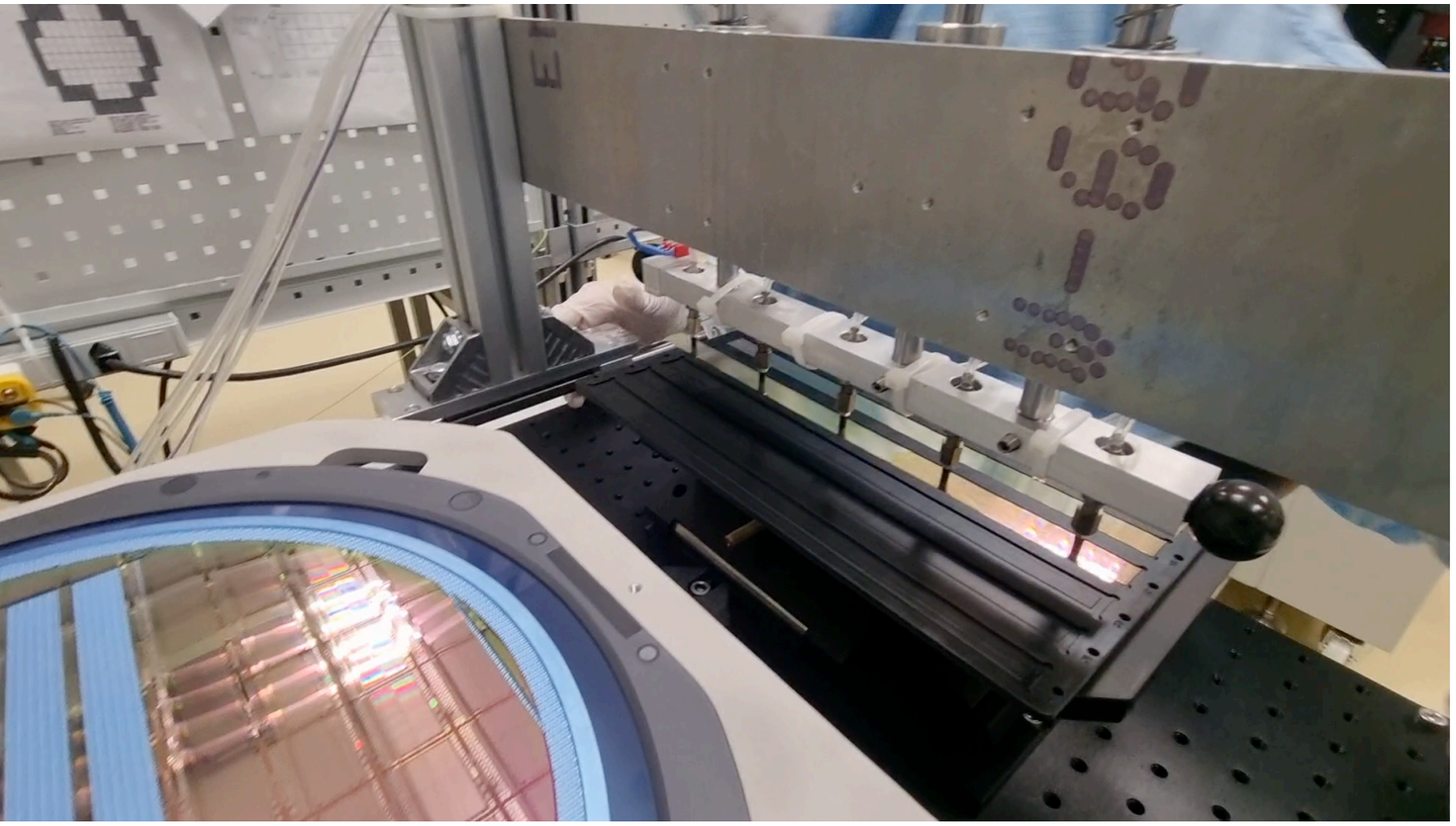

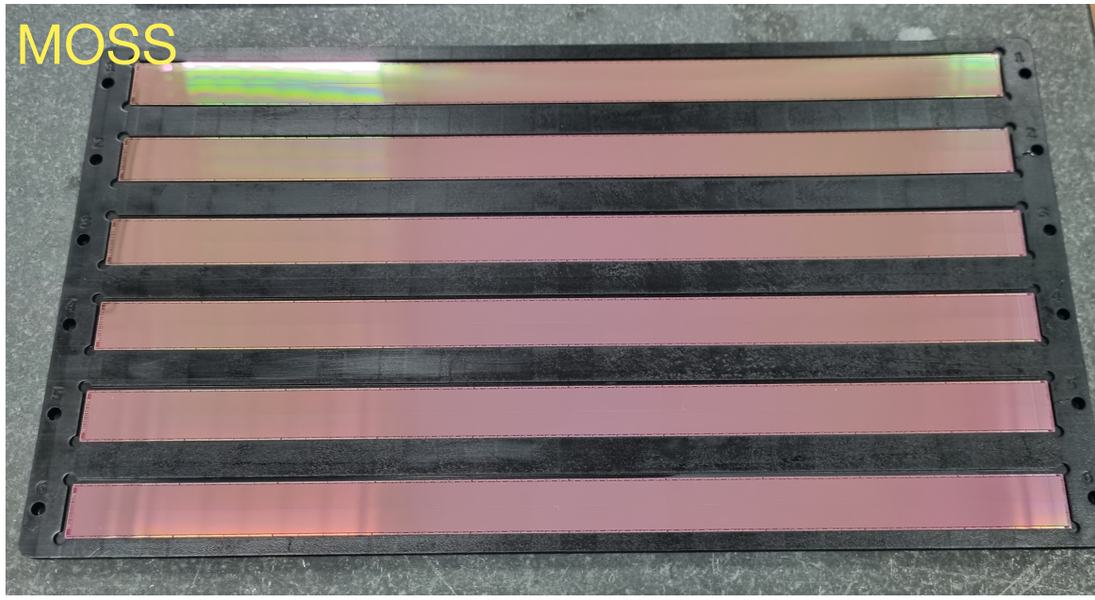

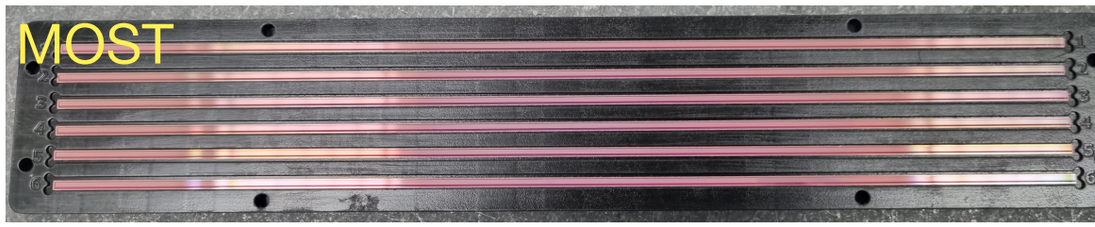

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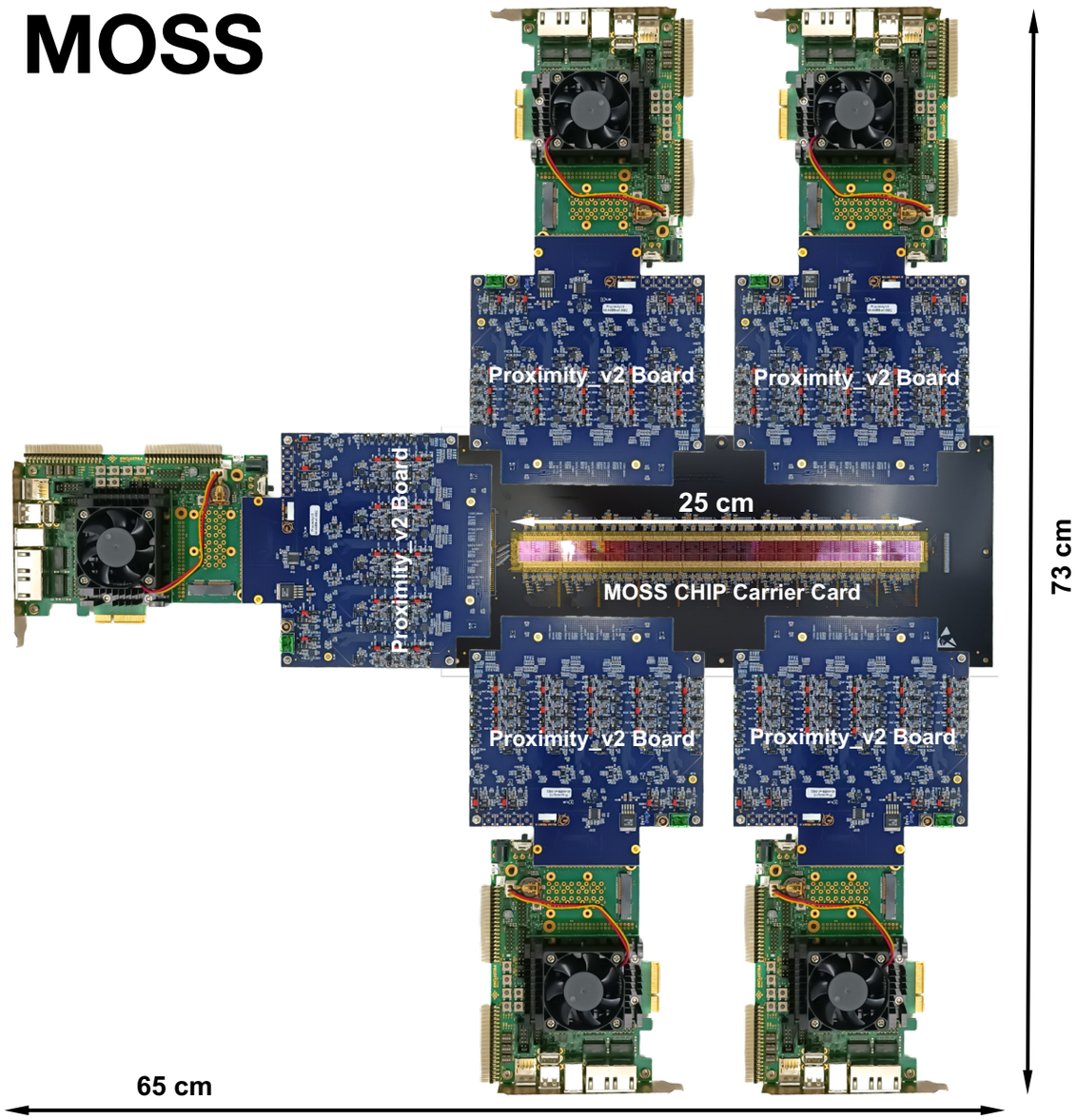
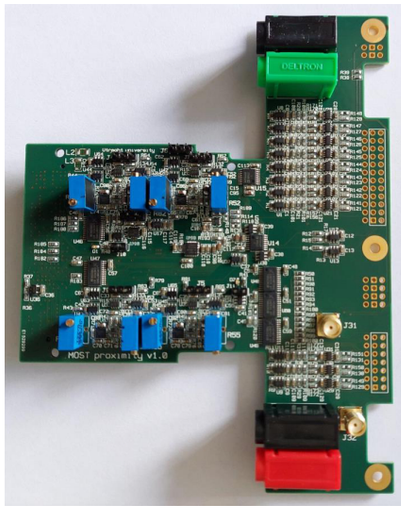
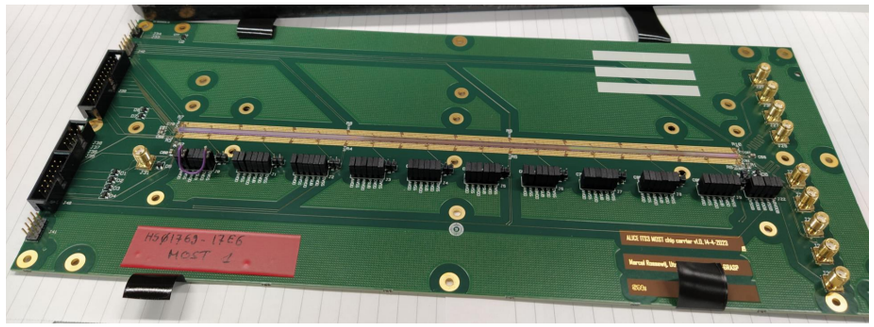
ER1 test systems

MOSS



MOST





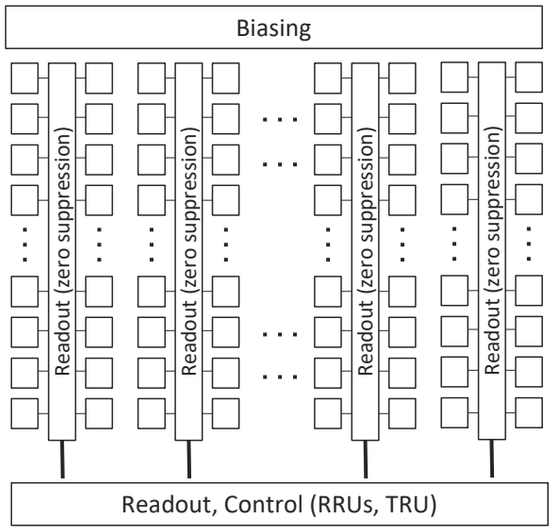
+ same FPGA board (x1) as MOSS

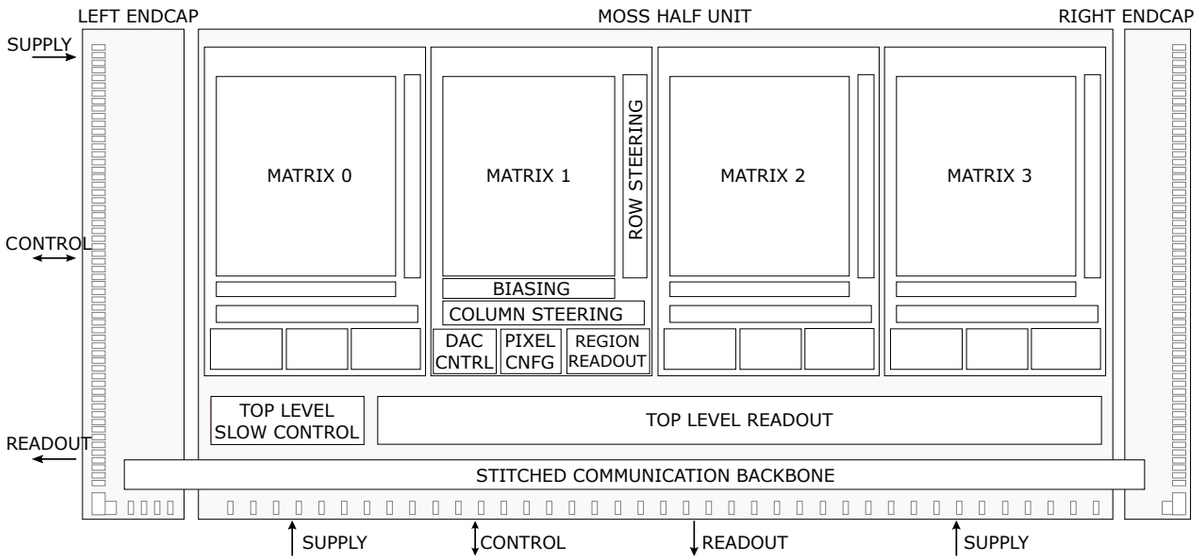
+ oscilloscope for readout

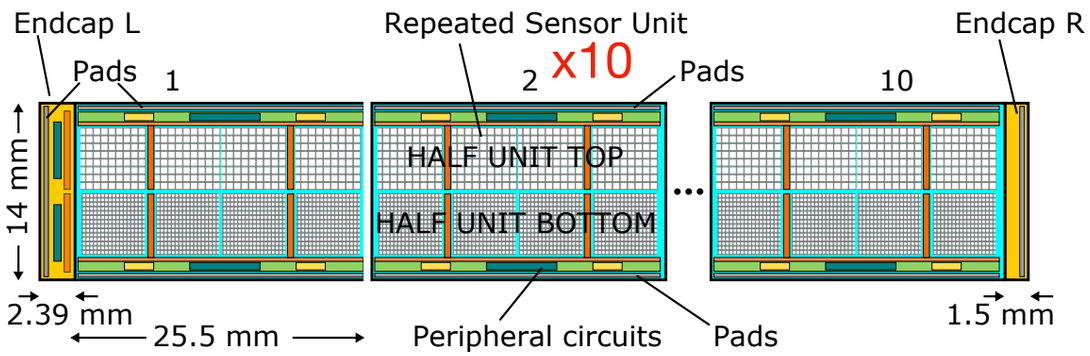
Test system scale in size as the sensors do

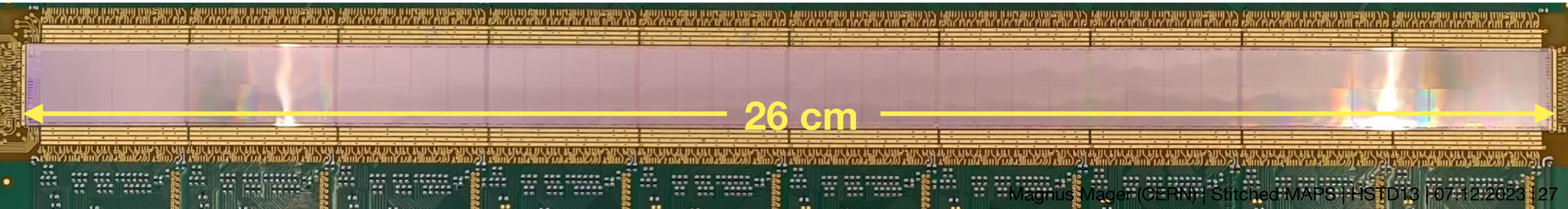
Prototypes: MOSS
design (1/2)

- MOSS is segmented into:
  - 10 repeated sensor units (RSU)
  - top and bottom halves with different pitches (22.5 and 18μm)
  - four different sub-matrices each with different analog designs
- Each half RSU is powered and can be tested independently
  - goal: understanding of yields and possible defects
  - difficulty: large number of power domains
- Stitched “back-bone” allows to control and readout the sensor from the left short side

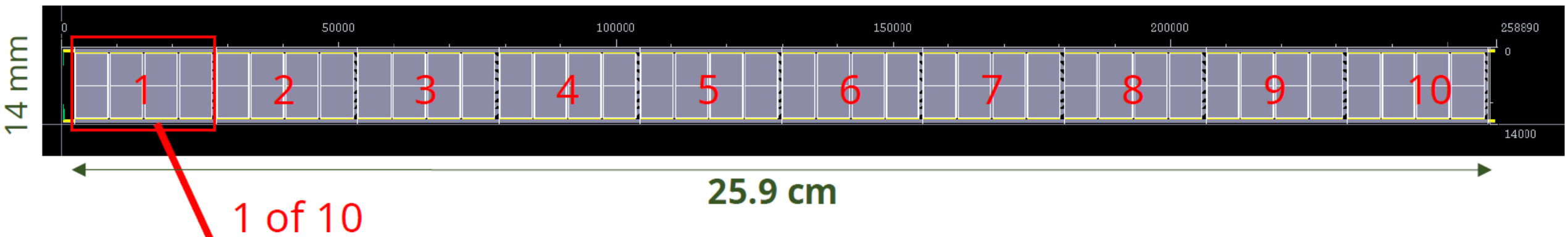




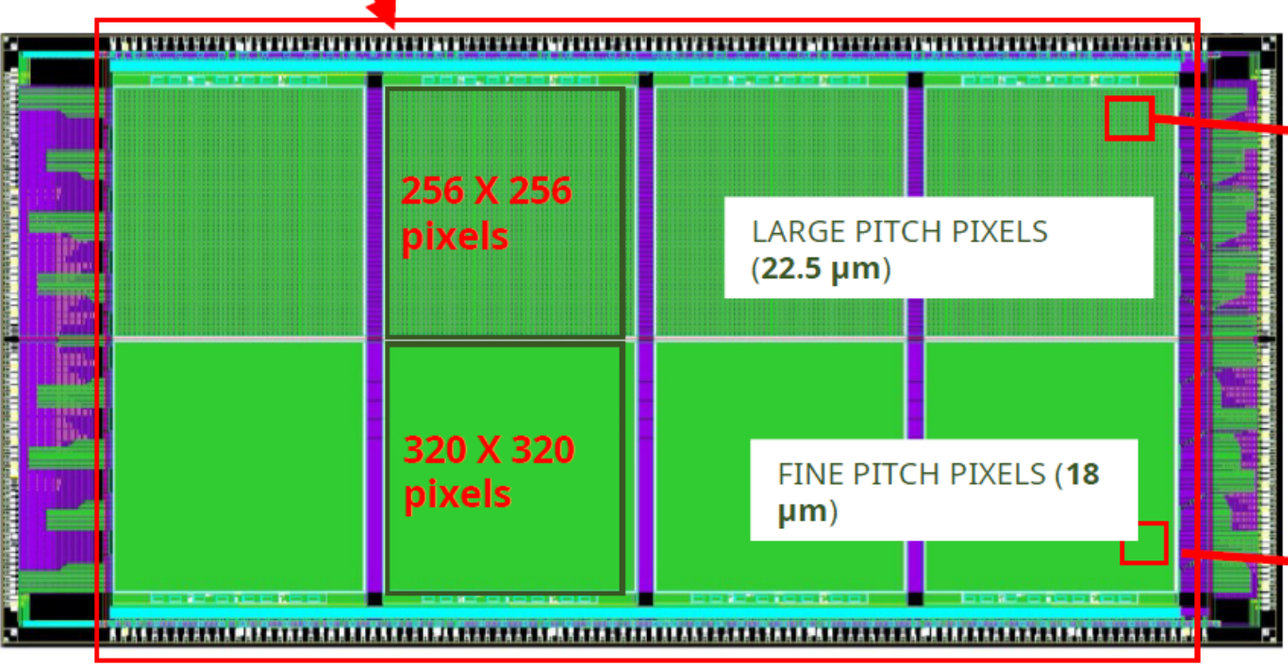


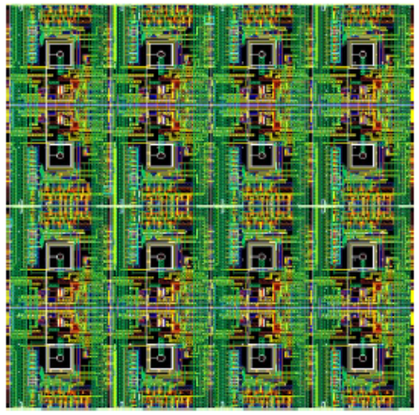


Prototypes: MOSS
design (2/2)

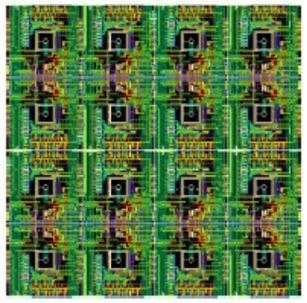


1 of 10





Pitch 22.5 µm
- Conservative layout
- 7 mW/cm2 (analog FE)
- 1us peaking time



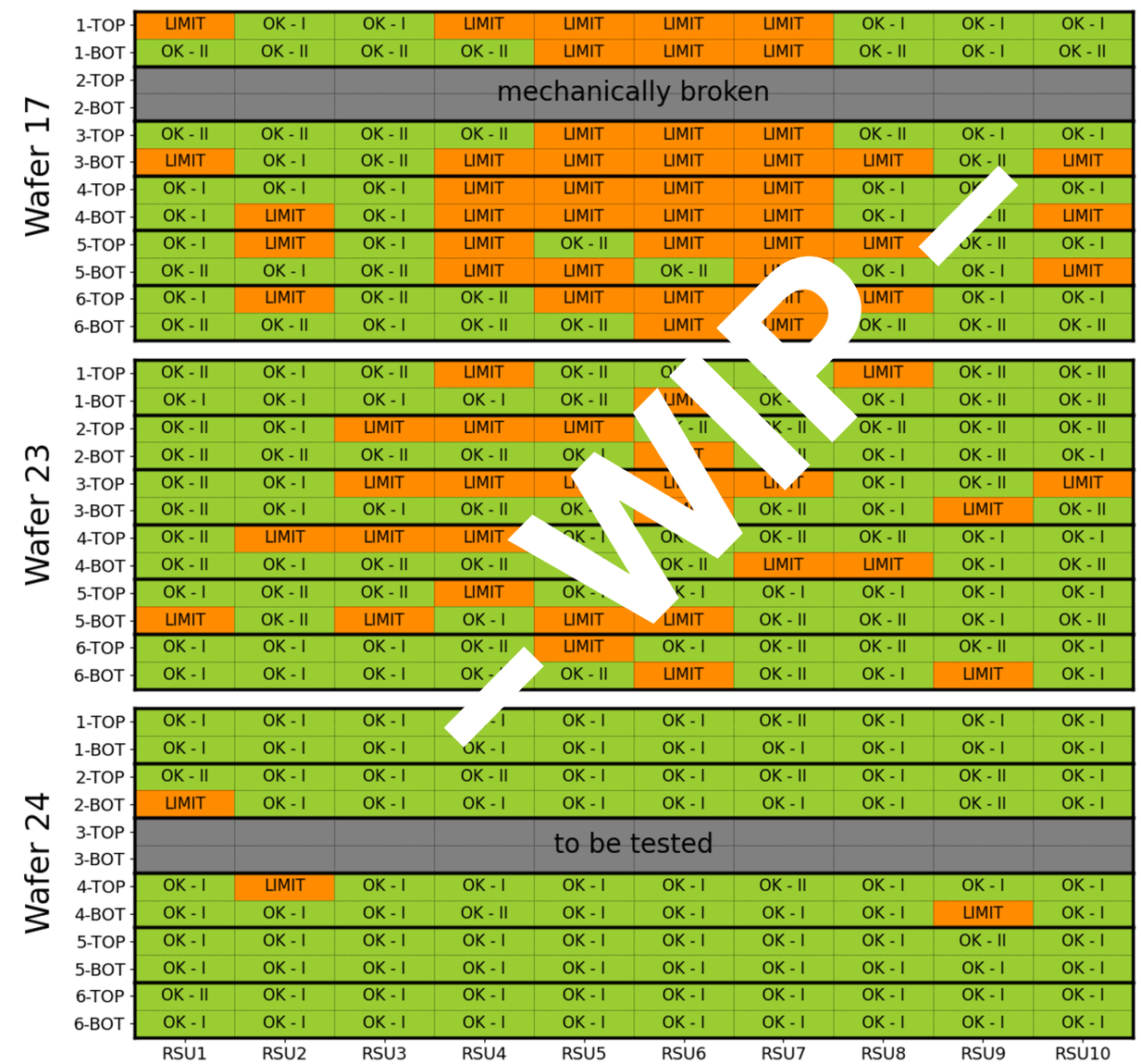
Pitch 18 µm
- Compact layout
- 11 mW/cm2 (analog FE)
- 1us peaking time

- 1.4 x 26 cm monolithic stitched sensor

MOSS lab testing

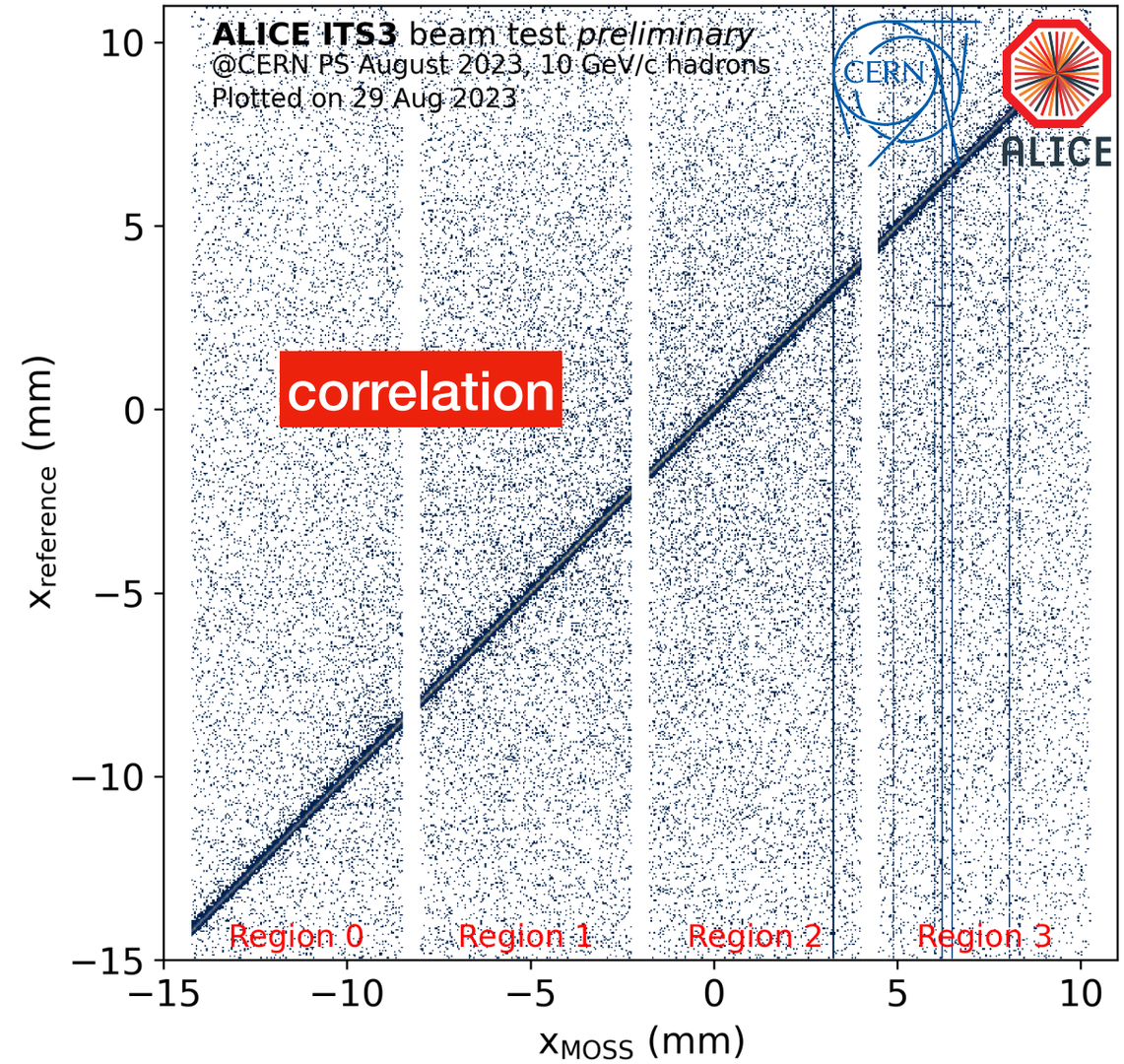
power tests

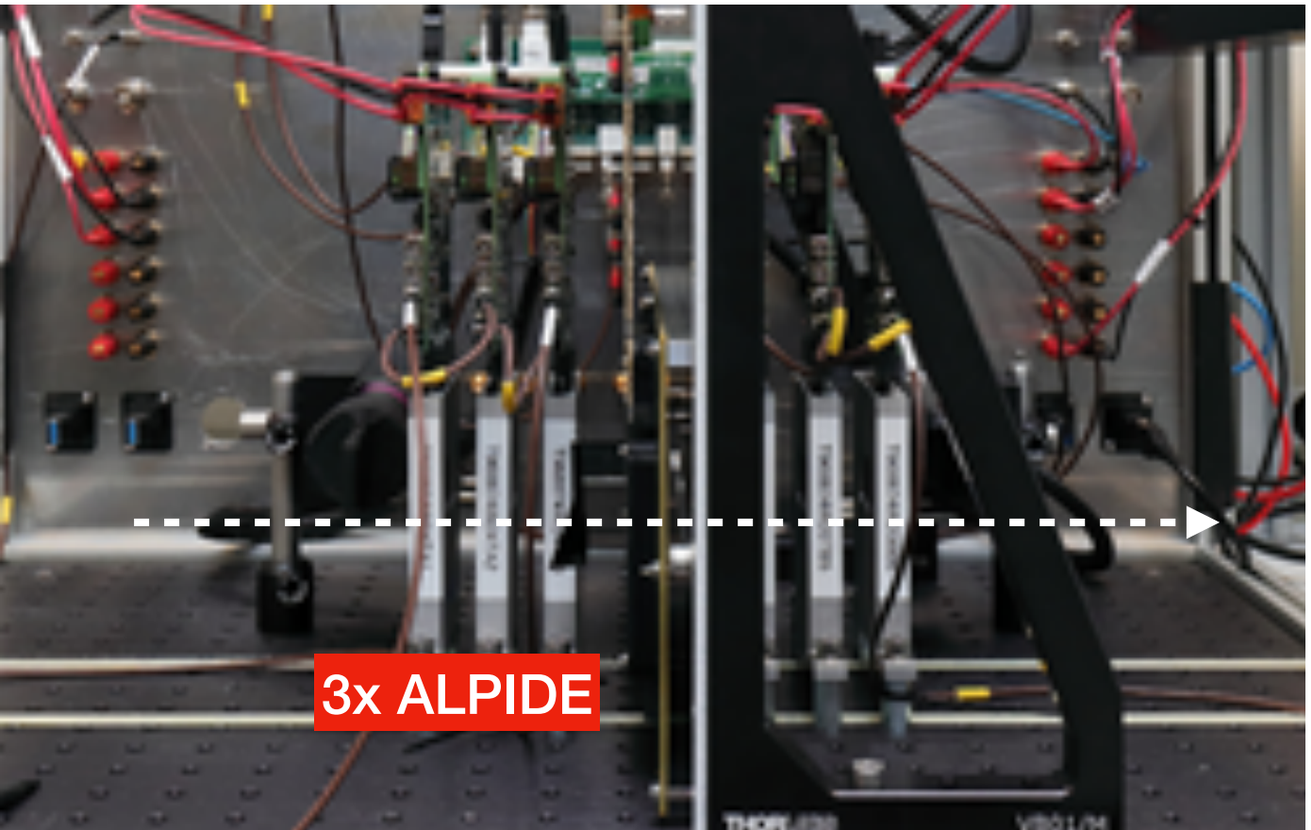
- Powering up the large chip is not easy
  - some important learnings were made here for the next chip iteration (ER2)
- Current results are based on a very gentle and careful powering
  - “you cannot repeat the first power up”
  - subsequently allowing larger margins continues to increase the “yield”
- A large wafer-wafer spread is observed
  - compatible with first findings from the second prototype (MOST)
- “Powerable” units are also functionally working (slow control)

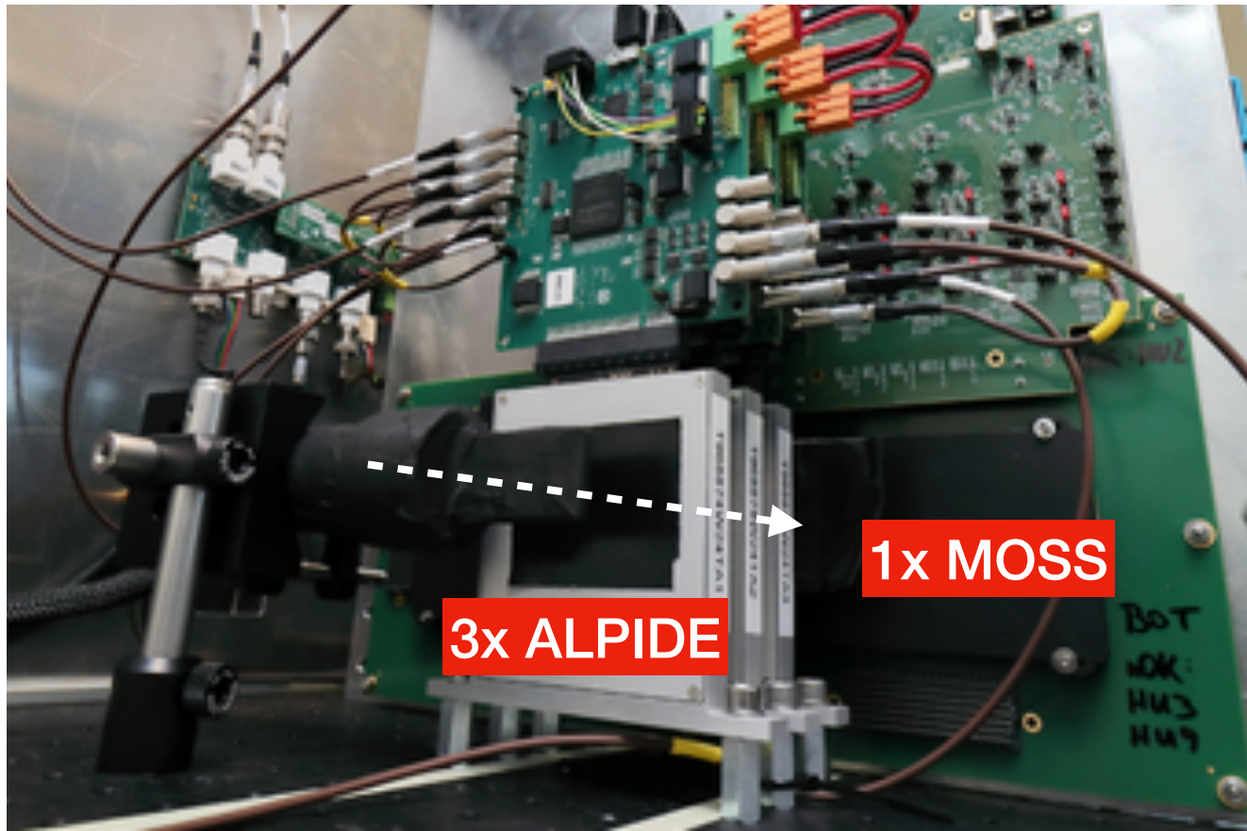


MOSS test beams

- Several campaigns in 2023
- Works out of the box
- Parameters still to be optimised and data to be analysed in more detail
- But very encouraging result!

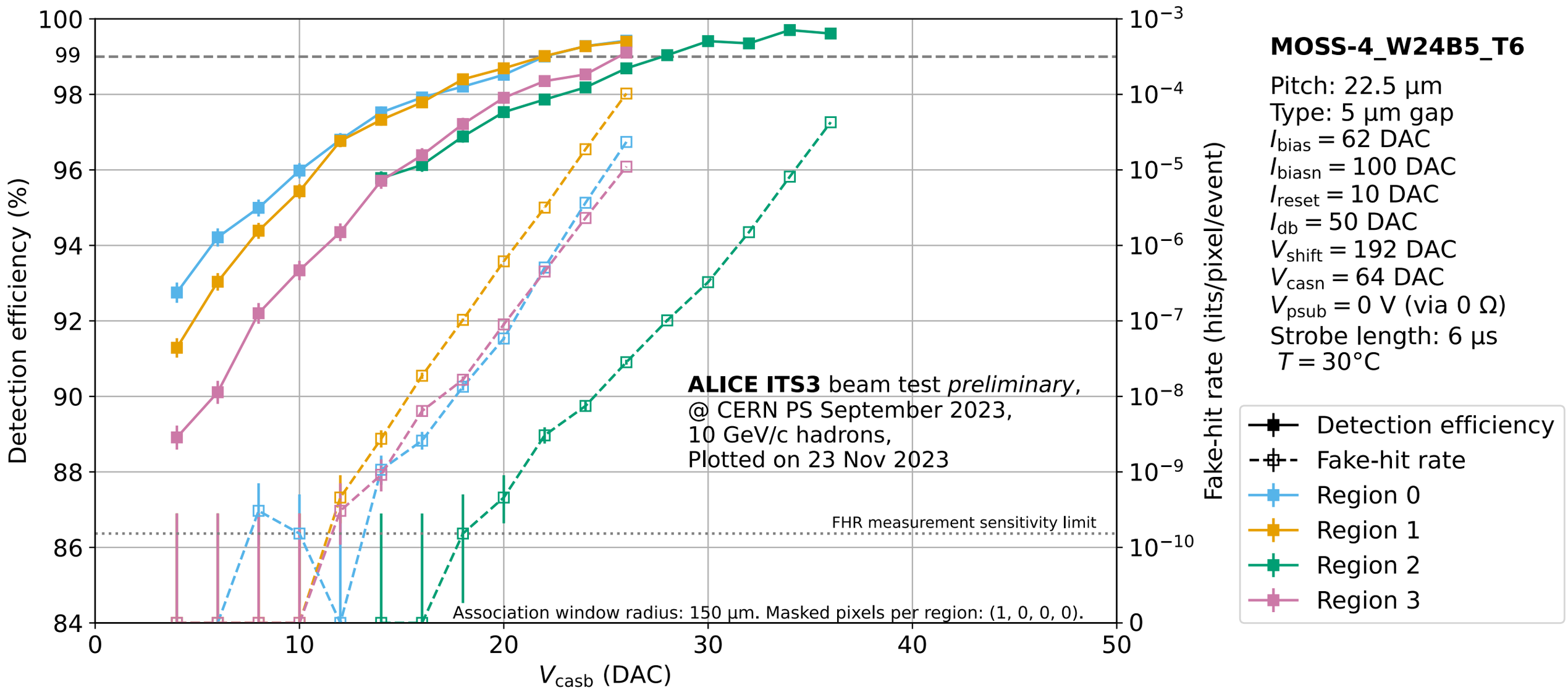






MOSS test beams

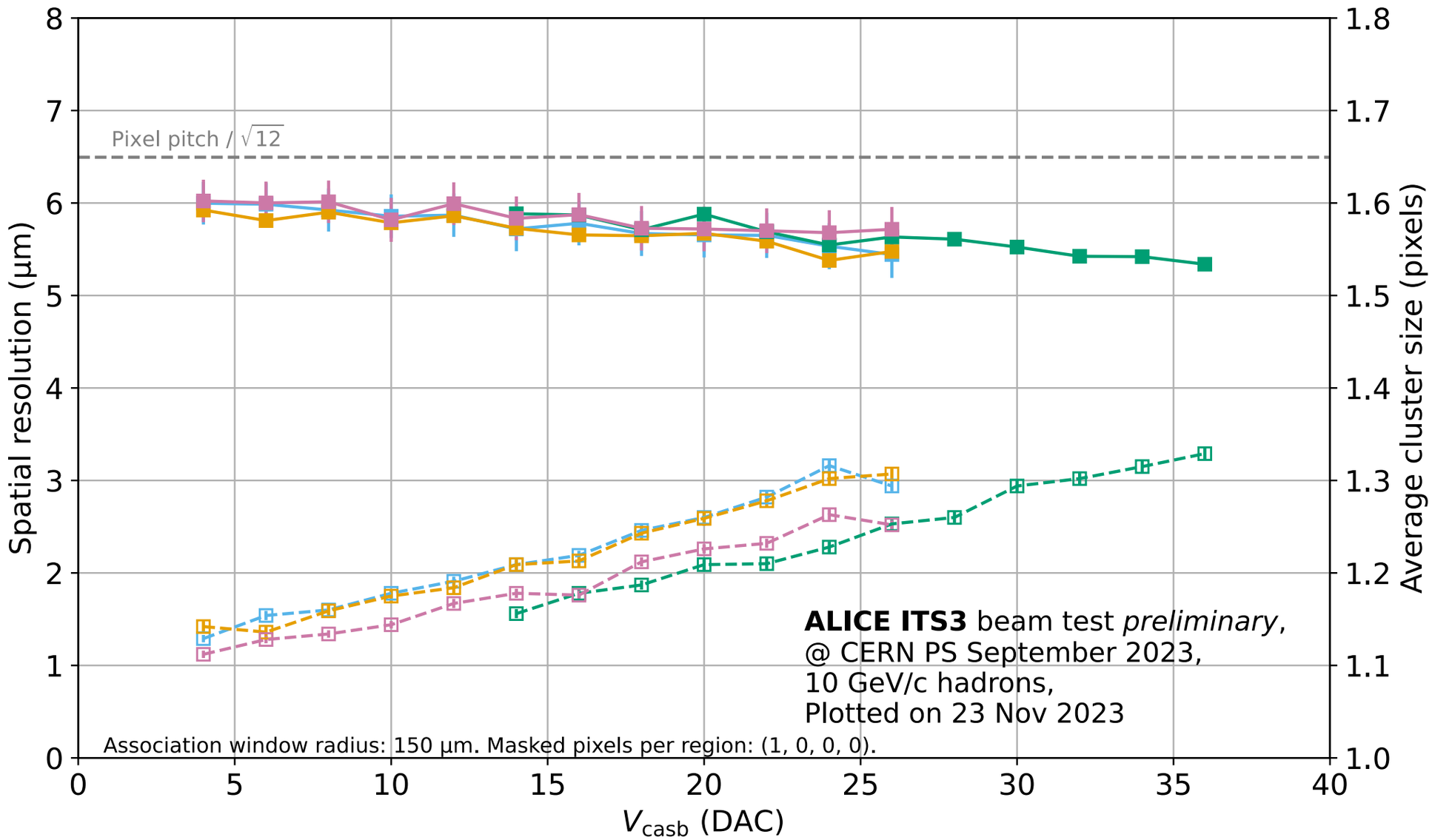
Detection efficiencies and fake-hit rates



Operational with a bit of margin — NB: bias settings are still being optimised

MOSS test beams

spatial resolutions and cluster sizes



MOSS-4_W24B5_T6

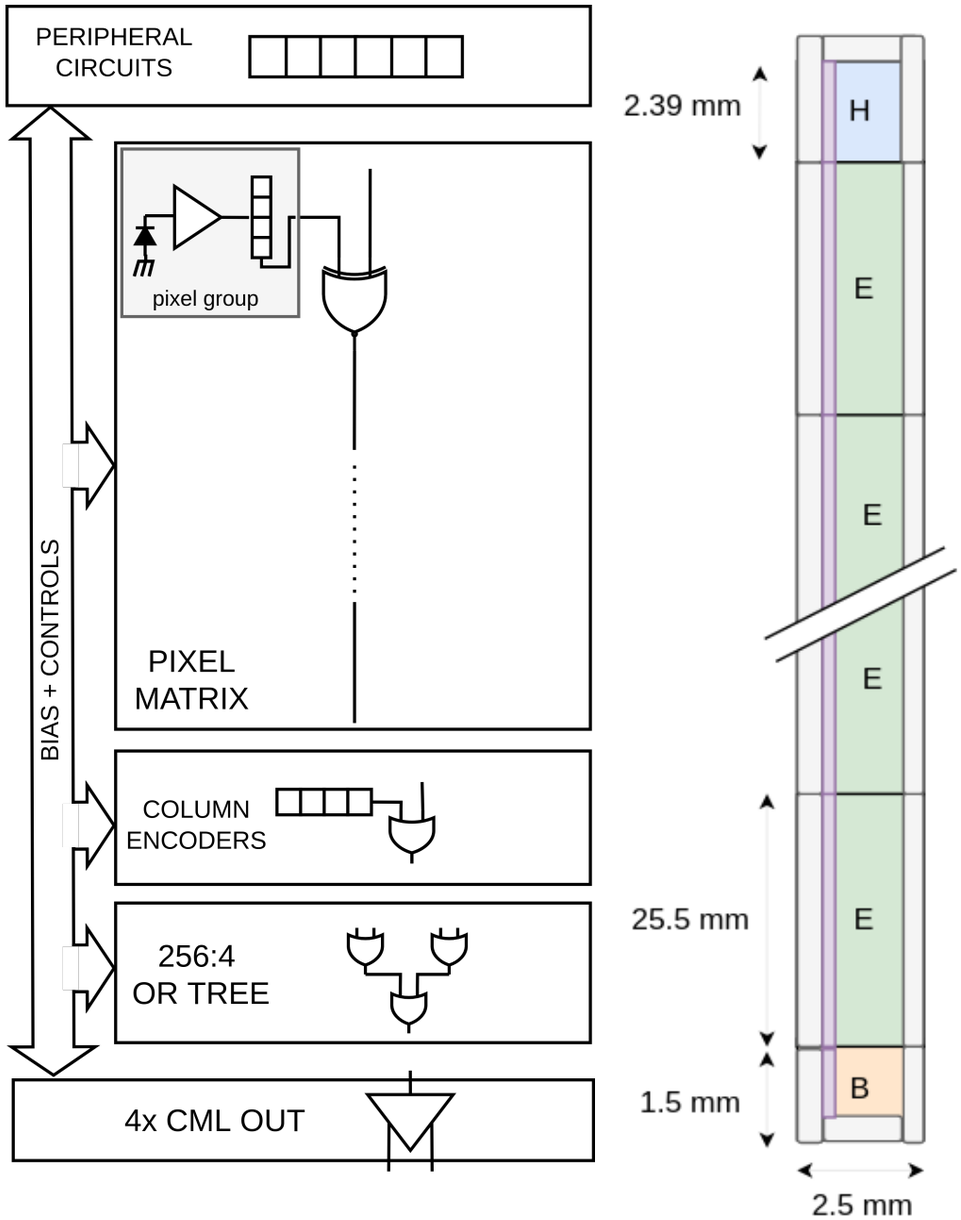
Pitch: 22.5 µm
Type: 5 µm gap
$I_{bias} = 62$ DAC
$I_{biasn} = 100$ DAC
$I_{reset} = 10$ DAC
$I_{db} = 50$ DAC
$V_{shift} = 192$ DAC
$V_{casn} = 64$ DAC
$V_{psub} = 0$ V (via 0 Ω)
Strobe length: 6 µs
$T = 30°C$

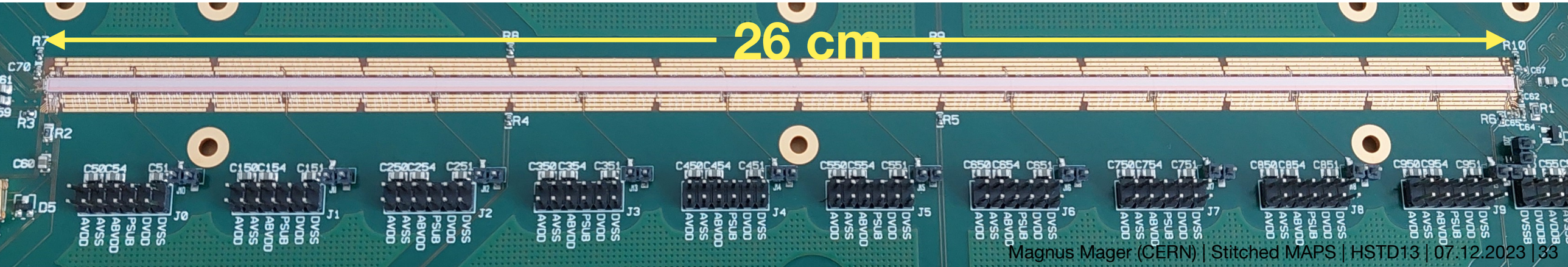
- Spatial resolution
- Average cluster size
- Region 0
- Region 1
- Region 2
- Region 3

Spatial resolutions and cluster sizes match those of small prototypes

Prototypes: MOST
design (1/2)

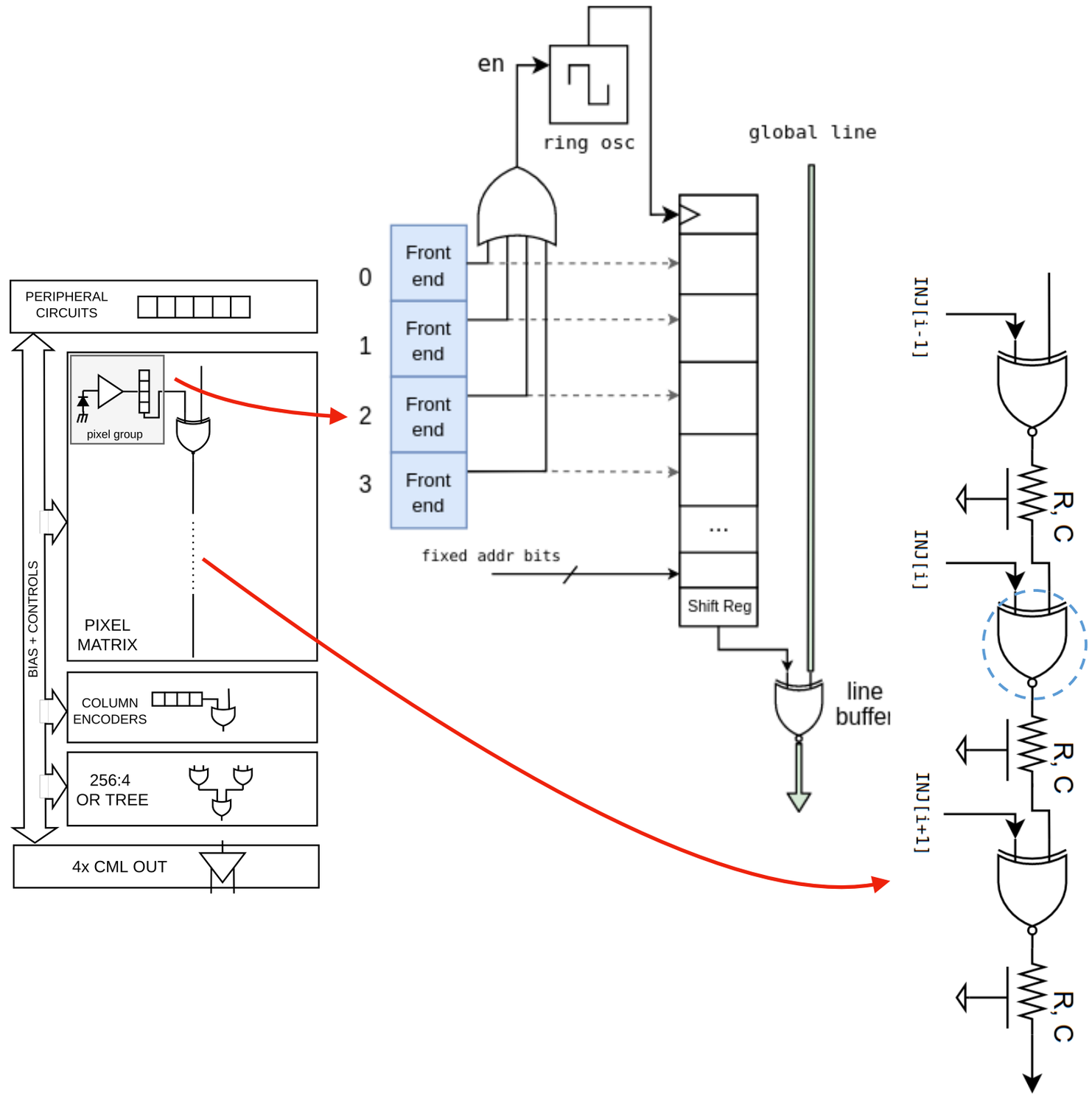
- MOST is based on a very densely integrated pixel matrix
- Power is distributed globally
  - yield is addressed by a highly granular set of switches that allow to turn off faulty parts locally
- Readout is purely asynchronous and hit-driven
  - low power consumption + timing information





Prototypes: MOST
design (2/2)

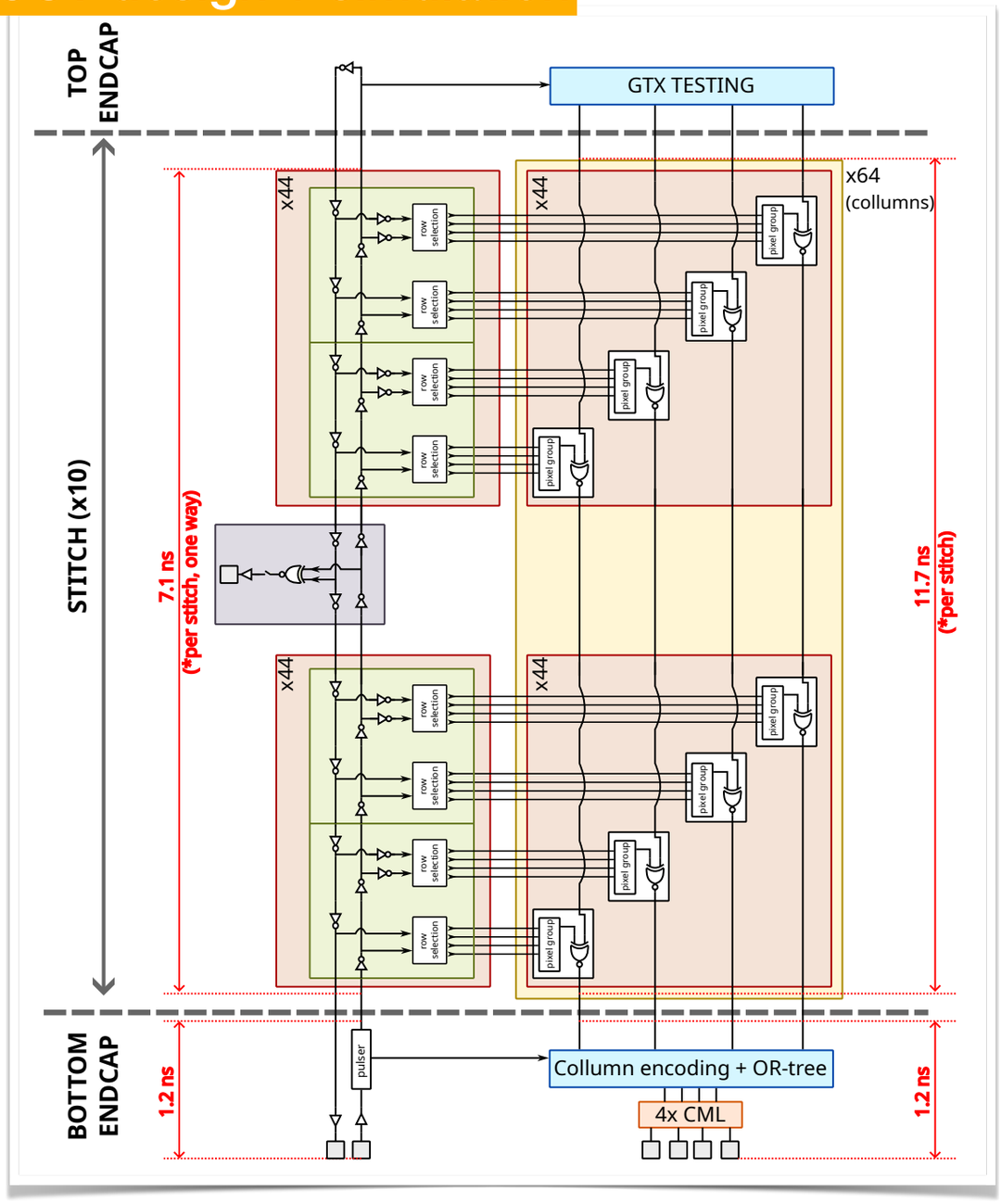
- Each set of 4 pixels contains a local oscillator and address serialiser
  - only active when a hit is detected
- Signal is buffered several times along chip
- Sharing of the same transmission channels along a column



Digital pulsing & readout
concept

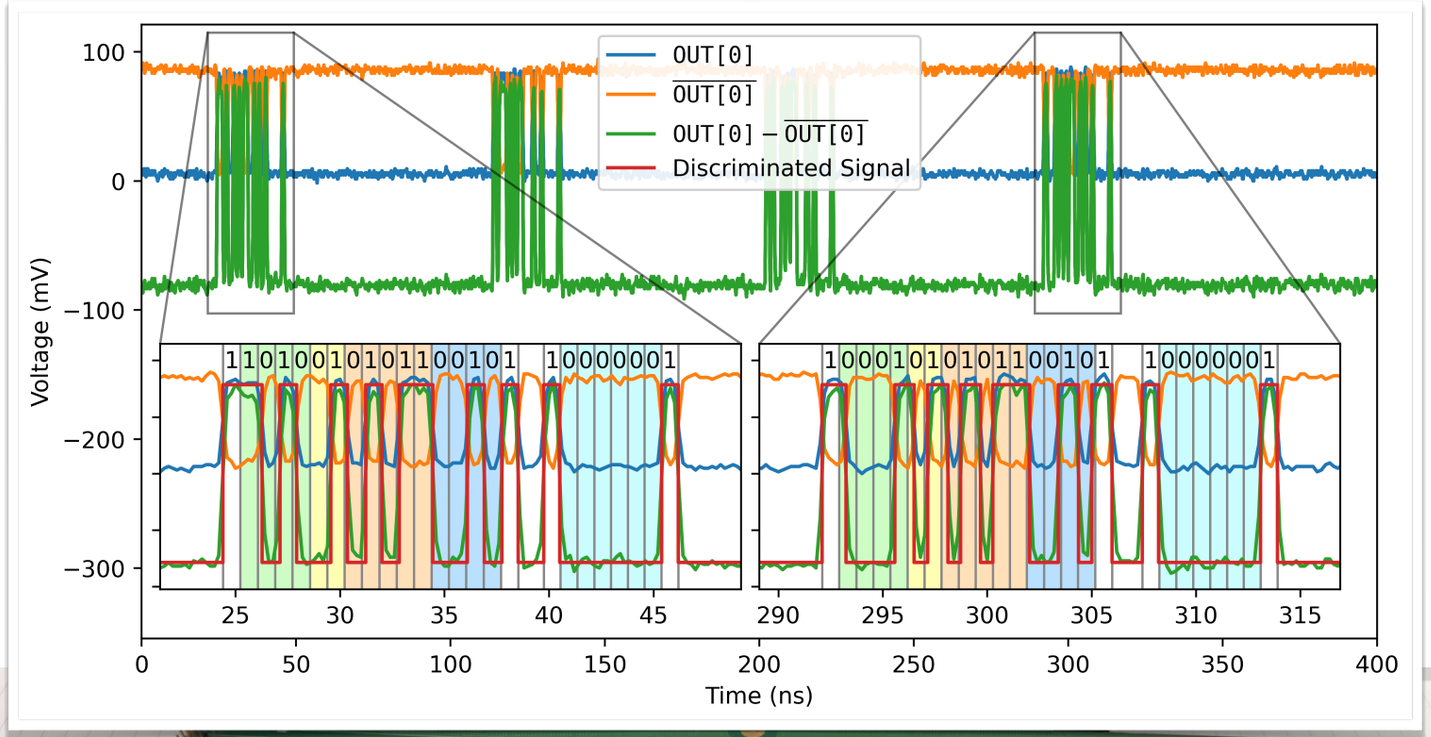
- A test pulse can be fed at the bottom
  - travels across the full chip to the top
  - and then back
- Fired pixels send their address to the bottom
  - as serial bitstream of **~1Gbit/s**
  - there are 256 of these lines on MOST (4 per column)
- Total round trip is expected to be of **O(200 ns)** for the top most stitch
- Pulsing and readout signal each go via up to **880 repeaters over 26 cm**

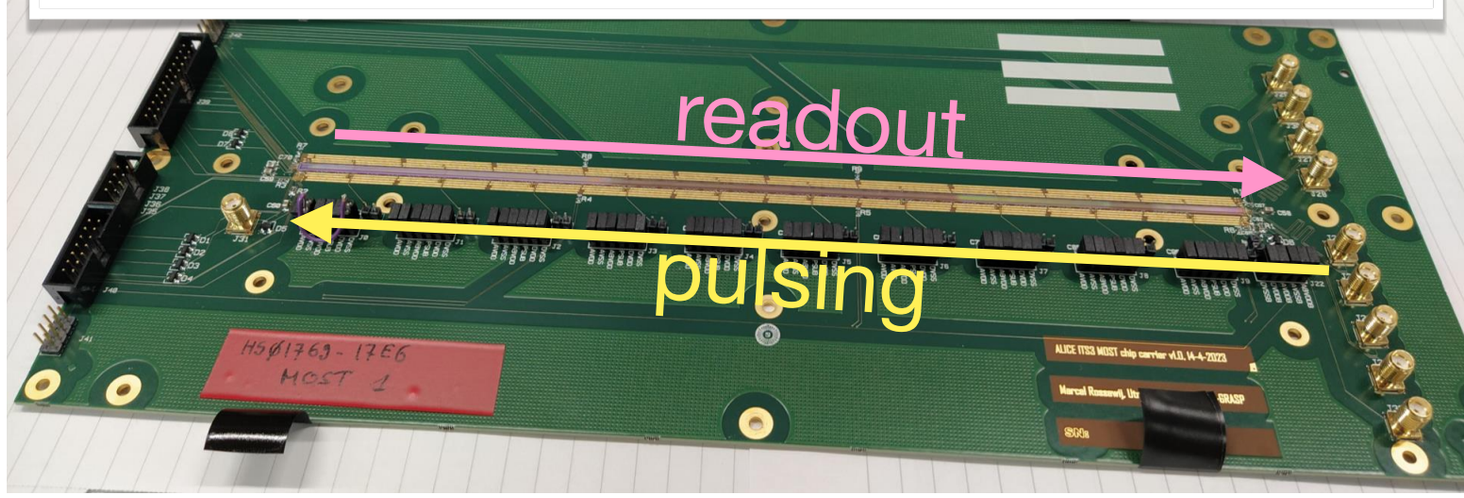
MOST design + simulation



Pulsing & readout
measurement

- All 256 readout lines work across the full length of the chip/across all stitches
- Decoding of pixel addresses work nicely
- Tests of the analog front-ends are starting (they are alive, stay tuned for more soon)





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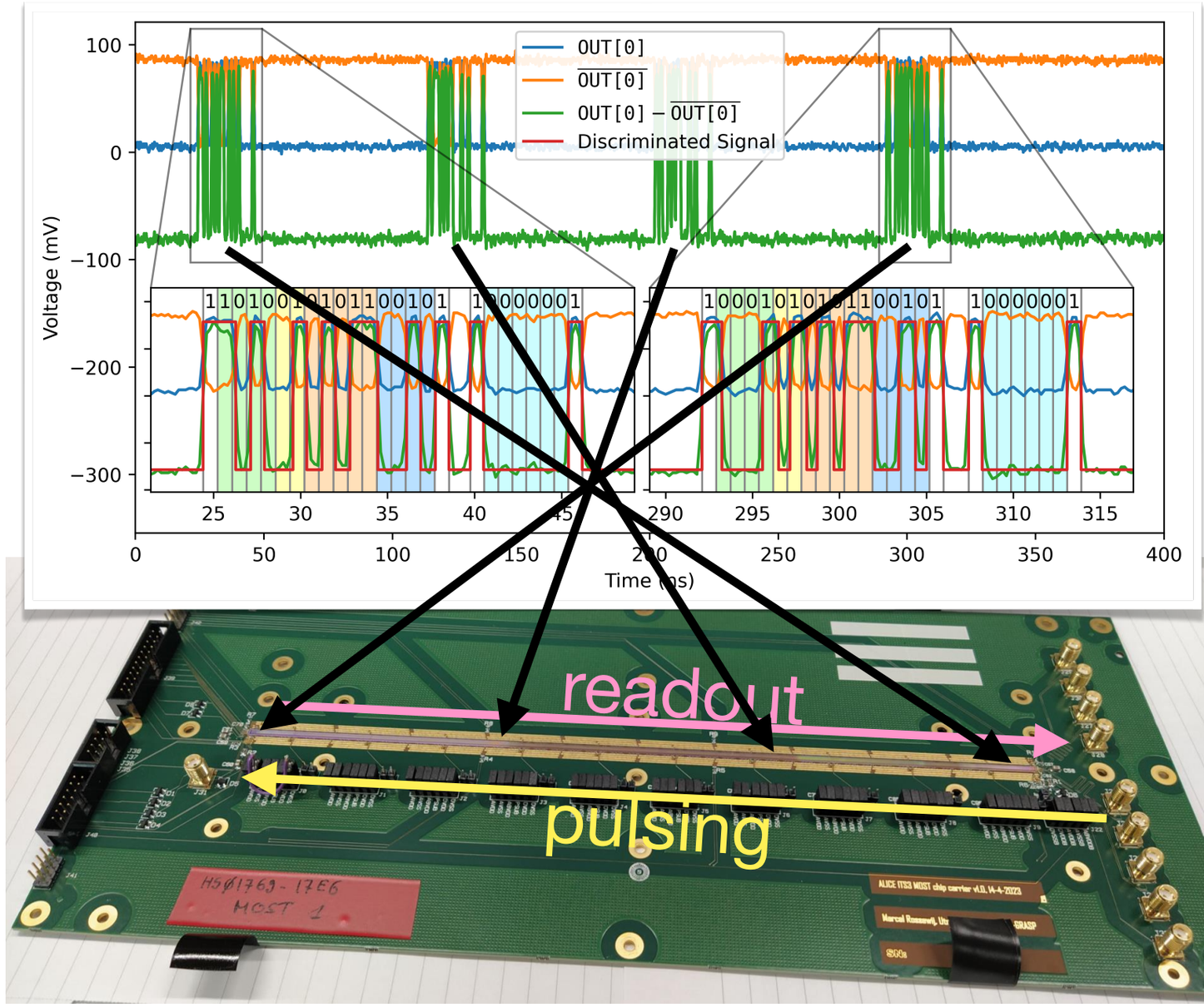
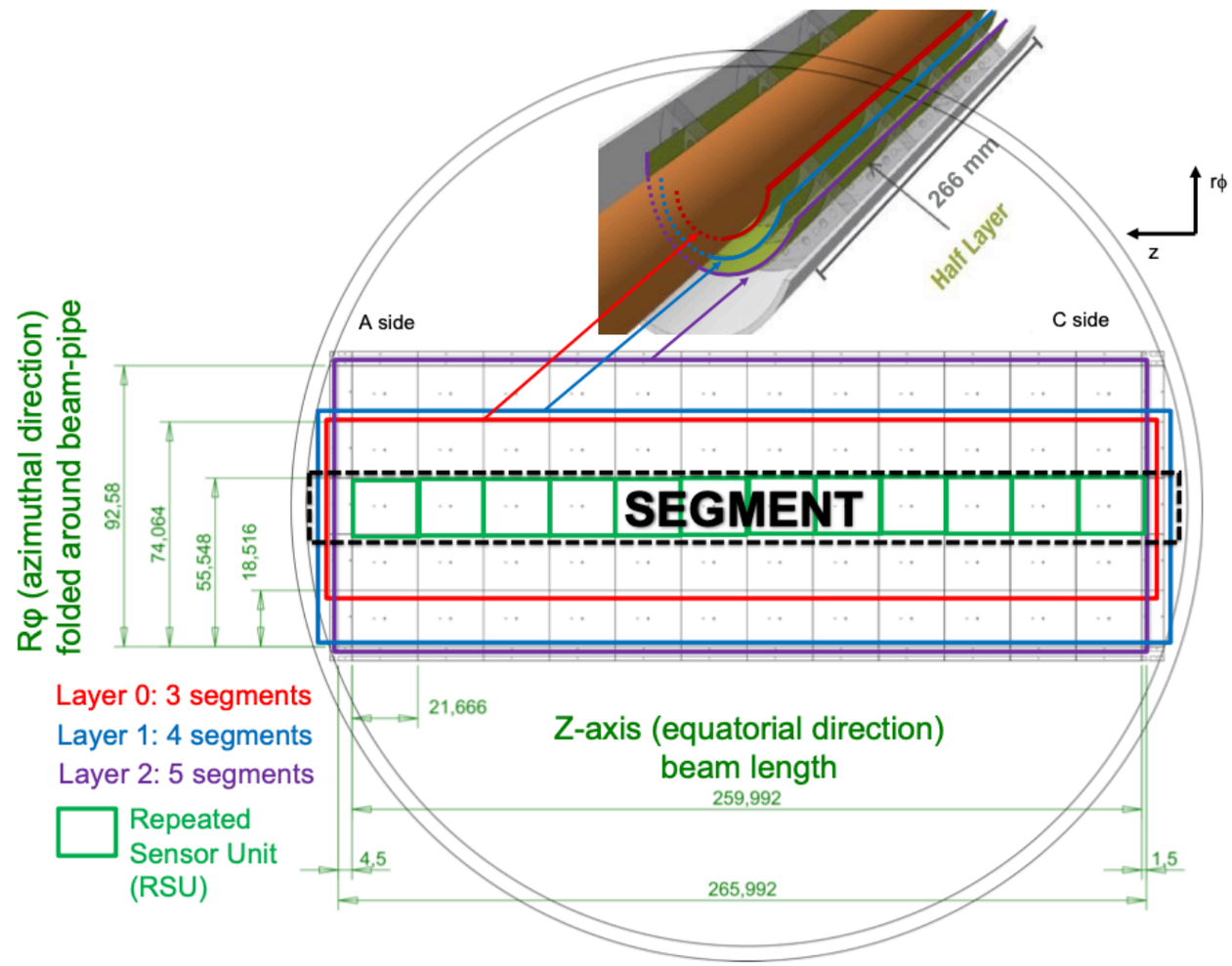


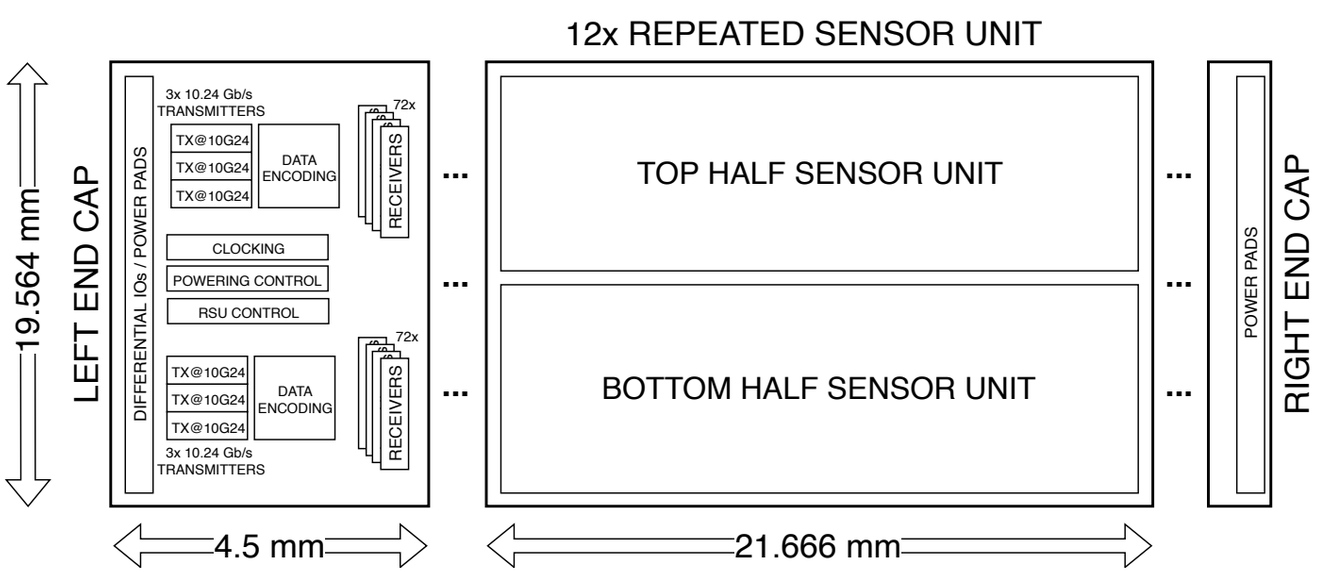
Next steps
MOSAIX (ER2) (1/2)

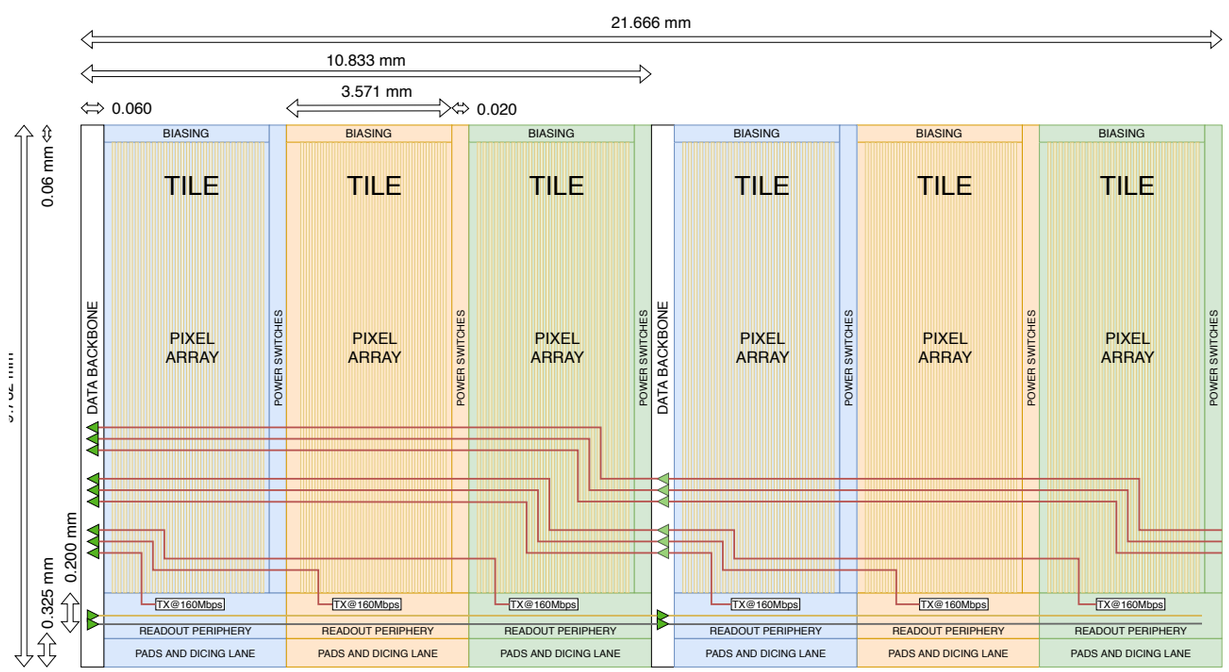
- "**MOSAIX**" is being designed
  - a real sensor with all functionality
  - to be used in an experiment (ALICE ITS3)
- Learnings from MOSS and MOST on stitching are folded into the design
  - powering granularity has been adjusted: 20→144 per segment
  - introduction of on-chip power swtiches
- Interfaces with off-detector electronics are incorporated
- New low-leakage standard cell library
- Stitching plan fixed and under review with foundry



Next steps
MOSAIX (ER2) (2/2)

- Left end cap circuit
  - like a separate “readout chip”
- 12 repeated units with 12 independent matrices each
- Design ongoing, plan to submit in fall 2024





Summary

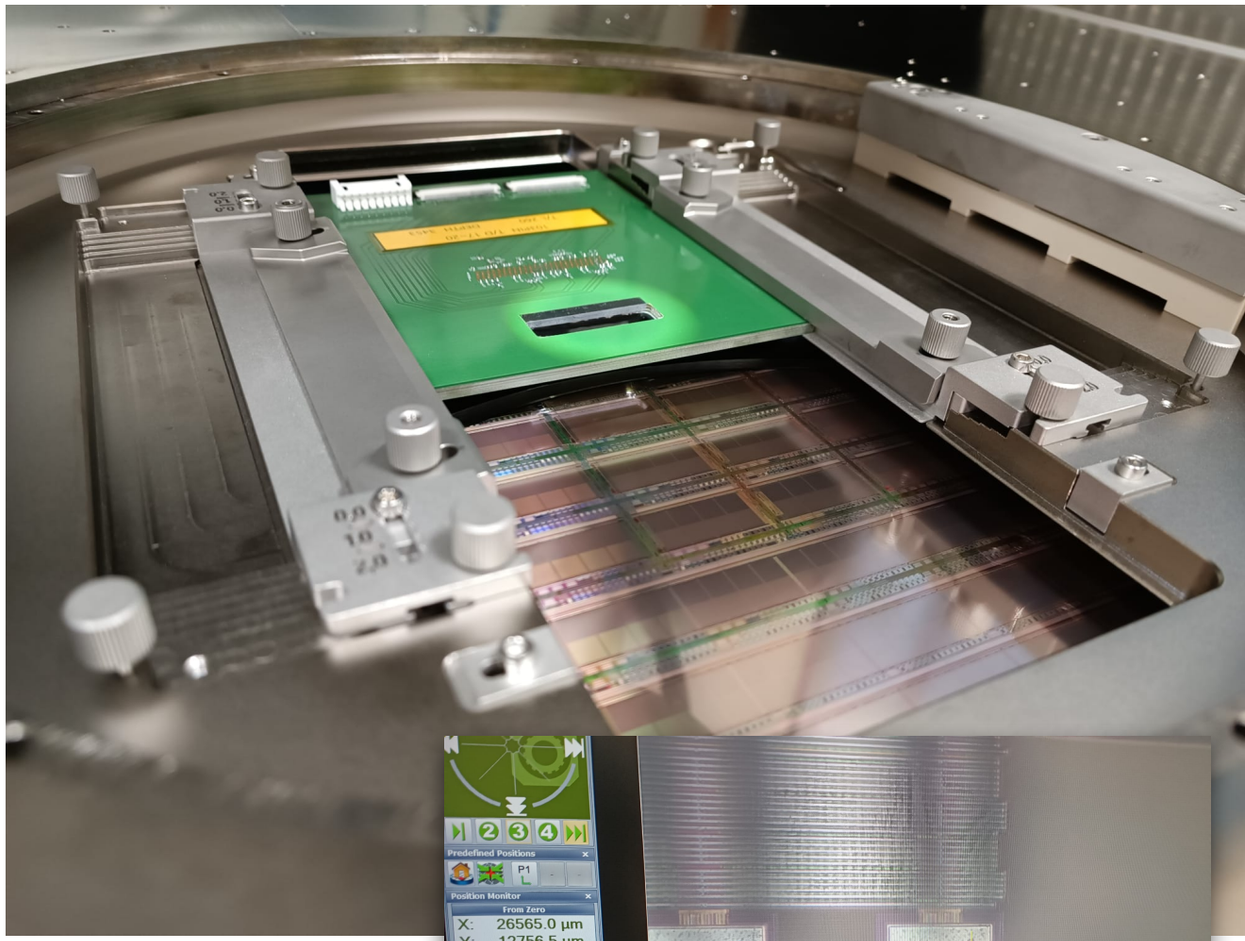
- **Stitched, wafer-scale MAPS** offer a unique possibility to build ultra-light, highly granular detectors
- **Bending** of 50 μm-thick chips and wafers is exercised routinely
- Two **key design challenges** are being dealt with:
  - power
  - yield
- Two 26 cm long, stitched prototypes ("**MOSS**", "**MOST**") have been fabricated in a first engineering rung ("ER1") in TPSCo 65 nm
  - both work!
  - detailed characterisation is ongoing
- Next step: integration of a sensor that can be used on a detector ("**MOSAIX**")
  - design is ongoing for submission in fall 2024

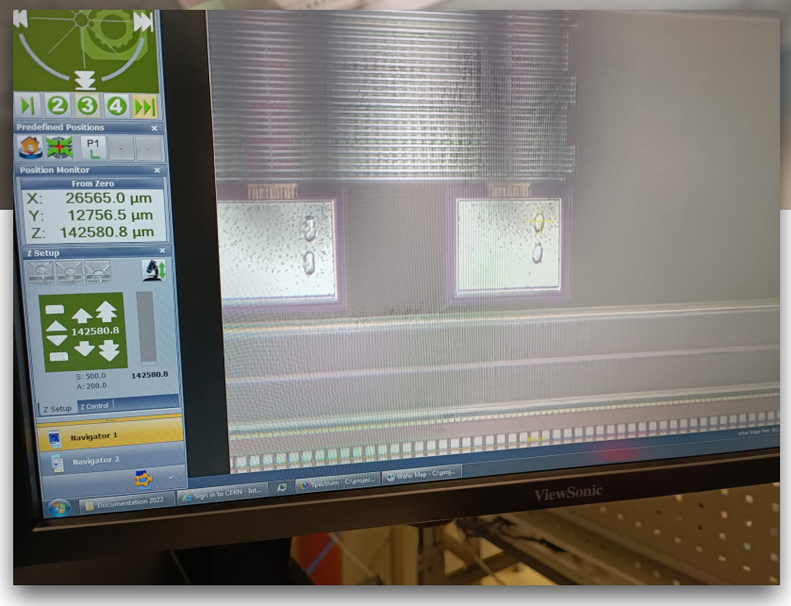
Thank you!

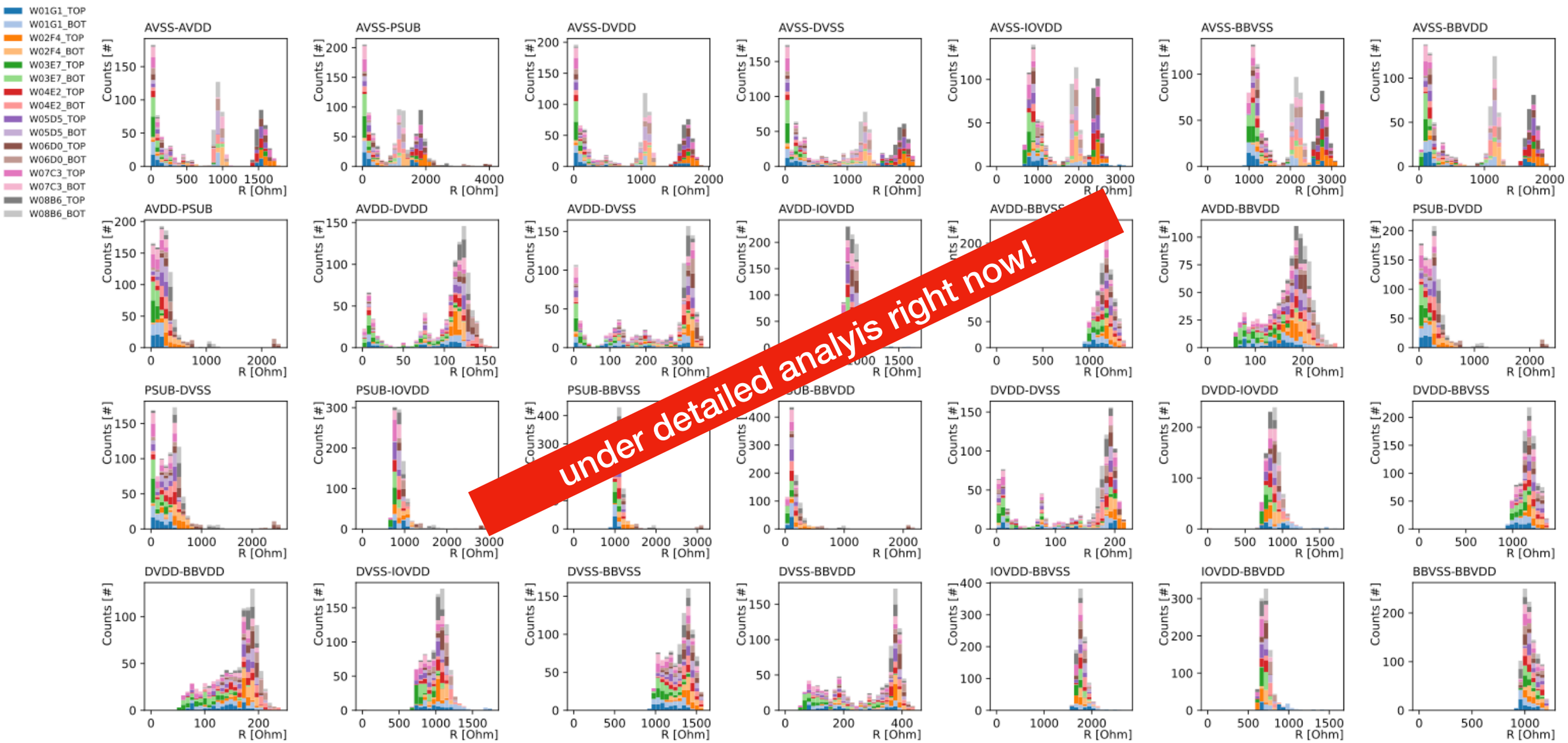
Supplemental material

MOSS probe testing
on wafer level

- Dedicated needle card for MOSS ready
- Compatible with test system for chips on carriers
  - first functional tests of MOSS were actually done using this needle card
- Systematic impedance tests carried out for 8 wafers





MOSS probe testing

Impedance measurements