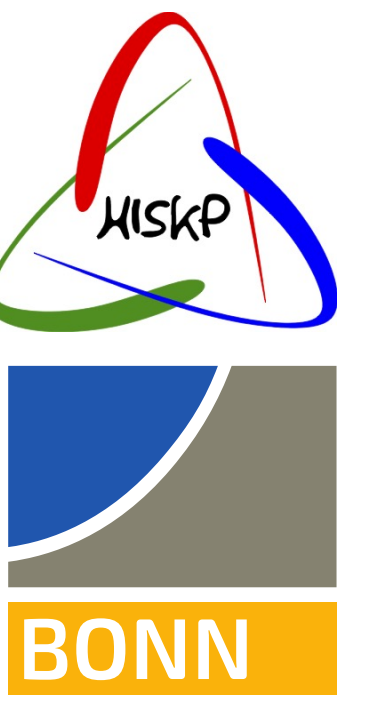


# Mighty Tracker

## Performance Studies of the MightyPix for LHCb

13th International "Hiroshima" Symposium on the Development & Application of Semiconductor Tracking Detectors



Hannah Schmitz, hannah.schmitz@cern.ch  
On behalf of the LHCb Collaboration

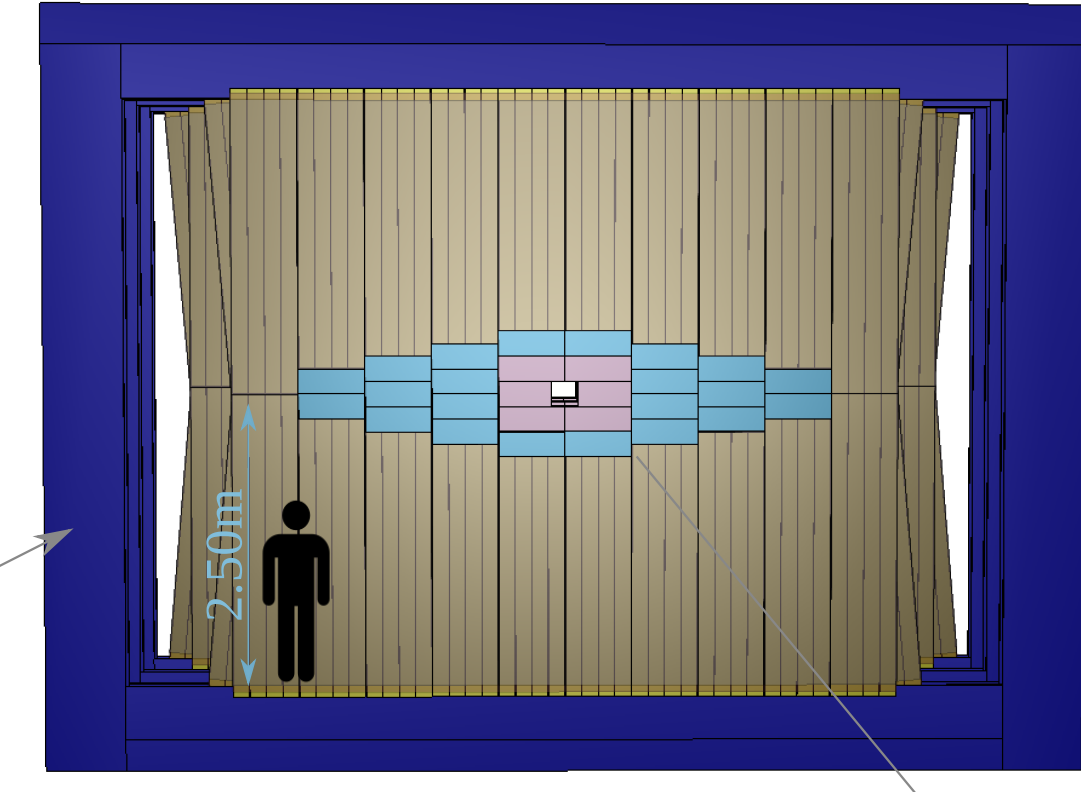
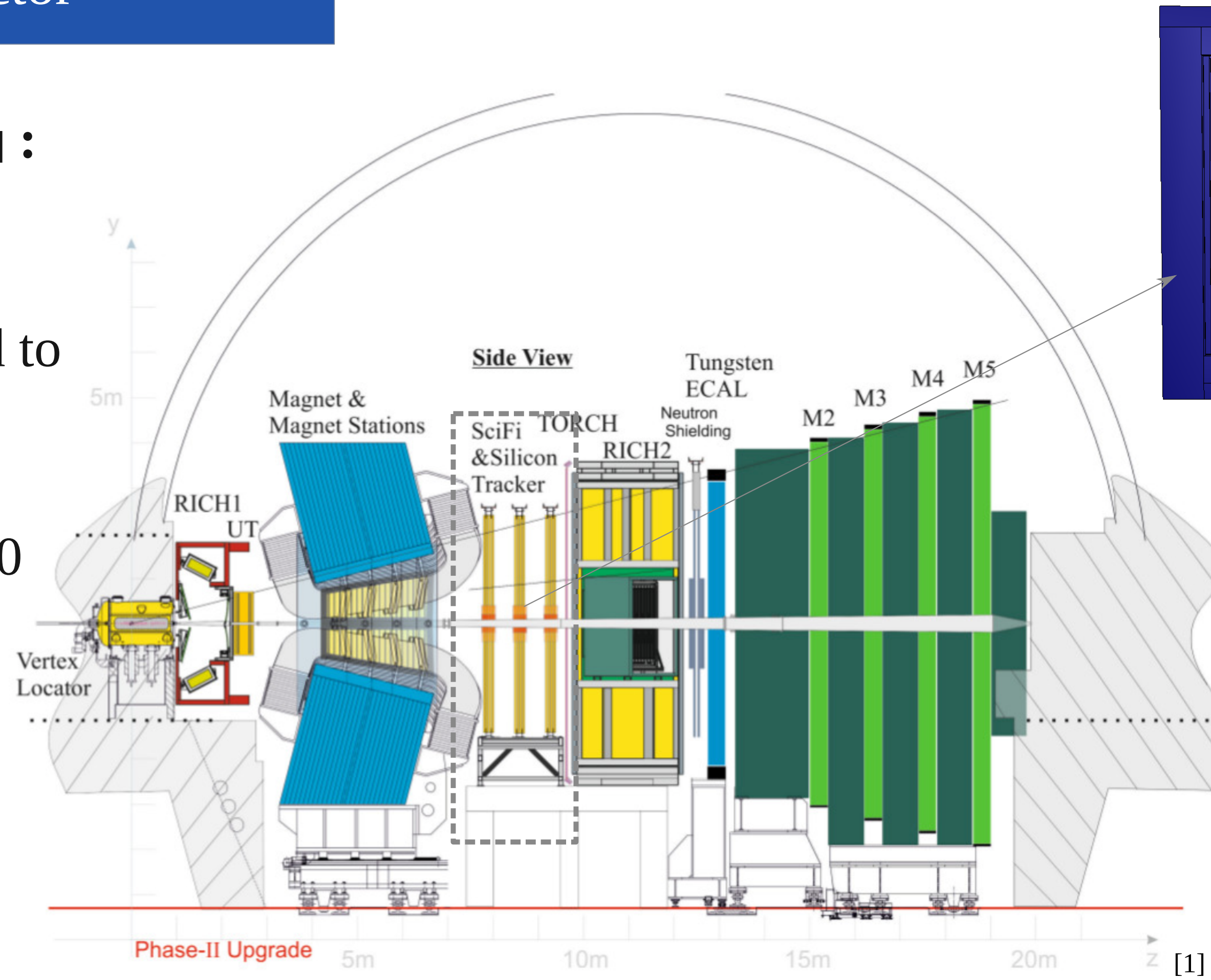
UNIVERSITÄT BONN

### LHCb Upgrade II Detector

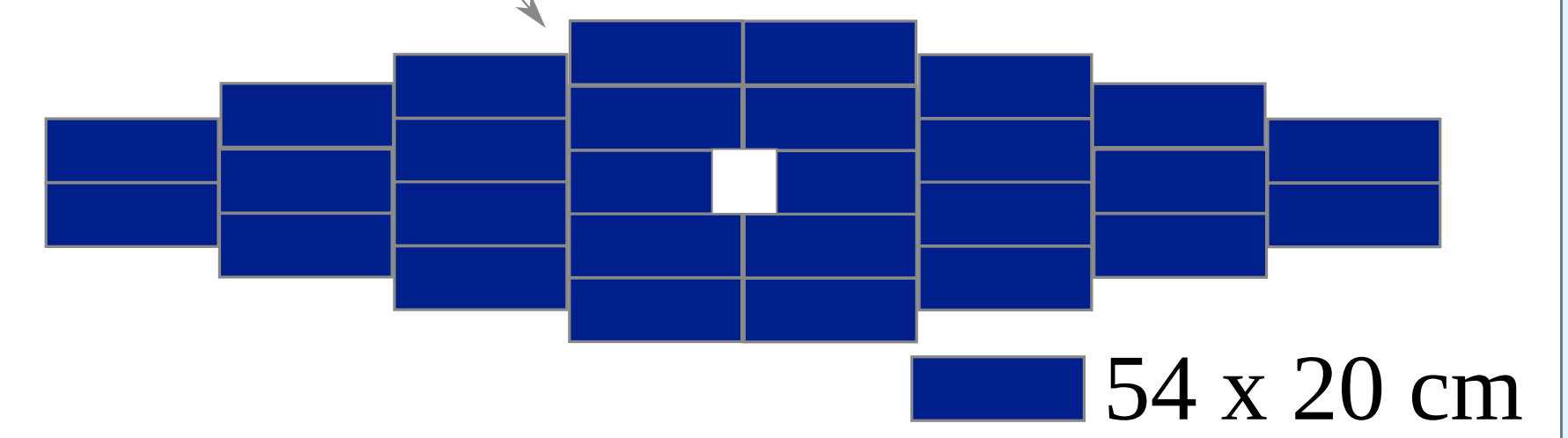
#### Planned Upgrade II specifications [1]:

- 40 MHz triggerless DAQ
- $L_{inst} = 1.5 \cdot 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
- 6x higher occupancy/fibre compared to Upgrade 1 for SciFi only
- $6 \cdot 10^{14} \text{ MeV n}_{eq}/\text{cm}^2$  after Run 6
- Interactions/bunch crossing  $\langle \mu \rangle = 40$

→ Upgrade during LS4 to ensure efficient tracking & particle identification



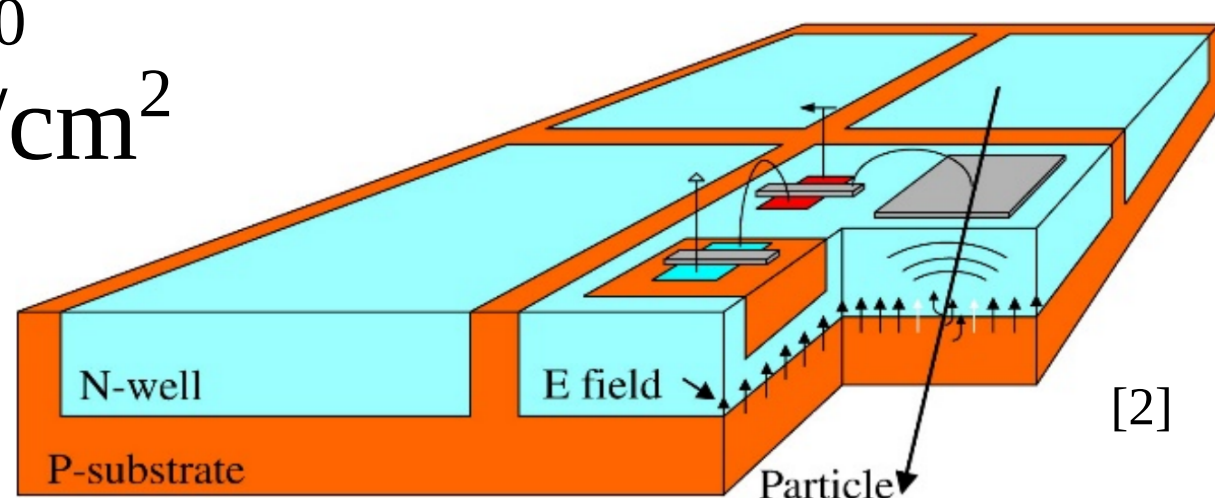
- 6 layers silicon in total
- 28 submodules/layer
- 35 pixel/submodule
- 18 m<sup>2</sup> pixel area



- Pixel size of 55 x 165 μm<sup>2</sup>
- 29 columns x 320 rows
- CMOS amplifier & comparator
- V1 chip size: 5 x 20 mm

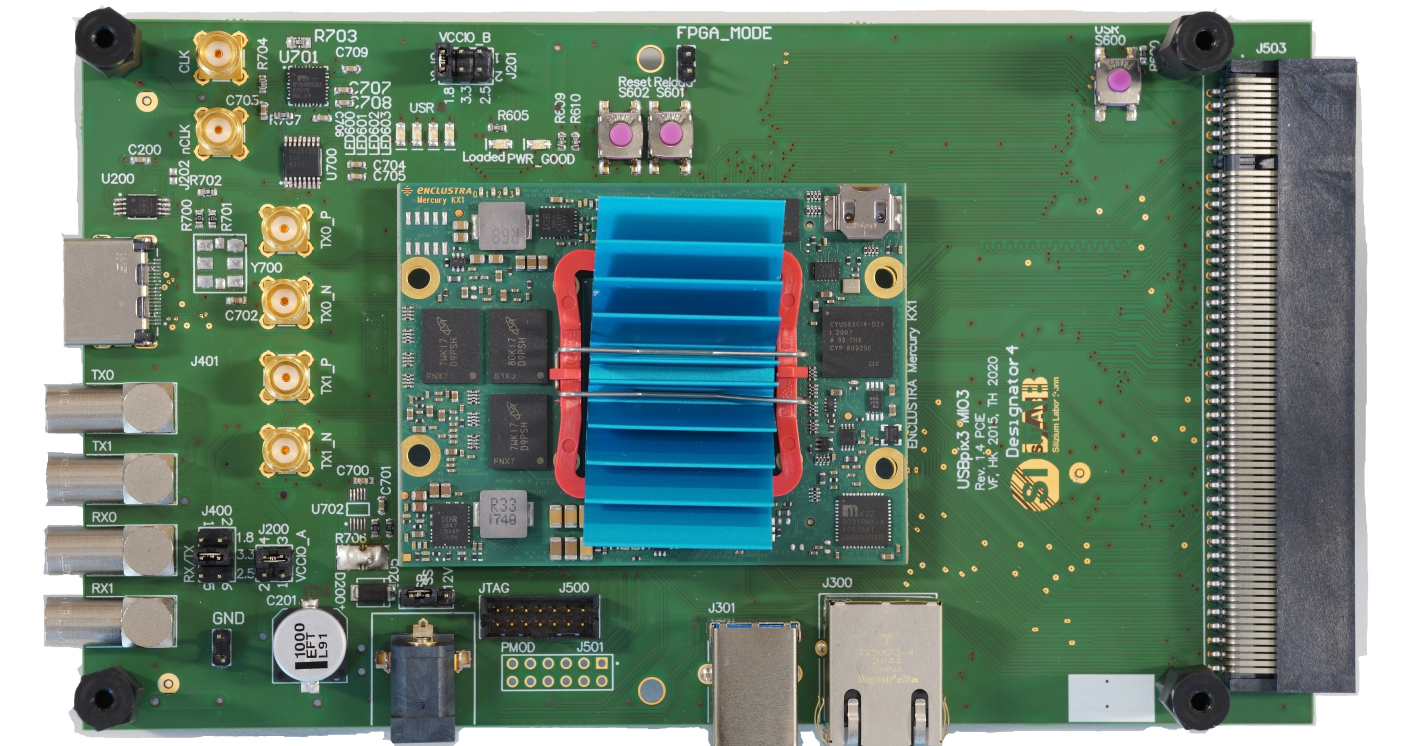
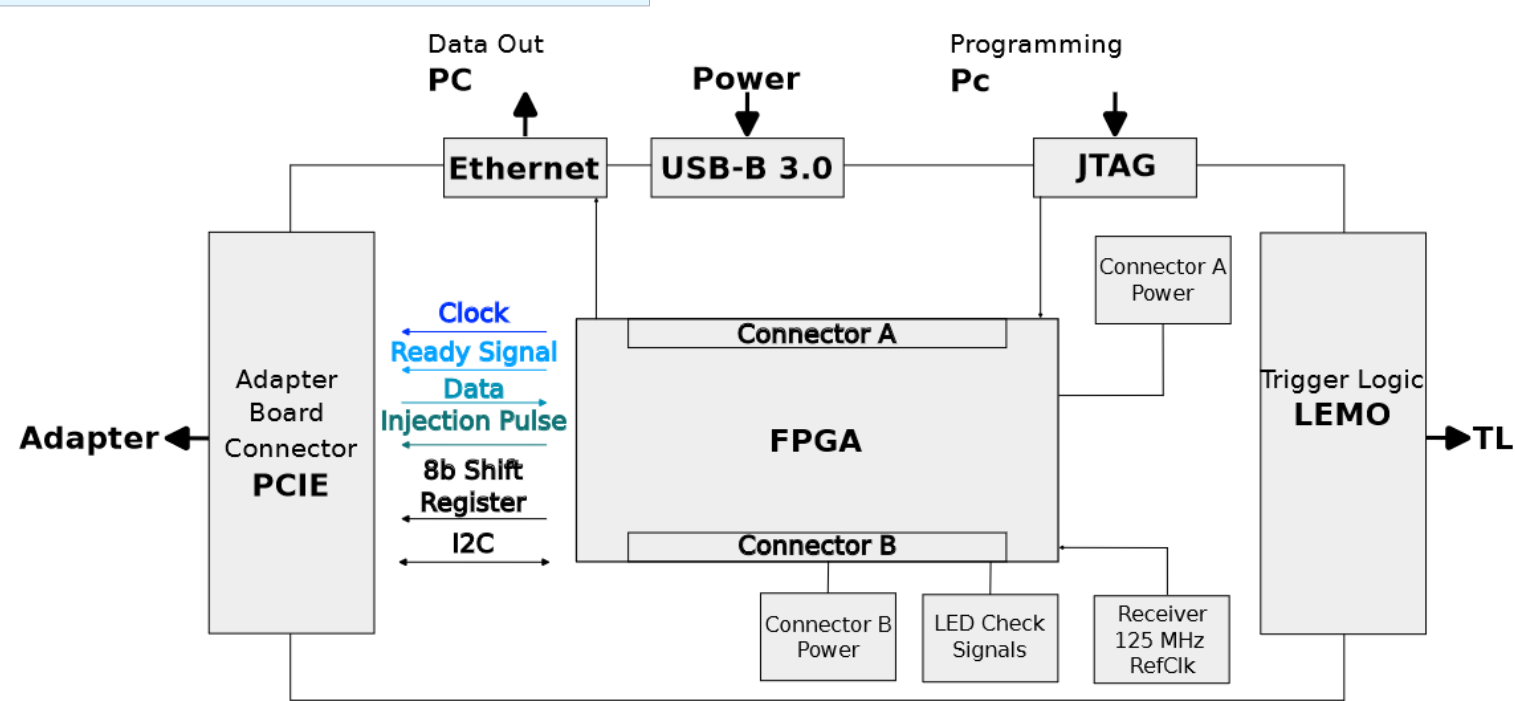
### MightyPix Specifications [1][2][3]

- Power consumption < 150 mW/cm<sup>2</sup>
- Low material budget < 1 % of X<sub>0</sub>
- Radiation hard:  $6 \cdot 10^{14} \text{ MeV n}_{eq}/\text{cm}^2$
- Time resolution < 3 ns
- Hit rate: 17 MHz/cm<sup>2</sup>
- HV-CMOS MAPS

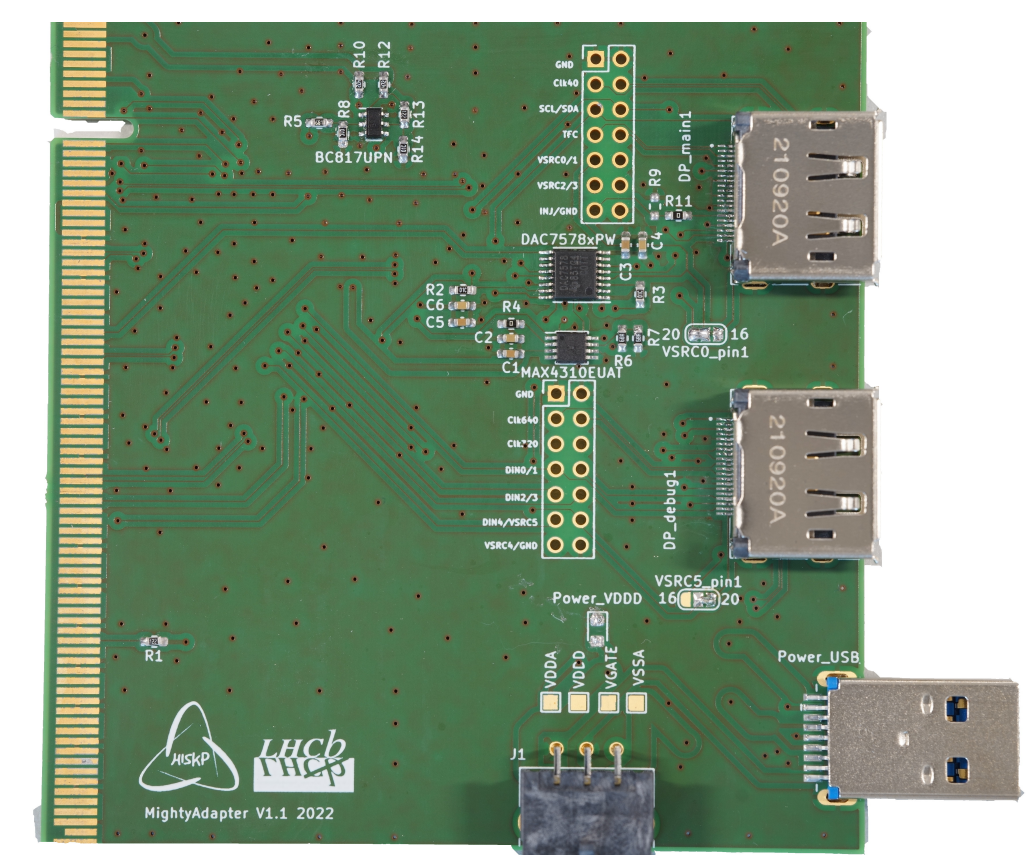
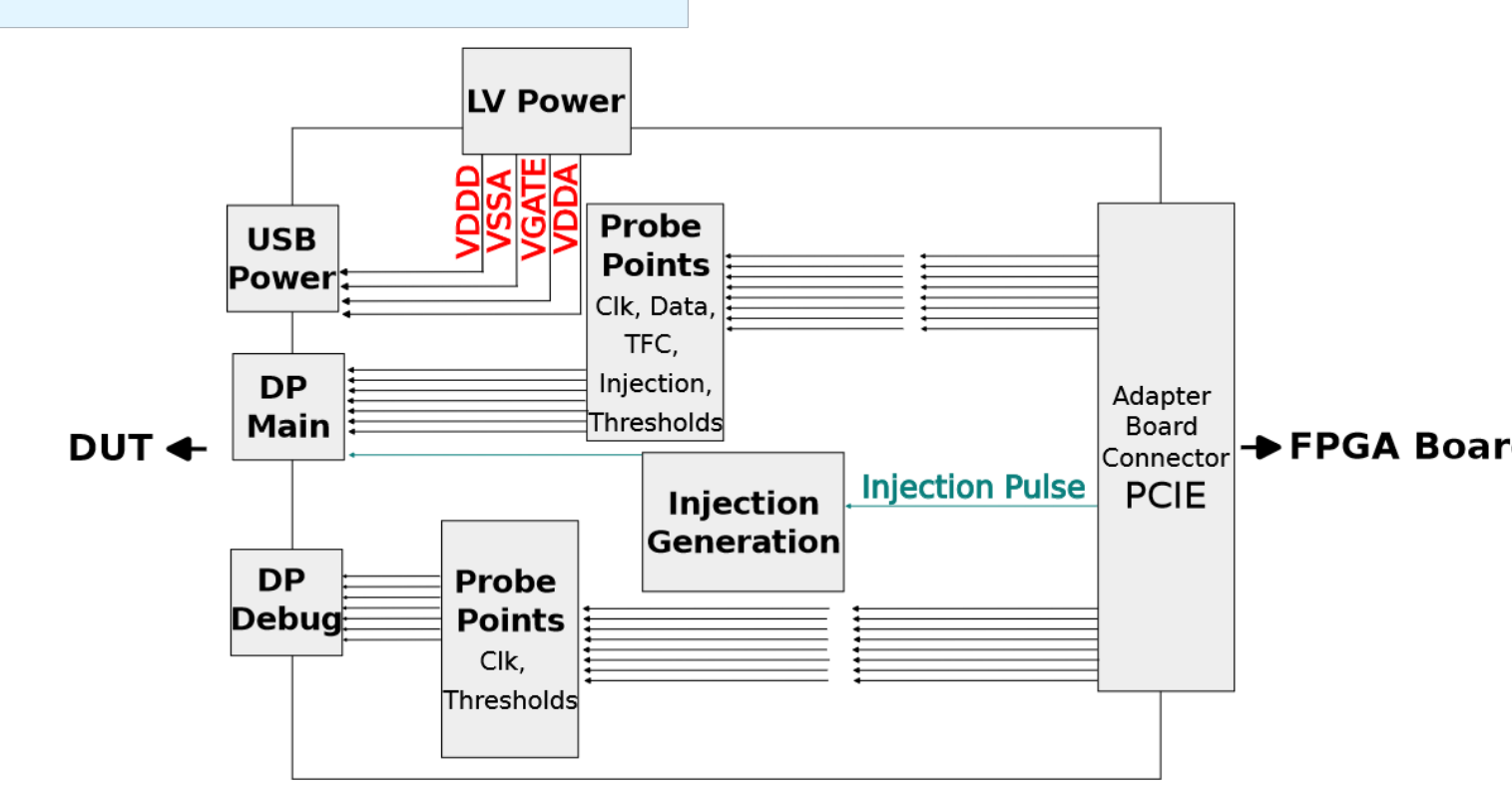


### MightyPix Readout - MARS

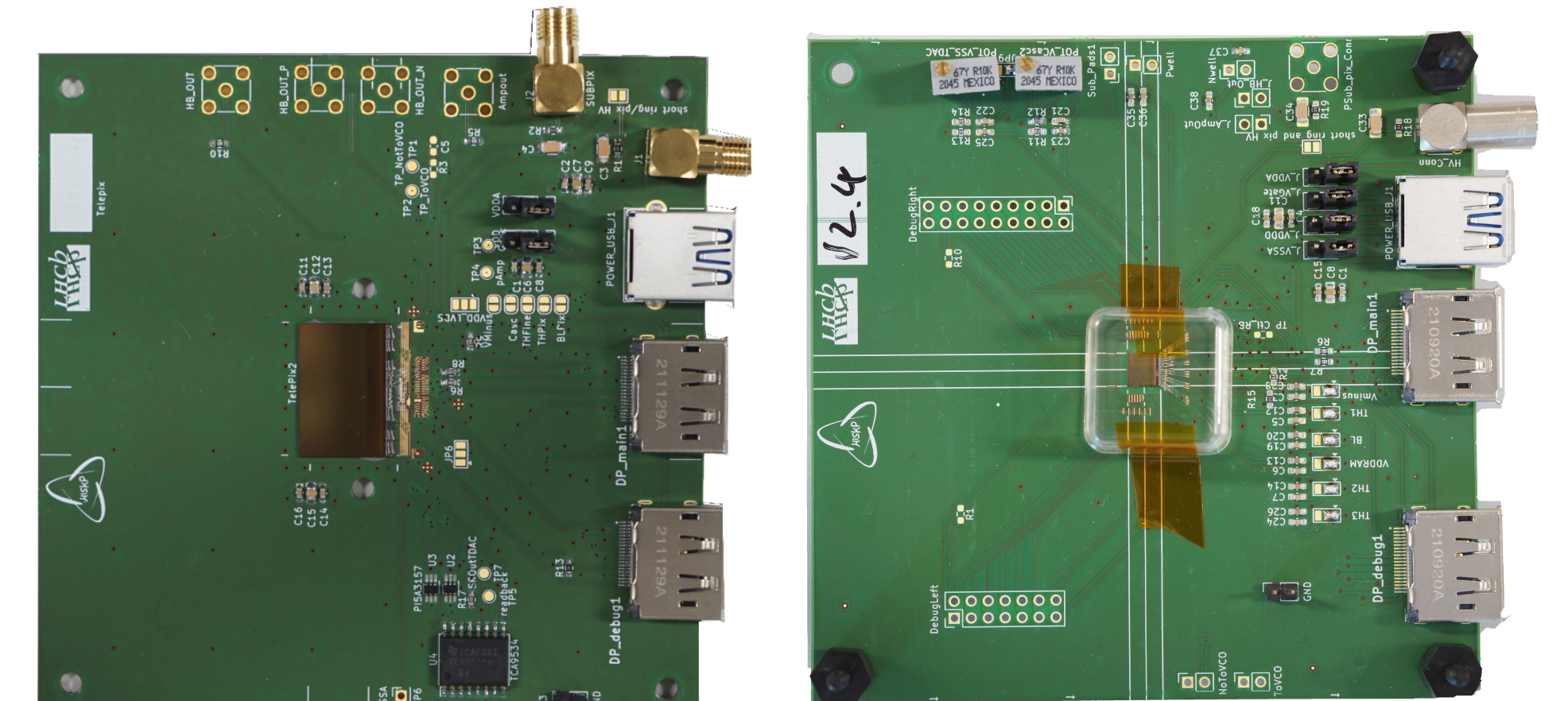
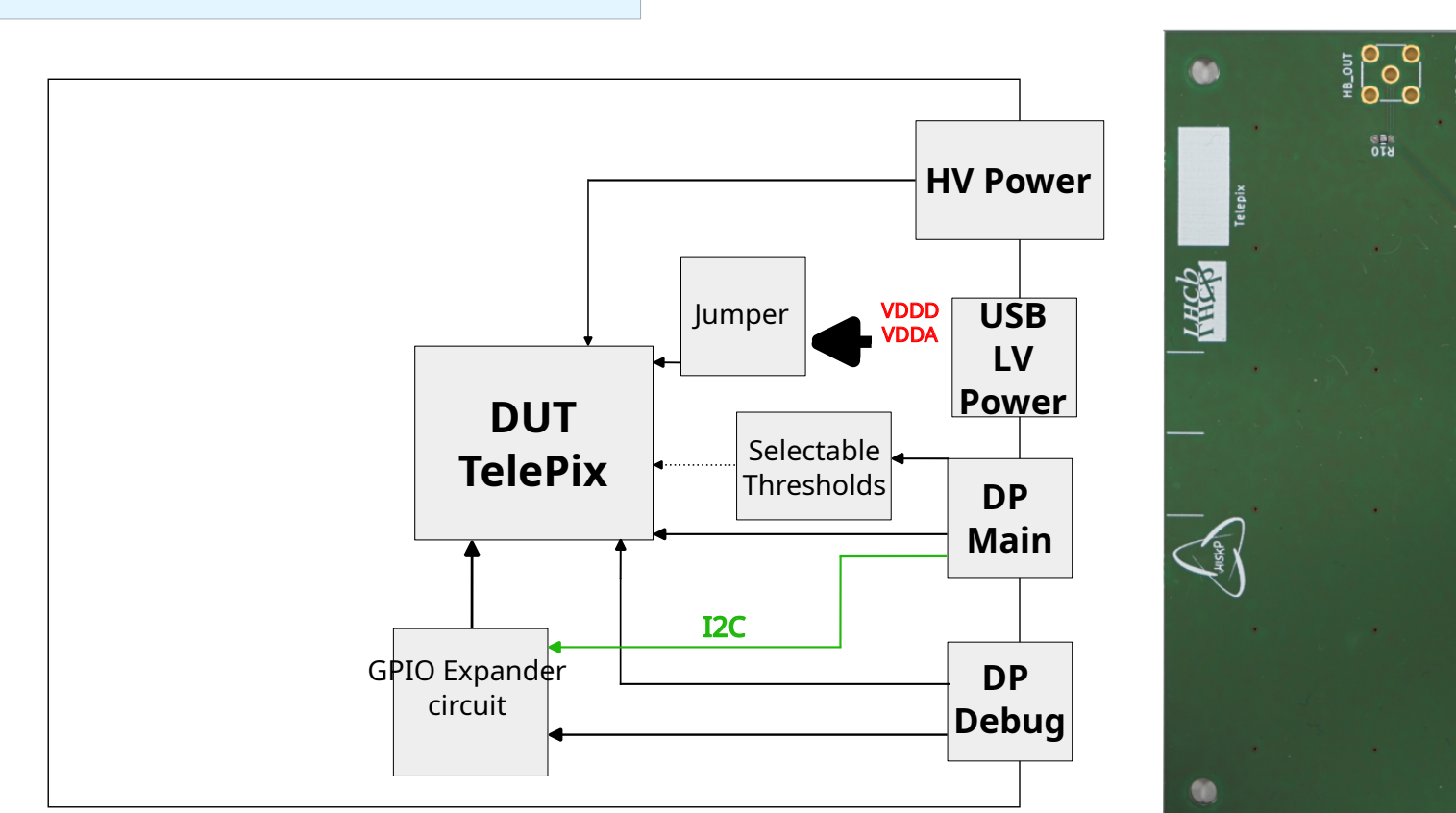
#### FPGA Board



#### Adapter Board

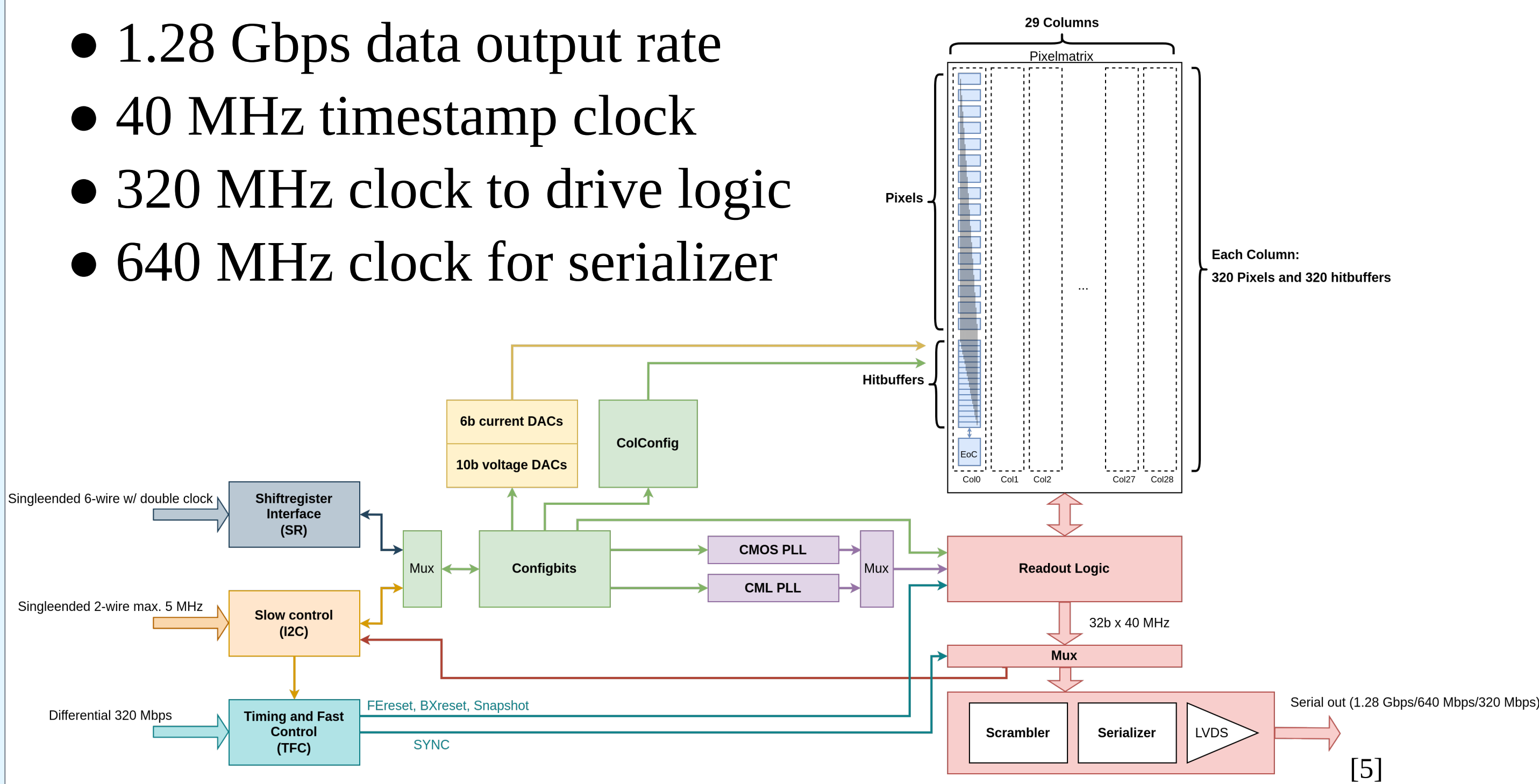


#### DUT Board



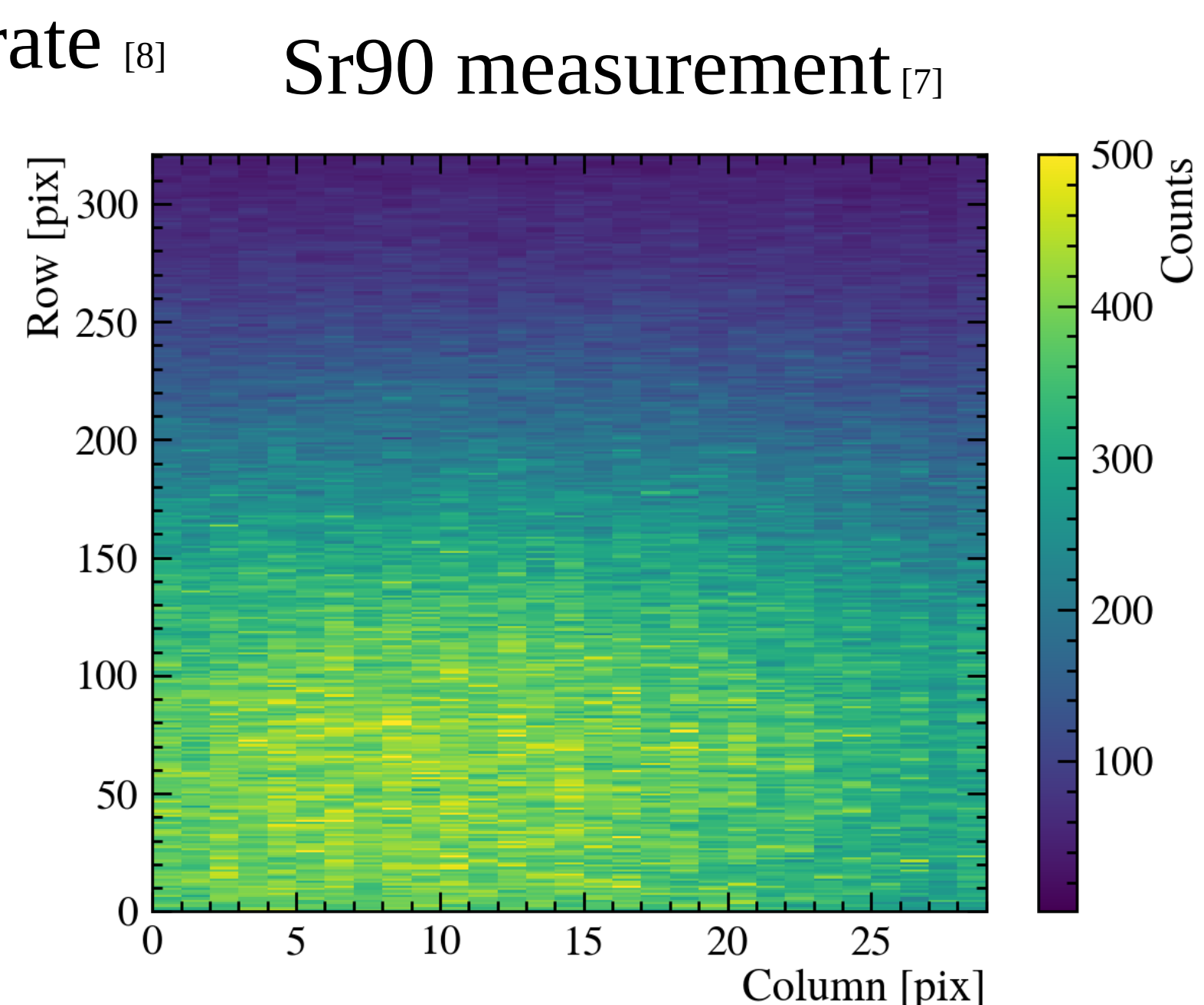
### MightyPix Design [1][2][3][5]

- Commercial 180 nm production
- Control interfaces: TFC, I2C, SR
- 1.28 Gbps data output rate
- 40 MHz timestamp clock
- 320 MHz clock to drive logic
- 640 MHz clock for serializer



### MightyPix - First Performance Studies [7]

- Simulation confirmed hit rate [8]
- Lab tests started 2023
- Functionality tests:
  - CMOS PLL
  - Slow control
  - TFC interface
  - SR interface
- Breakdown ~ 200V
- Time resolution studies started



### MARS - Specifications

- Modular & flexible hardware design
- Usable at testbeam facilities
- Adapter to use Chip carrier boards from other readout systems
- Multiple DUTBoards: Run2020, Run2021, TelePixV2, MightyPixV1
- High readout speed possible: 1.6 GBps
- Firmware: Modular design with switchable receiver (fast/slow)
- Slow control: Python interface with common functions for all DUTs
- DUT specification defined in configuration file
- Functionality validated for Run202x and TelePix sensors
- Characterization of TelePix ongoing

[1] Framework TDR for the LHCb Upgrade II - Opportunities in flavour physics, and beyond, in the HL-LHC era, LHCb Collaboration, CERN-LHCC-2021-012, LHCb-TDR-023

[2] A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology, I. Peric, NIM A 2

[3] TSI engineering run HVMAPS, I. Peric, https://adl.ipe.kit.edu/downloads/TSI\_engineering\_run\_v2.pdf

[4] https://github.com/SiLab-Bonn/basil, 06.09.2022

[5] MightyPix Documentation, N. Striebig & T. Frei, 21.11.2023

[6] https://gitlab.cern.ch/mightypix/MightyPixdaq, 21.11.2023

[7] L. Dittmann, Heidelberg University, Internal Communication 22.11.2023

[8] MightyPix at the LHCb Mighty Tracker, S.Scherl, TWEPP 2023