Motivation
High-Voltage CMOS (HVCMS) sensors, featuring a deep n-well separating the transistors and the depletion region, is intrinsically radiation hard. As the sensors can be implemented in commercially available technologies without modifying the process, HVCMS is a promising candidate for large-area tracking systems in future high energy collider experiments, such as:
• Upstream Tracker for LHCb upgrade II (max fluence $\sim 3 \times 10^{14} \text{cm}^{-2}$)
• Silicon tracker for future Circular Electron Positron Collider (covering area $\approx 70 \text{ m}^2$)
Series of successful HVCMS chips have been developed using IBM 180nm or LFfoundry 150nm technologies (ATLASpix, MuPix, LF-Monopix, …). Transition to smaller feature size will help improve chip performance, and open up more possibilities:
• Lower power dissipation, improved readout speed, …
• Higher circuit density hence more functionality

Feasibility study with 55nm technology
Two MPWs were submitted to a foundry with 55nm CMOS processes, to study the feasibility to implement HVCMS process using this foundry.

MPW with Low-Leakage process
MPW submitted in Aug 2022 with 55nm LL process, 40 chips received in Q2 2023
• NB: not HV process, yet having a similar deep-n-well structure separating the transistors and substrate
• 3 × 2 mm$^2$ in area
• Standard (low-resistivity) wafer → limited charge generation
• Variation of passive diode arrays
• Simple amplifiers in corners

Layout
Passive sensor arrays:
• 12 layout design to enable effect of pixel size, charge sharing etc.
• Pixel size: 25 × 150μm$^2$, 50 × 150μm$^2$
• Pixel array: 3 × 4
• With/without P stop betw. pixels
• Space betw. pixels: 5μm/10μm/15μm
• Connection method

Typical IV curves
• Breakdown voltage $\sim 6$V
• Leakage current small $\sim 100$μA
• Capacitance of a single pixel 0.1~0.2 pF as expected
• Noise reduces when applying reverse bias voltage

Preliminary test results

In-pixel electronics
• Sensor biased with active resistor
• Calibration capacitor integrated
• Charge Sensitive Amplifier structure
• Two stage source follower used to drive the signal out

MPW with High-Voltage process
MPW submitted in Oct 2023 with 55nm High-Voltage process
• 1 kΩ - n-type substrate $\rightarrow$ expected breakdown voltage $> 50$ V
• 4 × 3 mm$^2$ in area
• 10 metal layers enabling fine pitch routing, with 2 thick metal layers for power
• Core power 1.2V, custom designed I0

Summary
Motivated by large-area and irradiation-hard tracking for future collider experiments, attempts are made with a potential 55nm technology:
• MPW submitted with LL (non-HV) process with standard substrate to validate deep n well structure; preliminary results are encouraging.
• MPW submitted with HV process using high resistance substrate with various design to validate the process. Chips expected in early 2024.