Feasibility Study of CMOS Sensor in 55nm Process for Tracking

Zhuojun Chen[1], Ruoshi Dong[2,3], **Yiming Li***[2], Weiguo Lu[2], Yunpeng Lu[2], Ivan Peric[3], Jianchun Wang[2], Zhiyu Xiang[2], Zijun Xu[2], Hui Zhang[3], Mei Zhao[2], Yang Zhou[2], Hongbo Zhu[4], Xiaoyu Zhu[2,5]

[1]*Hunan University, Changsha, China*
[2]*Institute of High Energy Physics, CAS, Beijing, China*
[3]*Karlsruher Institut für Technologie, Karlruher, Germany*
[4]*Zhejiang University, Hangzhou, China*
[5]*Central China Normal University, Wuhan, China*
***E-mail: liyiming@ihep.ac.cn**

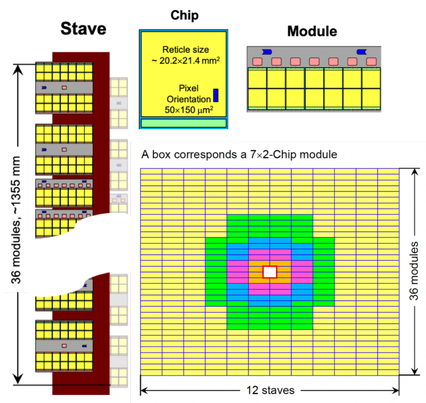
Motivation

High-Voltage CMOS (HVCMOS) sensors, featuring a deep n-well separating the transistors and the depletion region, is intrinsically radiation hard. As the sensors can be implemented in commercially available technologies without modifying the process, HVCMOS is a promising candidate for large-area tracking systems in future high energy collider experiments, such as:

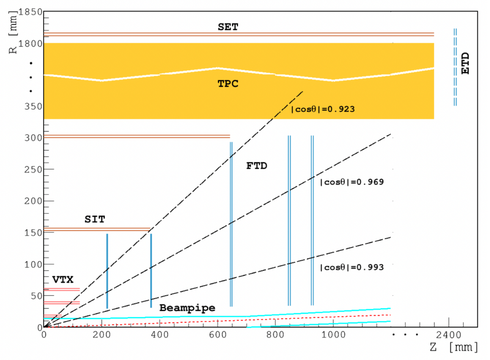
- Upstream Tracker for LHCb upgrade II (max fluence ~ $3\times10^{15} n_{eq}/\mathrm{cm}^2$)
- Silicon tracker for future Circular Electron Positron Collider (covering area >~ 70 m^2)

Series of successful HVCMOS chips have been developed using IBM 180nm or LFoundry 150nm technologies (ATLASPix, MuPix, LF-Monopix, …). Transition to smaller feature size will help improve chip performance, and open up more opportunities:

- Lower power dissipation, improved readout speed, …
- Higher circuit density hence more functionality



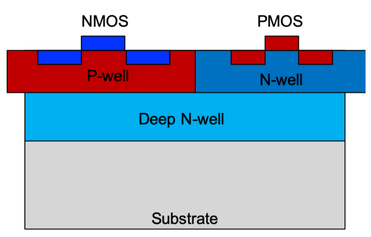
Proposal for LHCb Upstream Tracker upgrade in Upgrade II
CERN-LHCC-2021-012



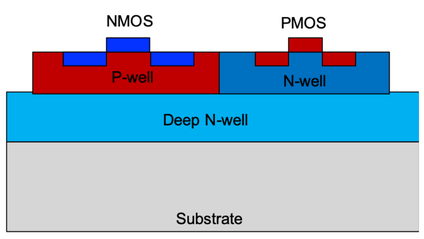
Tracking system (a quarter) of the CEPC baseline detector concept
CEPC CDR, arXiv:1811.10545

Feasibility study with 55nm technology

Two MPWs were submitted to a foundry with 55nm CMOS processes, to study the feasibility to implement HVCMOS process using this foundry.



55nm Low-Leakage process
Submitted in Aug 2022 to verify the deep n-well structure



55nm High-Voltage process
Submitted in Oct 2023 to verify the sensor on a high-resistivity wafer

MPW with Low-Leakage process

MPW submitted in Aug 2022 with 55nm LL process, 40 chips received in Q2 2023

- NB: not HV process, yet having a similar deep-n-well structure separating the transistors and substrate
- 3×2 mm^2 in area
- Standard (low-resistivity) wafer → limited charge generation
- Variation of passive diode arrays
- Simple amplifiers in corners

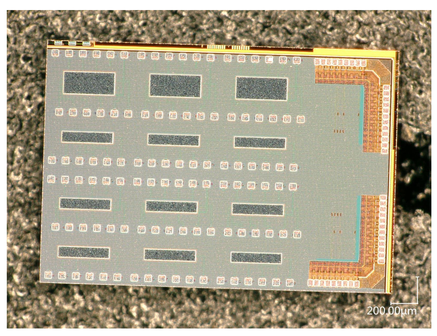
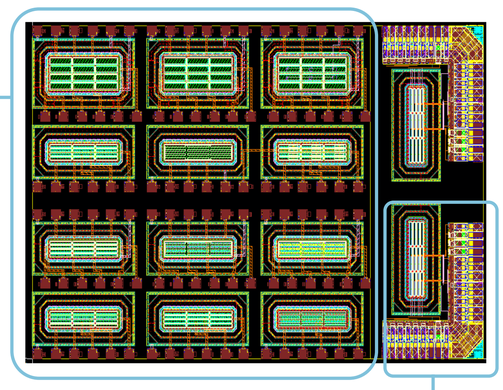


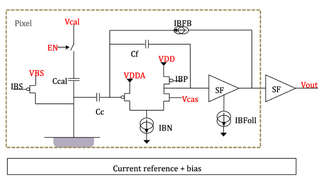
Photo of a chip from 55nm LL MPW

Layout

Passive sensor arrays:

- 12 layout design to enable effect of pixel size, charge sharing etc.
- Pixel size： $25 \times 150\mathrm{um}^2$, $50 \times 150\mathrm{um}^2$
- Pixel array： 3×4
- With/without P stop betw. pixels
- Space betw. pixels: 5um/10um/15um
- Connection method



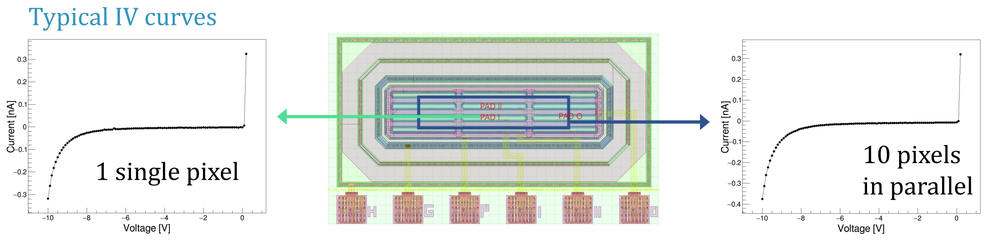


In-pixel electronics

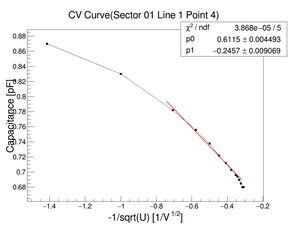
- Sensor biased with active resistor
- Calibration capacitor integrated
- Charge Sensitive Amplifier structure
- Two stage source follower used to drive the signal out

Preliminary test results

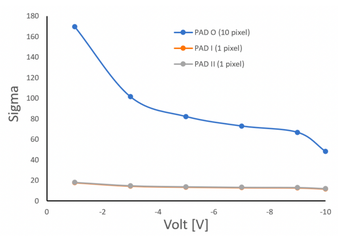
Typical IV curves



- Breakdown voltage ~-8V
- Leakage current small ~10pA
- Capacitance of a single pixel 0.1~0.2 pF as expected
- Noise reduces when applying reversed bias voltage



CV of a single pixel

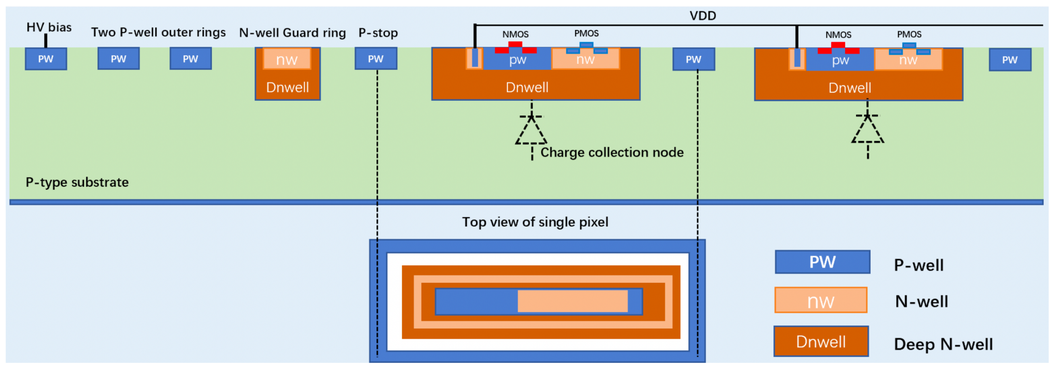


Noise wrt. bias voltage

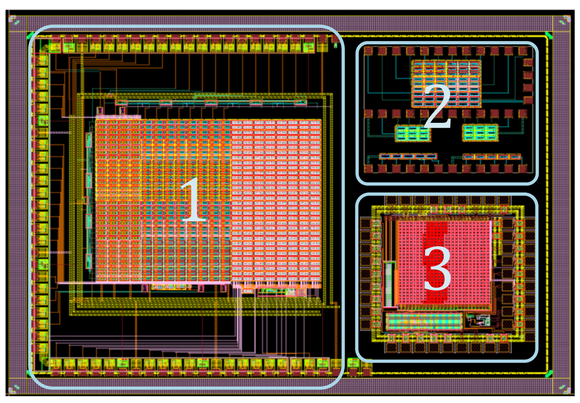
MPW with High-Voltage process

MPW submitted in Oct 2023 with 55nm High-Voltage process

- 1 kΩ · cm p-type substrate → expected breakdown voltage > 50 V
- 4×3 mm^2 in area
- 10 metal layers enabling fine pitch routing, with 2 thick metal layers for power
- Core power 1.2V, custom designed IO



Cross-section and top view of the guard ring and pixel structure



Layout

Three sections:

1. 32×20 pixel matrix with varius diodes and in-pixel amplifier or discriminator designs for process validation
2. 5 passive diode arrays for study on sensing diode and charge sharing
3. 26×26 pixel matrix with digital readout periphery for novel electronics structure study

Sections 1 and 2:

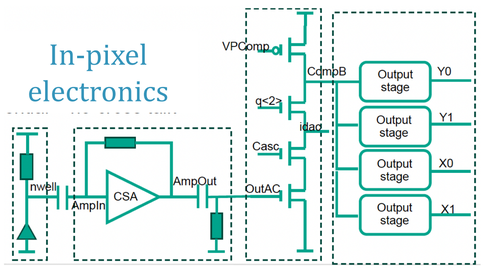
- Pixel size 40 µm × 80 µm; Six flavours of charge sensing diodes
- Two versions of in-pixel electronics; both analog and digital signals are output

Diode flavour	Specification	
Pix_D10core	Single DNW size 30 µm × 70 µm, Space betw. Neighbouring nodes: 10µm	With P stop betw. pixels
Pix_D10core_wps		Without P stop
Pix_D15core	Single DNW size 20 µm × 60 µm, Space betw. Neighbouring nodes: 20µm	With P stop betw. pixels
Pix_D15core_wps		Without P stop
Pix_D20core	Single DNW size 25 µm × 65 µm, Space betw. Neighbouring nodes: 15µm	With P stop betw. pixels
Pix_D20core_wps		Without P stop

Sections 3:

- Pixel size 25 µm × 25 µm; 26 row × 26 columns; Bias provided by 8-bit voltage DAC
- Timestamp measurement: 24 columns analog + 2 columns digital encoding of pixel address

In-pixel electronics



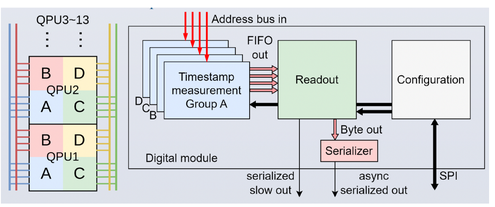


Diagram of digital module.
A 2×2 array forms a quad pixel unit (QPU)

Summary

Motivated by large-area and irradiation-hard tracking for future collider experiments, attempts are made with a potential 55nm technology.

- MPW submitted with LL (non-HV) process with standard substrate to validate deep n well structure; preliminary results are encouraging.
- MPW submitted with HV process using high resistivity substrate with various design to validate the process. Chips expected in early 2024.

The 13th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD13), Vancouver, Canada