Radiation Study of the LHCb UT front-end readout ASIC

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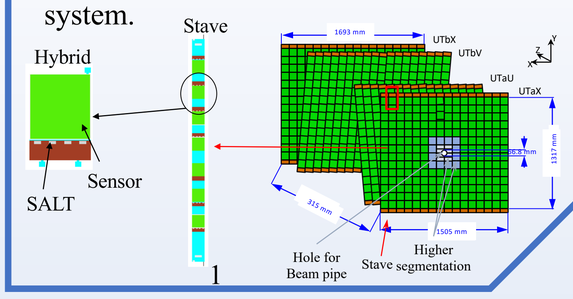
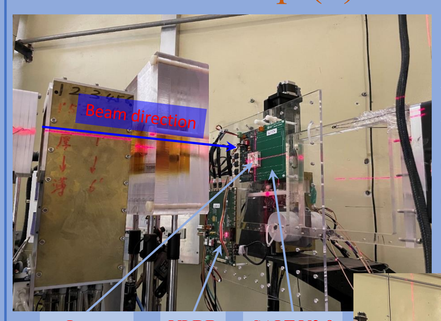
Introduction

- **UT**(Upstream Tracker) is a new silicon strip tracker in LHCb upgrade I.
- It has 4 layers, each layer consists of 16/18 staves, and each stave consists of 14/16 hybrids.
- **SALT** (Silicon ASIC for LHCb Tracker) is the front end readout ASIC of the UT system.



Test Beam Setup (1)



Main equipment
a) 1 SALT board + 1 VLDB board
b) 1 LinuxPC
c) 1 MiniDAQ
d) 1 Raspberry Pi3 computer

The Features of Beam	
Size	2.0×2.0cm²
Energy	100MeV
Flux	3×10^{7}–$10^{10} p/cm^2/s$
Uniformity	90%

Run	Starting Time	Flux [cm⁻²s⁻¹]	SEU			TMR						
			Ped	Trim	Ext	SER	DSP	ANA	MIS	TFC	MEM	GLB
1	133201	3.12 E7	0	0	0	3	6	3	0	4	0	28
2	140203	1.35 E8	0	0	0	0	10	6	4	5	0	59
3	143436	1.03 E9	1	0	0	5	71	81	17	25	7	-
4	145750	1.12 E10	removed due to a mechanical issue									
5	155531	1.03 E9	1	0	0	7	59	66	17	38	2	-
6	160824	1.12 E10	4	3	1	63	-	-	214	-	56	-
7	162440	1.12 E10	3	4	1	64	-	-	x	-	51	-

- Calibration with a Faraday cup was performed for each intensity value.
- The total fluence for SEU test is 1.48×10^{13} cm^{-2}, 45.5% with KillMask.

Register configuration & Rate of SEUs

- SALT V3.9 was configured to a normal running condition.
- In the last run KillMask = 0×00, so as to read out ADC value from all channels.

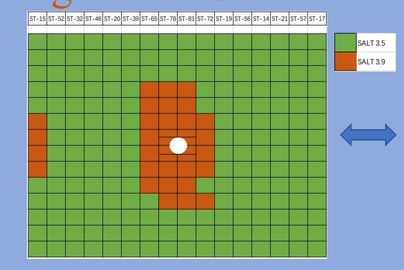
Address	Number	Value	Function
206-285	128	0×AA	TrimDAC
115-194	128	0×AA	Pedestal
105-114	16	0×AA	Kill Mask
307-316	16	0×AA	Inject Mask
205	1	0×AA	Global TrimDac
286-287	2	0×AA	TestChan TrimDAC

- Here are all SEUs in the Configuration Registers.

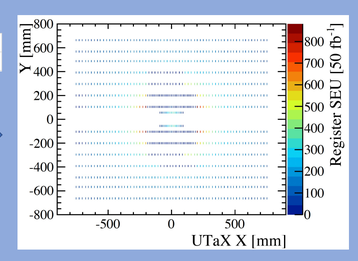
Chronological order	Run	Regi	Vset	Vnew	Nbit	Ch
	3	154	AA	00	4	3F
	5	190	AA	8A	1	7B
6		26F	AA	8A	1	69
		144	AA	08	3	2F
		14F	AA	A0	2	3A
		26D	AA	A2	1	67
		214	AA	A2	1	0E
		14D	AA	00	4	38
		11E	AA	00	4	09
		114	AA	00	4	-
7		245	AA	88	2	3F
		217	AA	8A	1	11
		130	AA	00	4	1B
		182	AA	02	3	6D
		214	AA	80	3	0E
		204	0C	08	1	-
		21D	AA	82	2	17
		172	AA	00	4	5D

- The SEU rate of the per channel TrimDAC register.
  a) Total 7 register changes ⇒ cross section = 4.7×10^{-13} cm^2.
  b) SEU rates among UT vary due to the related different hadron fluence.
  c) The max TrimDAC SEU is 755.1/ASIC corresponding to a total integrated luminosity $50 fb^{-1}$.
- Maximum Pedestal register SEU: 200.9 /ASIC.

Register SEUs



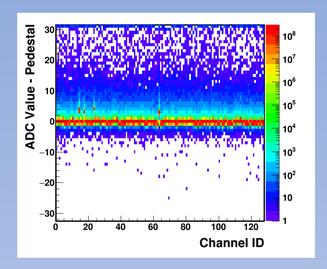
Chip version map for the first layer



Register SEUs Vs 992 ASICs distribution

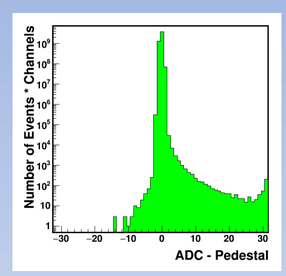
- The register SEUs have much higher value nearby the most inner region with ASIC version of 3.5.

ADC SEUs



Flux = 1.12×10^{10} cm^{-2}s^{-1}

~140 M NZS events, remove channels **14,17,23,& 63** that TrimDAC registers changed.

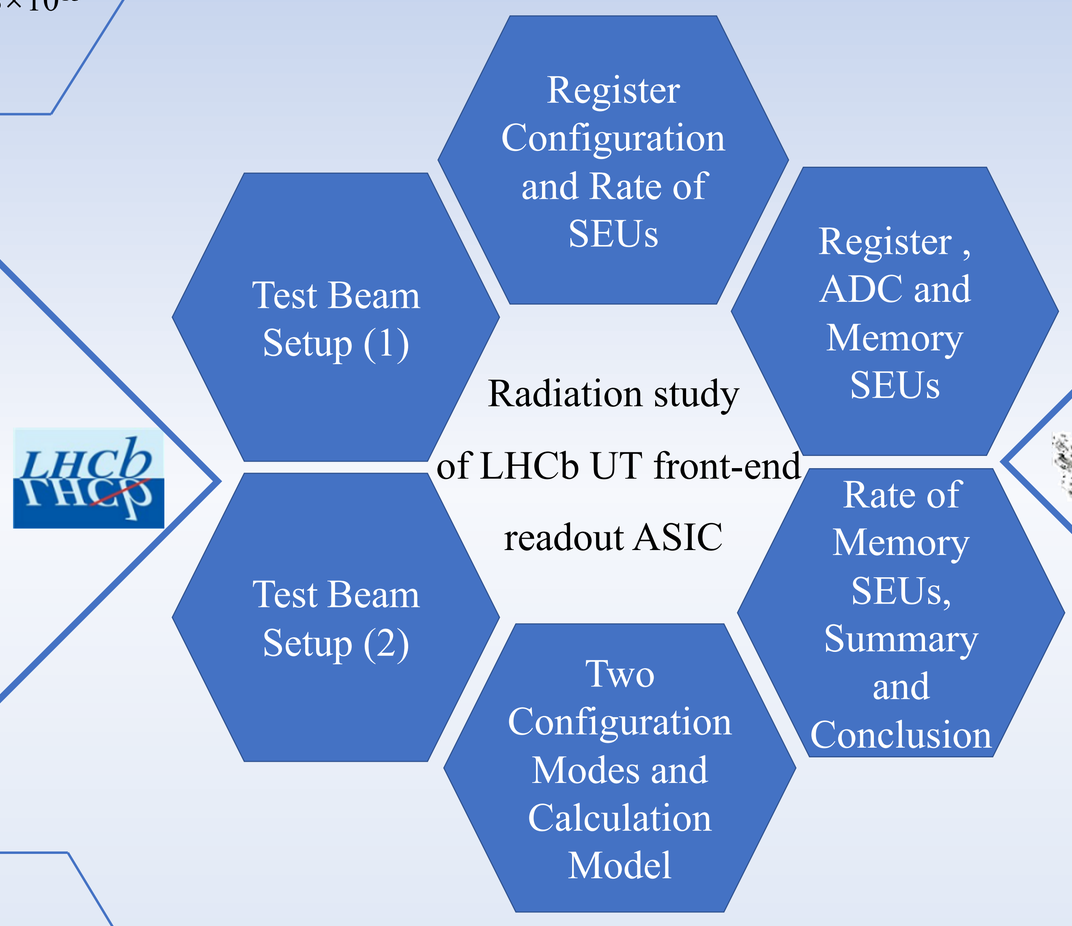


ADC – Ped	Rate
> +7	4.8×10^{-7}
> +5	8.1×10^{-7}
> +3	1.7×10^{-6}
< –3	3.5×10^{-8}
< –5	9.1×10^{-9}
< –7	4.2×10^{-9}

Memory SEUs

- 2 memory SEUs were observed, so we did another beam test at Dongguan to check more about memory SEUs.

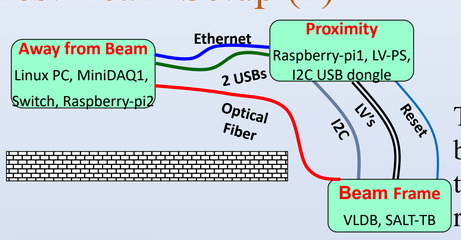
Register SEU Test @CIAE



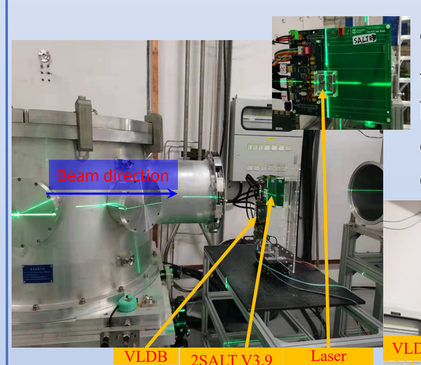
Motivation

- SALT V3.5 is vulnerable to radiation in its TrimDAC and Pedestal registers. The cross sections are 7.8×10^{-11} cm^2 and 1.3×10^{-11} cm^2, respectively.
- **SALT V3.9 was also tested twice.**
  The first was at the **CIAE** (China Institute of Atomic Energy) on Dec 31, 2020.
  The second was at the **CSNS** (China Spallation Neutron Source) from Oct 18 to 25, 2021.

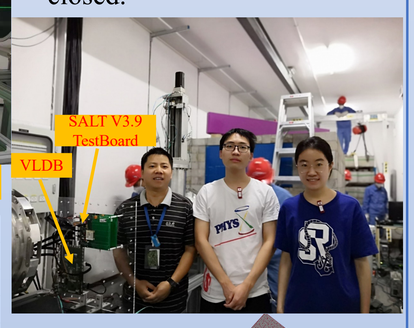
Test Beam Setup (2)



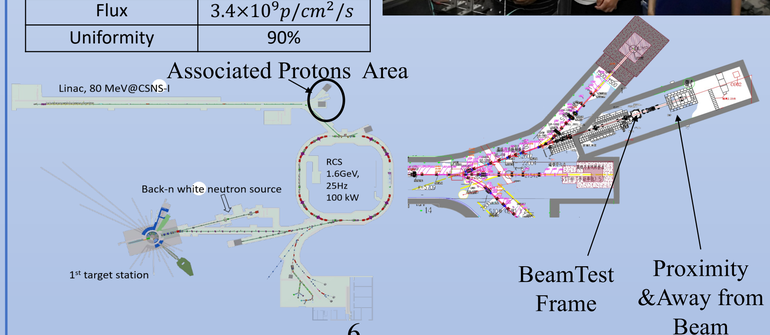
The two layouts are basically similar, except that we added an extra raspberry-pi to reset the CCPC of the MiniDAQ.



The same board used at CIAE was tested at CSNS. The 2nd board failed and could not be connected once the cavern is closed.



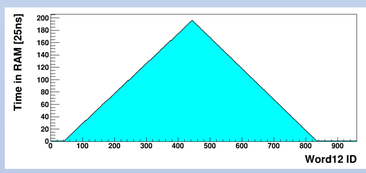
The Features of Beam	
Size	2.0×2.0cm²
Energy	80MeV
Flux	$3.4\times10^{9} p/cm^2/s$
Uniformity	90%



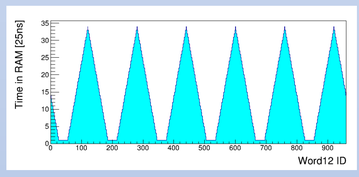
Memory SEU Test @CSNS

Two Configuration Modes & Calculation Model

- SALT V3.9 was set to a special mode that the ADC value is constant 0x15.
- In order to calculate the rate of SEUs occurring **during memory** or **data transfer**, we planned two different configurations, difference between which is the time of data in the memory~6 times.
  DAQ Configuration:
  ❑MEP size of N × 480 BXs.
  ❑TFC sequence= 6*(1 NZS + 79 HeaderOnly).
  Average time in memory: 81.4*25ns
  TFC sequence= (1 NZS + 79 HeaderOnly).
  Average time in memory: 14.4*25ns



Memory-dominated Mode



Transfer-dominated Mode

- During the process of fetching data, the beam flux was maintained at $3.4\times10^{9} p/cm^2/s$. There are 10 and 7 SEUs observed in the two modes respectively.
- Calculation Model

$$N^{RAM} \propto T\times \sigma_{RAM} \times fluence \qquad N_1 = N_1^{RAM} + N_1^{Trans}$$
$$N^{Trans} \propto \sigma_{Trans} \times fluence \qquad N_2 = N_2^{RAM} + N_2^{Trans}$$

Rate of Memory SEUs

The cross section of data during transfer is much larger (~100 times) than that in memory. Take the cross section of **data transfer as the total cross section**.

- The SEU rate of the per channel in data transfer:
  a) cross section $\sigma_{total} = 5.9\times10^{-14} cm^2$.
  b) The maximum memory SEU is 19.4/ASIC corresponding to a total integrated luminosity $50 fb^{-1}$.

Summary of SEUs @ $50 fb^{-1}$

	aX	aU	bV	bX
Total ASIC	992	992	1104	1104
SALT V3.9	224	248	200	224
SALT V3.5	768	744	904	880
Average TrimDAC SEU (/ASIC)	126.5	122.2	125.2	124.0
Average Pedestal SEU (/ASIC)	25.5	24.8	24.8	24.6
Average Memory SEU (/ASIC)	2.2	2.0	2.4	2.1

Conclusion

- The rate of SEUs is low enough to LHCb.
- SALT has excellent performance in radiation resistance.

Acknowledgements

- Thanks to everyone for helping set up a system at Beijing, especially Zhuoming Li, Federico Alessio, Paolo Durante, Ken Wyllie, Carlos Abellan, Will Parker, CIAE and CSNS colleagues.

13th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD13), Vancouver, Canada