Analysis of MOS capacitor with p-layer with TCAD simulation

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Abstract - The ATLAS18 strip sensors of the ATLAS inner tracker upgrade (ITk) are under production since 2021. Along with the large-format n⁺-in-p strip sensor in the center of the wafer, test structures are laid out in the open space for monitoring the performance of the strip sensor and its fabrication process. One of the structures is a 1.2×1.0 mm² test chip that includes representative structures of the strips, and Metal-Oxide-Silicon (MOS) capacitors. In addition to the standard MOS capacitor, a MOS capacitor with a p-layer in the surface of silicon, the MOS-p capacitor, is designed with a p-density representative of the p-stop doping for isolating the n⁺ strips. The C-V curve of the MOS capacitor shows characteristic behavior in the accumulation, depletion, and inversion regions as a function of bias voltage, from which one can estimate the amount of the interface charge. The MOS-p capacitor shows the C-V curve modulated by the properties of the p-layer.

With over 50% of the full production complement delivered, we have observed consistent characteristics in the MOS-p capacitors. Rarely and currently only in 3 batches, we have observed abnormalities. To further study them, we have simulated the MOS-p capacitor with TCAD software, which successfully reproduces the normal behavior, including a feature caused by a geometrical setback of the p-layer to the metal area, with the p-density and the interface charge within the expected range. By contrast, the overall shapes of the abnormal cases are only reproduced with 1/10 of the p-density to the specification and possible charge traps in the p-layer area. A smaller but distinctive feature in the behavior may require a non-uniform distribution of the p-density and the interface charge or something else. These simulations help to take final decisions for the batches in production.

Introduction – We are producing 20800 strip sensors for the upgrade ATLAS inner tracker (ITk), in 8 different shapes (2 in the barrel and 6 in the endcap sections) [1]. The strip sensors are made of n⁺ readout strips in the p-type silicon bulk, with p-stop isolation structure between the n⁺ strips. In the wafer layout (Fig. 1), we have implemented two Metal-Oxide-Silicon (MOS) capacitors in the Quality Assurance (QA) chips, for evaluating the interface charge and the density of the p-stop implantation (Fig. 2), (1) the standard capacitor (MOS) and (2) a special MOS capacitor with p-layer in the surface of the silicon bulk with the density of p-stop isolation (MOS-p) (Fig. 3).

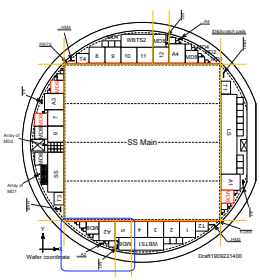

Fig. 1 Wafer layout of barrel sensor, Short-strip type (SS). QA chips are groups of test structures (encircled in blue), diced out in orange into Testchip&MD8 and Mini&MD8, one set per wafer.

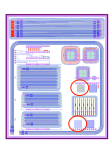

Fig. 2 ATLAS test chip (labeled as Ax in the wafer layout). Two MOS capacitors are encircled in red.

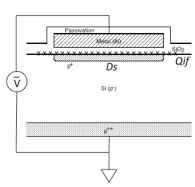

Fig. 3 MOS-p capacitor, implemented in 2D in TCAD. *Qif* is the interface charge in the interface of oxide and silicon bulk. *Ds* is the density of p implantation.

As of November 2023, we have received over 50% of the sensors, in 300 or more batches. We have observed abnormal behavior in the MOS-p capacitors in 3 batches: VPA37921, 42646, and 46225 [2]. Such abnormal behaviors are shown together with a normal case of VPA37914 et al (Fig. 4). We have tried to understand the source of such abnormalities with a technology CAD program (TCAD) [3].

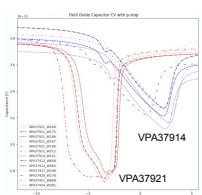

Fig. 4 Normal (VPA37914) and abnormal (VPA37921) behaviors of MOS-p capacitor, in the "Flatband voltage measurement".

TCAD setup – We have used a TCAD 3D device simulator, HyDeLEOS VER. 8.5k [3]. The MOS structure is implemented in 2D geometry (Fig. 3). Geometrical parameters are listed in Table 1. We have varied mainly the interface charge (shown with "x" in Fig. 3) and the density of p-layer, which surface density is *Qif* and *Ds*, respectively.

We set the insulator thickness to a typical value obtained by the flatband voltage measurement of the standard MOS capacitor.

Table 1. Geometrical parameters of MOS-p capacitor in TCAD simulations

Capacitor width: 764 µm
Insulator (Oxide) thickness: 0.5 µm
Silicon bulk thickness: 320 µm
Silicon bulk Impurity concentration: Boron 4.7e12 cm^-3 (p-type 3 kΩcm)
p-layer thickness: 3 µm
Edge smearing: sigma of 0.5 µm

MOS capacitor (standard) – "Flatband voltage measurement" (capacitance measurement with an AC frequency as a function of DC bias voltage between the metal and the backplane) is to estimate the interface charge (*Qif*) and the thickness of the insulator (Fig. 5) [4].

We have a typical measurement (Fig.6) [5], with which we estimate *Qif* being approximately 8e10 / cm².

We have simulated the capacitance with *Qif* of 1e10, 5e10, 1e11, 2e11 /cm² (Fig. 7). The simulation with 5e10 is consistent with the measurement.

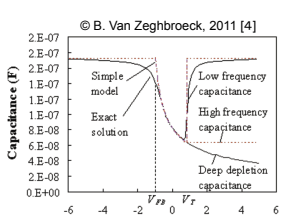

Fig. 5 Typical behavior of the capacitance as a function of DC voltage. A certain negative voltage is required to compensate the attracted charge with the interface charge in the surface of silicon bulk (which voltage is called "Flatband voltage (V_{FB})); over the voltage the silicon surface gets depleted; further above a voltage, creation of *e-h* pairs with the electric field cancels the depletion.

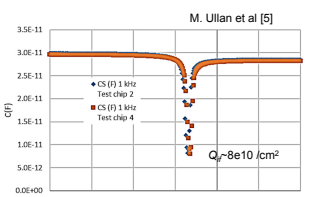

Fig. 6 Typical measurement of "Flatband voltage" with standard MOS capacitor [5].

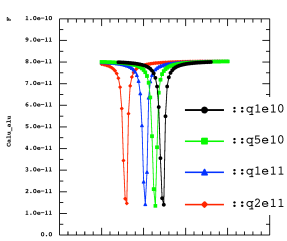

Fig. 7 TCAD simulations of "Flatband voltage" with *Qif* of 1e10, 5e10, 1e11, 2e11 /cm².

Device simulator simulates at thermal equilibrium, i.e., low frequency capacitance. Dynamic response of the charge in the inversion layer to AC voltage is not implemented in the program.

MOS capacitor with p-layer (I) – We have specified the surface density of p-stop structure to be approximately 4e12 cm² [1]. Under an interface charge *Qif* of 1e11 cm², we have simulated the behavior, with the p-layer density *Ds* of 2e12, 4e11, 2e11 cm² (Fig.8). The triangular behavior with 2e12 is consistent with that of the normal batch of VPA37914 (in Fig. 4).

A lower density moves the location of dip towards correct location, however, an order lower density *Ds* of 2e11 cm² is not enough to be consistent with the abnormal one. Lowering the density further does not help; the location of the dip tends to saturate. An increase of the interface charge *Qif* to 3e11 cm² moves the location further lower voltage to be consistent with the abnormal ones.

With these values of the p-density and the interface charge, the shape of the simulations are too sharp.

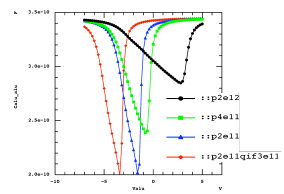

Fig. 8 TCAD simulations of "Flatband voltage measurement" with *Ds* of 2e12, 4e11, 2e11 /cm² (under *Qif* of 1e11 /cm²). An extra is *Ds* of 2e11 (under *Qif* of 3e11 /cm²)

MOS capacitor with p-layer (II) – *"Traps in p-layer"* - the p implantation creates charge traps as radiation damage remnants, which are "annealed" away with temperature treatment in the fabrication process. The traps can be negatively (p-type) or positively (n-type) charged-up sites after absorbing/releasing electrons or holes.

We have introduced charge traps in the p-layer area. Only positive traps (n-type) have affected the behavior. With the introduction, the dips are flattened in the abnormal behavior (red circles). Even in the normal one, the charge traps introduce a kink (red circle) which we observe in the VPA37914 (in Fig. 4). We set the density of the traps not to deviate too much in the normal one.

We have to tune the p density *Ds* a bit, but the relative locations of the dips of normal and abnormal stay the same (Fig.9).

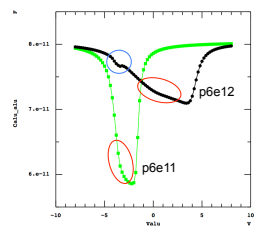

Fig. 9 TCAD simulations of "Flatband voltage measurement" with *Ds* of 6e12 and 6e11 /cm², under *Qif* of 1e11 /cm² and n-type charge traps in the p-layer region, together with the introduction of "setback" of p-layer to the metal area (blue circle).

MOS capacitor with p-layer (III) – We have observed a tiny dip at around -3 V in the normal behavior in Fig. 4. With simulation, this dip (Fig. 8, encircled in blue) is identified being caused by the "setback" of the p-layer to the metal area in reality.

We understand the two factors from the simulation: one is affecting the location and the other the depth of the dip. The former is the p density of the "setback" area, and the latter the wideness of the "setback". We set a smearing of p from the p-layer area with a sigma of 1 µm, otherwise the p density of the "setback" area is that of the silicon bulk. The "setback" is 4.5 µm in layout which results in the ratio of p-layer to metal area being 0.976. A bit smaller ratio of 0.97, which corresponds the setback of 5.5 um, reproduces the depth of the dip better.

MOS capacitor with p-layer (IV) – The introduction of charge traps in the p-layer is not enough to reproduce the "width" of the dip in the abnormal behaviors. For in case, we have introduced a surface contamination with n-type impurity, with the surface density of Null (black), 6e10 (green), 8e10 (blue), and 1e11 (red) cm² (Fig.10).

The location of the dips has moved. The bottom of the dips seems to be flatter, but the widths are stayed similar.

We also observe that the introduction of n-type surface contamination induces very similar effect as the interface charge, as expected.

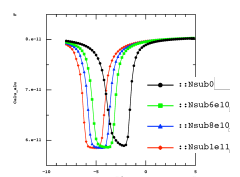

Fig. 10 TCAD simulations of "Flatband voltage measurement" with n-type surface contamination, under *Ds* of 6e11 /cm², and n-type charge traps in the p-layer region.

Discussion – TCAD simulations show that the abnormal behaviors can be reproduced in general with low p-density and charge traps in the p-layer, and interface charge and/or extra surface contamination with n-type impurity. One of the abnormal case with a rather wide width of the dip, however, still requires further investigation.

We have understood that the location and the shape of the dip are affected by the charge in the interface (either interface charge or n-type surface contamination, or both) and p-density. There could be local variation of these factors while we have applied the factors uniformly over the relevant area in the previous sections. We have already tried the possibility but have not reached a reasonable conclusion yet.

The results that we have already obtained imply that there could be issues in the fabrication process such as p-implantation, etching, insulator deposition, heat treatment, and even very local non-uniformity, which are being communicated with the vendor.

Conclusion – We have understood the general behavior of the MOS capacitors, with or without p-layer in the surface of silicon (MOS or MOS-p, respectively) with TCAD simulations. The rare but abnormal behavior of the MOS-p capacitor has been understood with a low p-density (1/10 or less of the specification) and potentially other factors such as interface charge, insufficient heat treatment, and else. The results have helped to make a final decision on the relevant batches with confidence.

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