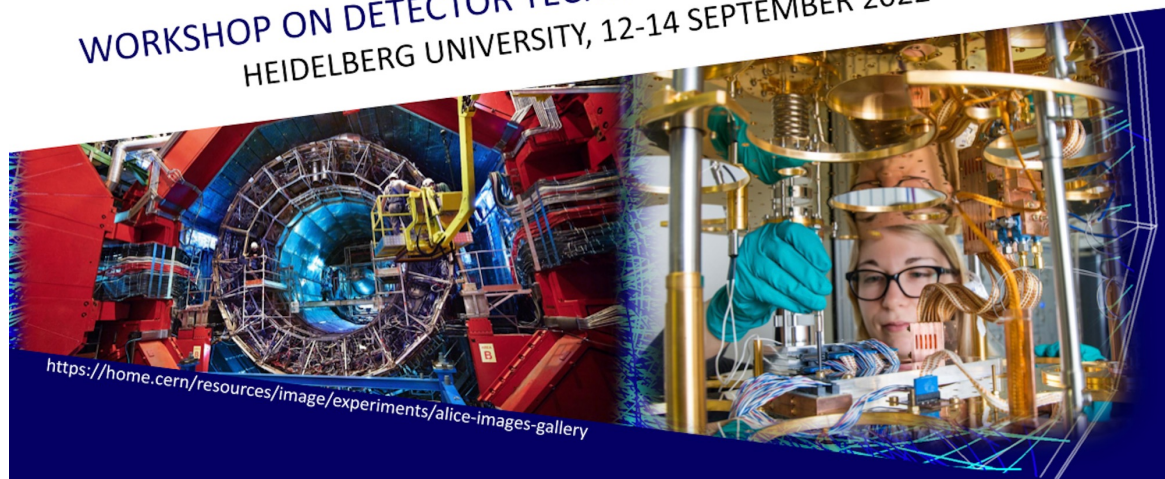


The evolution of the ALICE Inner Tracking System

Stefania Maria Beolé on behalf of the ALICE experiment

VISTAS ON DETECTOR PHYSICS
WORKSHOP ON DETECTOR TECHNOLOGY AND DEVELOPMENT
HEIDELBERG UNIVERSITY, 12-14 SEPTEMBER 2022



The ALICE experiment



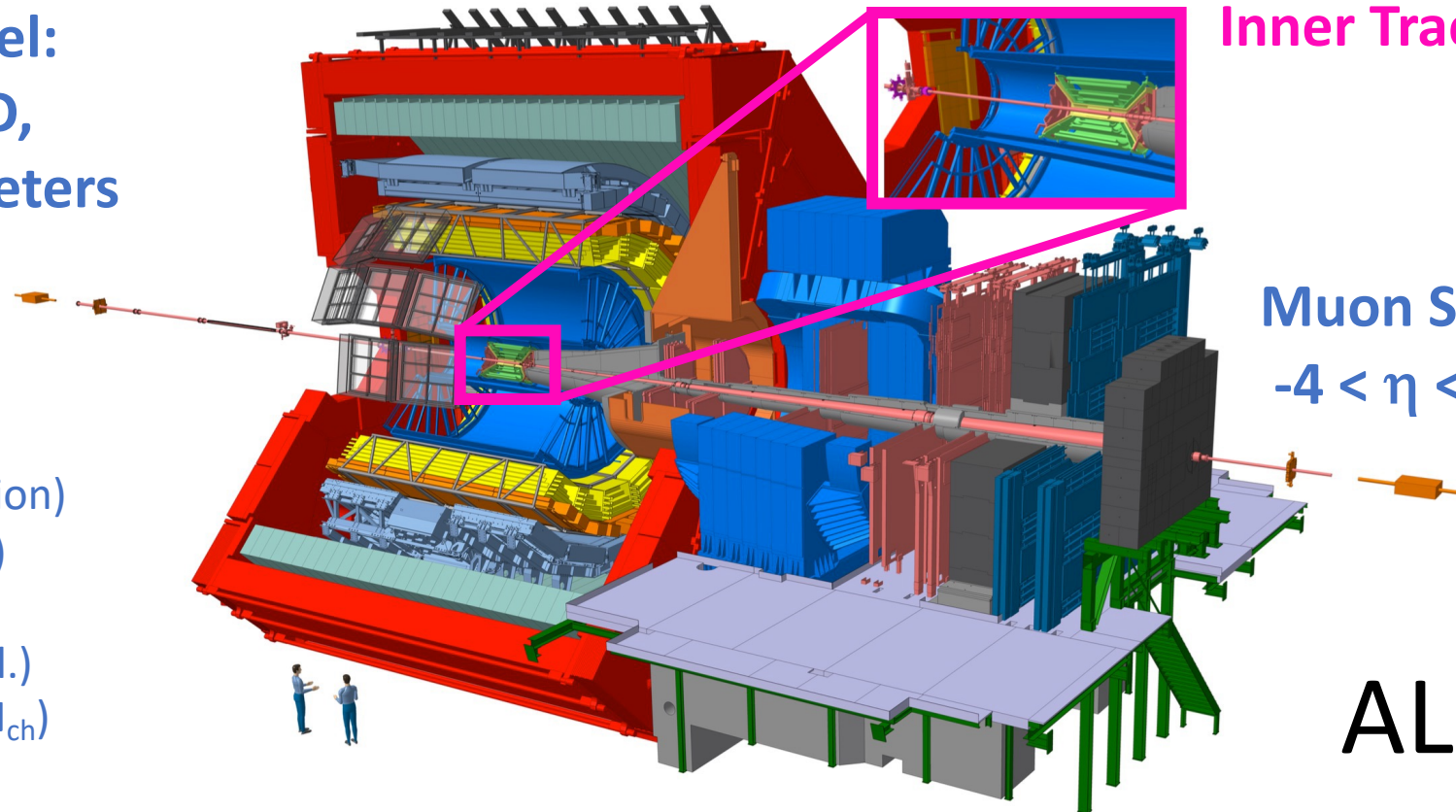
- ALICE is the experiment at the LHC specifically designed for studying heavy ion collisions
- The main goal is exploring the deconfined phase of QCD matter → quark-gluon plasma

LHC Pb-Pb → large energy density ($> 15 \text{ GeV}/\text{fm}^3$) & large volume ($\sim 5000 \text{ fm}^3$)

Central Barrel:
Tracking, PID,
EM-Calorimeters
 $|\eta| < 0.9$

Inner Tracking System

Muon Spectrometer
 $-4 < \eta < -2.5$



ALICE 1

ACORDE (cosmics)

Forward detectors:

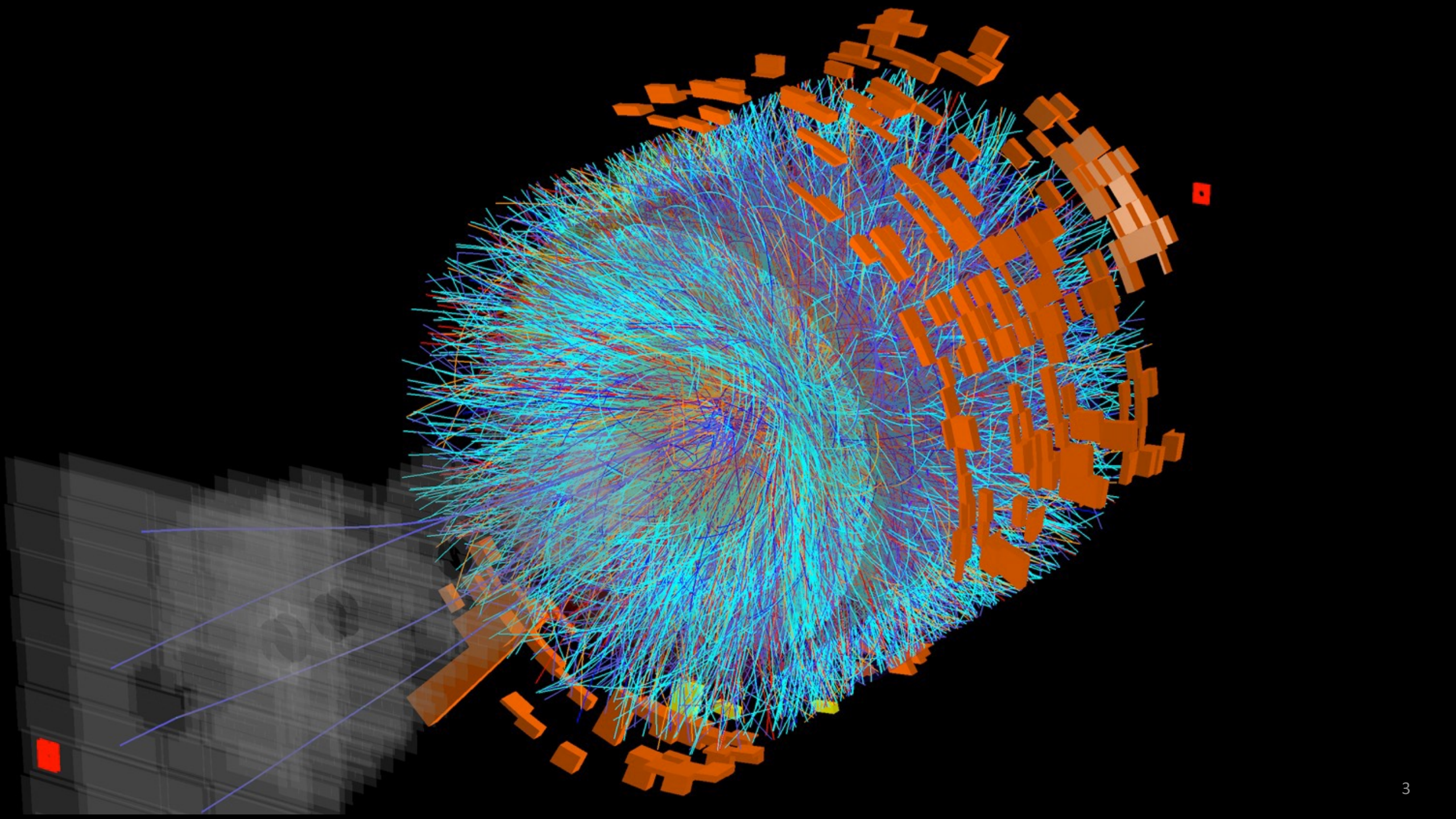
AD (diffraction selection)

V0 (trigger, centrality)

T0 (timing, lumi)

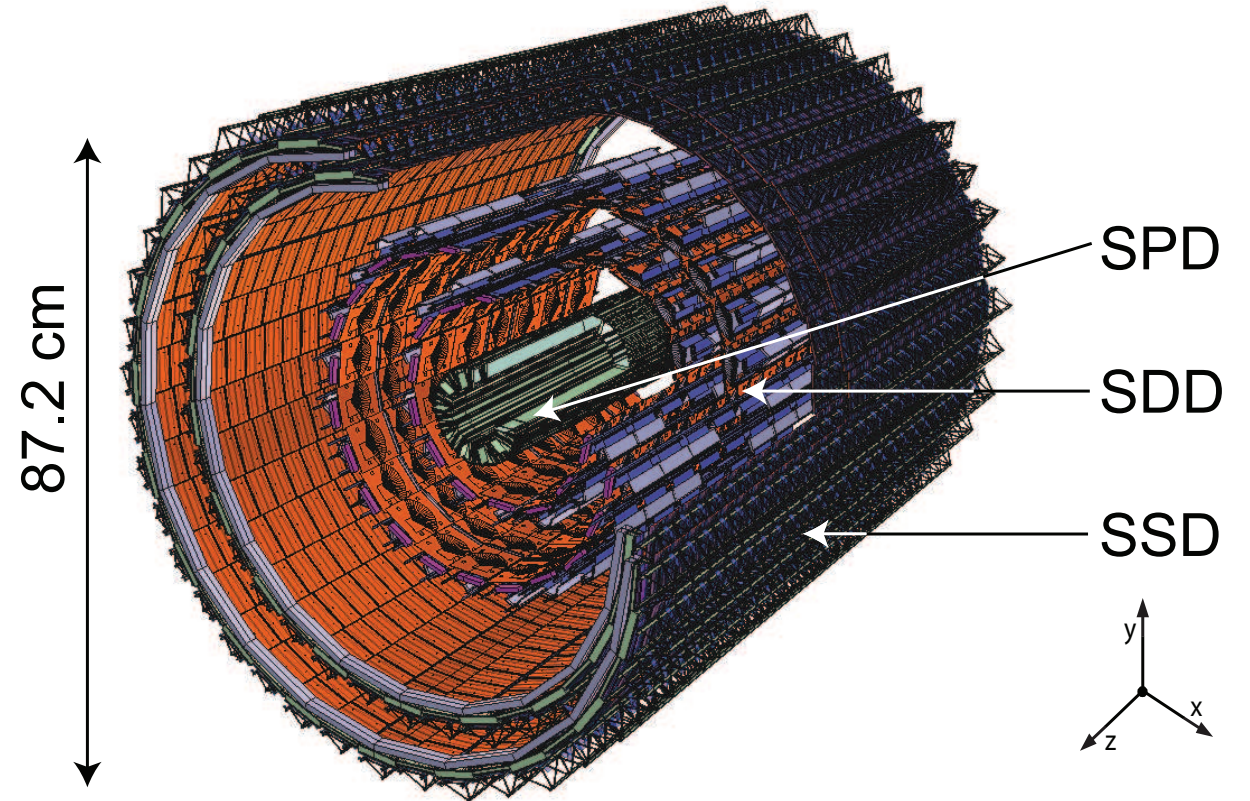
ZDC (centrality, ev. sel.)

FMD (N_{ch}) PMD (N_{γ} , N_{ch})



The first Inner Tracking System: ITS1

- Inner Tracking System goals:
 - improve primary vertex reconstruction, momentum and angular resolution of tracks from outer detectors
 - Secondary vertex reconstruction (c, b decay) with high resolution
 - Tracking and PID of low p_T particles, also in stand-alone mode
- Detector features
 - Capability to handle high particle density
 - Good spatial precision
 - Minimize distance of the innermost layer from beam axis
 - Limited material budget
 - Analogue information for particle identification via dE/dx (outermost 4 layers)
- **Main limitation: low readout rate capability (1kHz)**



3 different technologies

1. 2 layers of Silicon Pixel Detector (SPD)
2. 2 layers of Silicon Drift Detector (SDD)
3. 2 layers of double side Silicon Strip Detector (SSD)

ALICE Upgrades in LS2



Motivation:

High-precision measurements of rare probes at low transverse momentum

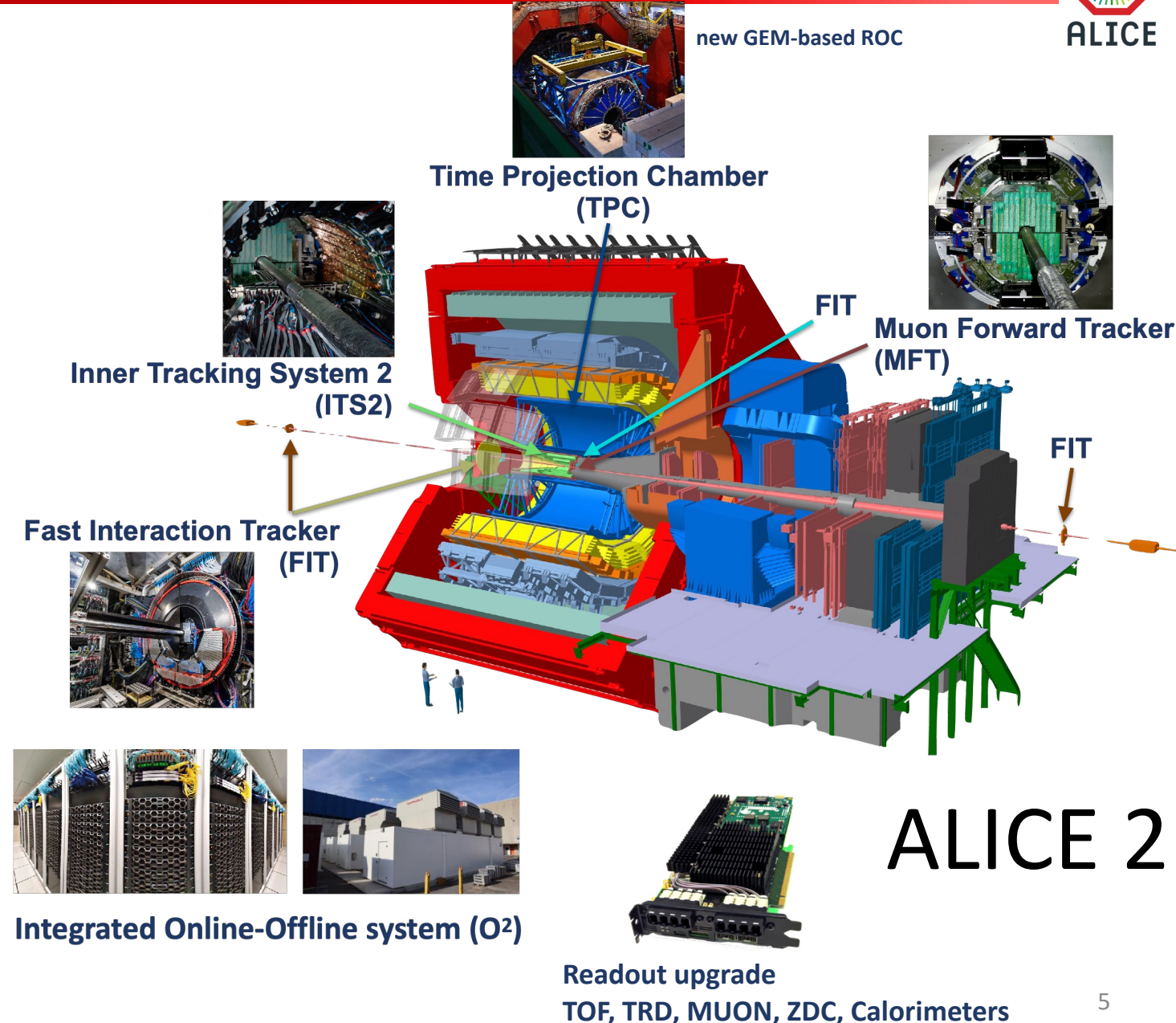
- Cannot be selected by hardware trigger
- Need to record large minimum-bias data sample: read out all Pb-Pb interactions up to the maximum collision rate of 50 kHz

Goal:

- Pb-Pb integrated luminosity 13 nb^{-1} (plus pp, pA and O-O data)
 - > **Gain factor 100 in statistics for min bias sample w.r.t. runs 1+2**
- **Improve vertex reconstruction and tracking capabilities**

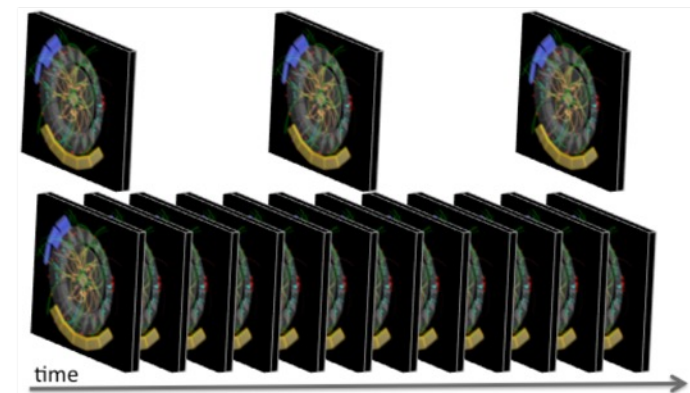
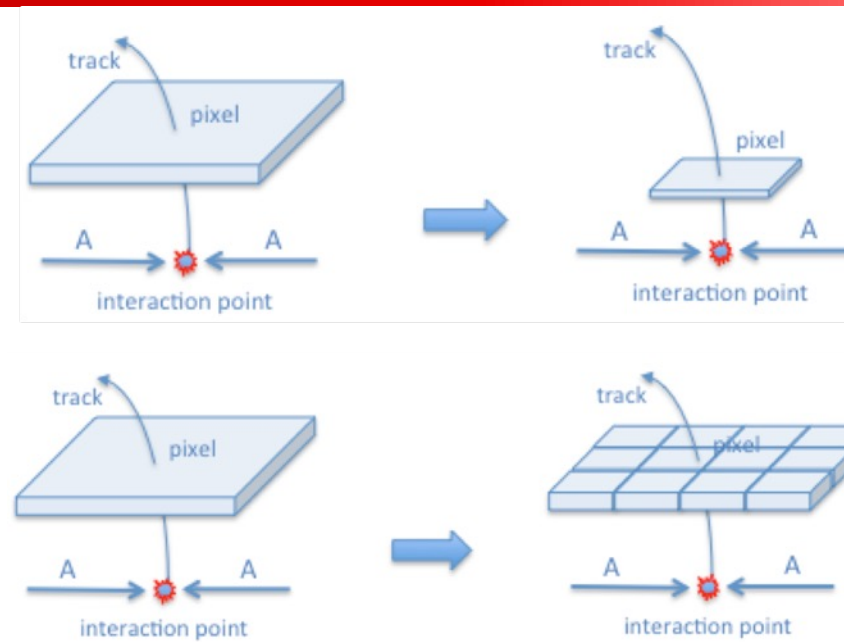
Strategy:

- new ITS, MFT, FIT, TPC ROC
- update FEE of most detectors
- new integrated Online-Offline system (O^2)



ITS2 Design Objectives

- **Improve impact parameter resolution** by factor ~ 3 in $r\phi$ and factor ~ 5 in z at $p_T = 500$ MeV/c
 - Get closer to Interaction Point: 39 mm \rightarrow 23 mm
 - Reduce material budget: $1.14\% X_0 \rightarrow 0.35\% X_0$ (inner layers)
 - Reduce pixel size: $50 \times 425 \mu\text{m}^2 \rightarrow \sim 30 \times 30 \mu\text{m}^2$
- **Improve tracking efficiency and p_T resolution at low p_T**
 - Increase number of track points: $6 \rightarrow 7$ layers
- **Fast readout**
 - Readout of Pb-Pb collisions at 50 kHz (ITS1: 1 kHz) and p-p at 400 kHz



ITS2 pixel chip: ALPIDE Monolithic Pixel Sensor

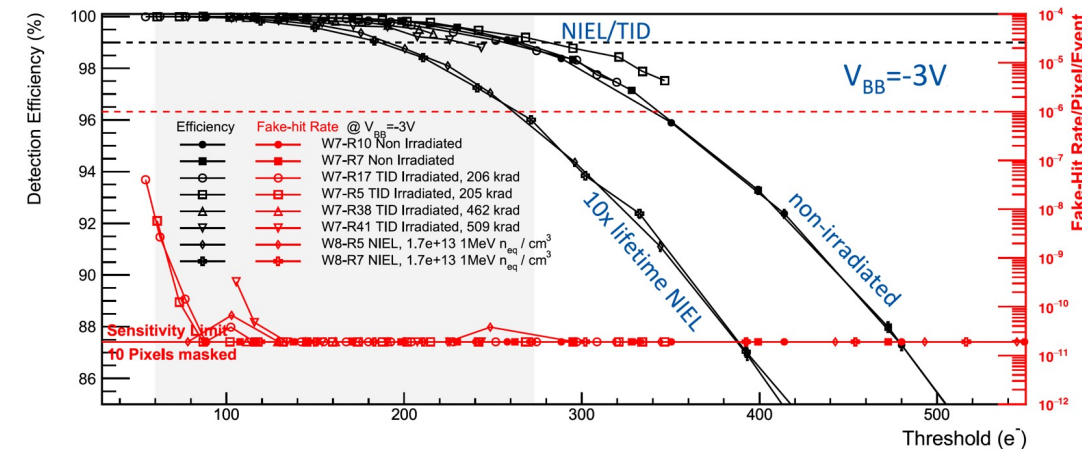
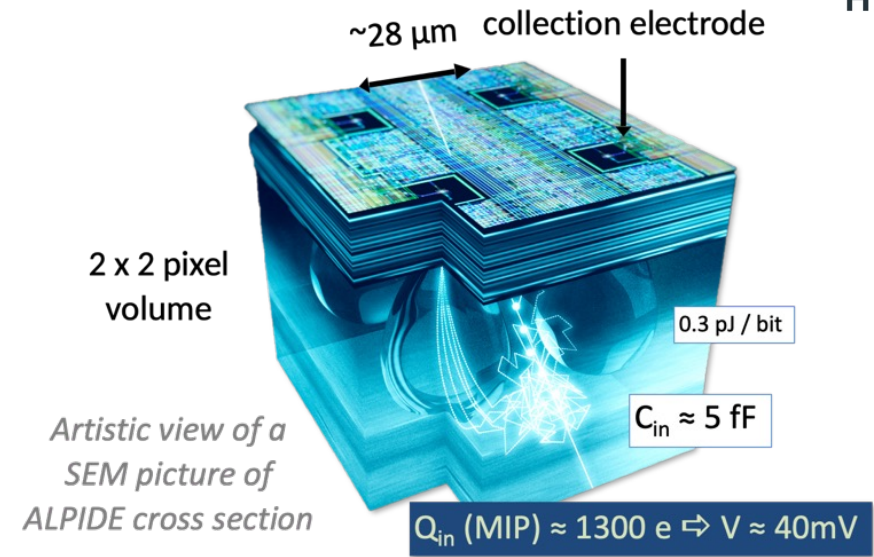


CMOS Pixel Sensor – Tower Semiconductor 180nm CMOS Imaging Sensor (CIS) Process

ALPIDE Key Features

- In-pixel: Amplification, Discrimination, multi event buffer
- In-matrix zero suppression: priority encoding
- Ultra-low power <math>< 40\text{mW}/\text{cm}^2</math> (<math>< 140\text{mW}</math> full chip)
- Detection efficiency > 99%
- Spatial resolution $\sim 5\mu\text{m}$
- Low fake-hit rate: $\ll 10^{-6}/\text{pixel}/\text{event}$ ($10^{-8}/\text{pixel}/\text{event}$ measured during commissioning)
- Radiation tolerance: 270 krad (TID), $> 1.7 \cdot 10^{13}$ 1MeV/n_{eq} (NIEL)

Same chip used for ITS and Muon Forward Tracker (MFT)



ALPIDE detection efficiency and fake hit rate

ALPIDE and other developments



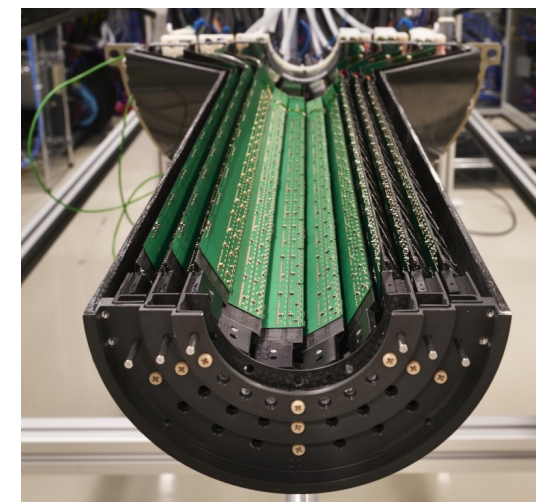
ALICE



ALPIDE: Tower Semiconductor 180nm CMOS Imaging Sensor (CIS) Process

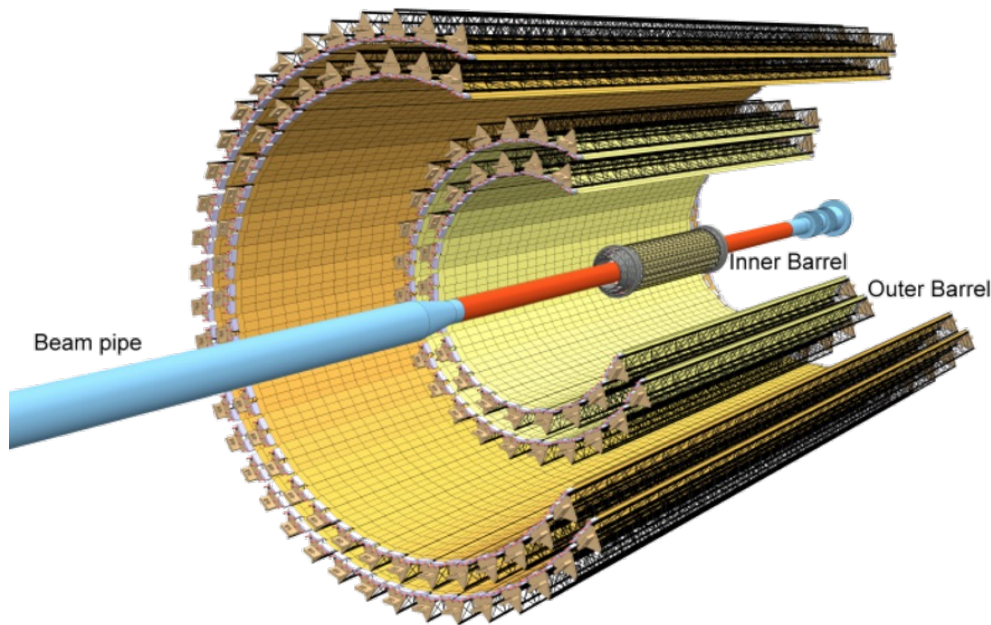
- R&D effort within the ALICE collaboration
 - excellent collaboration with foundry
 - **more than 70k chips produced and tested**
 - ALICE ITS pioneers large area trackers built of MAPS (EIC, ALICE 3, FCC?)
- in parallel studies to optimise process to reach full depletion and improve time response and radiation hardness up to 10^{15} 1MeV/n_{eq} :
 - **More details:** NIM A871 (2017)
<https://doi.org/10.1016/j.nima.2017.07.046>
 - **Now being further pursued: MALTA, CLICpix, FastPix, ...**

ITS2 Inner Barrel

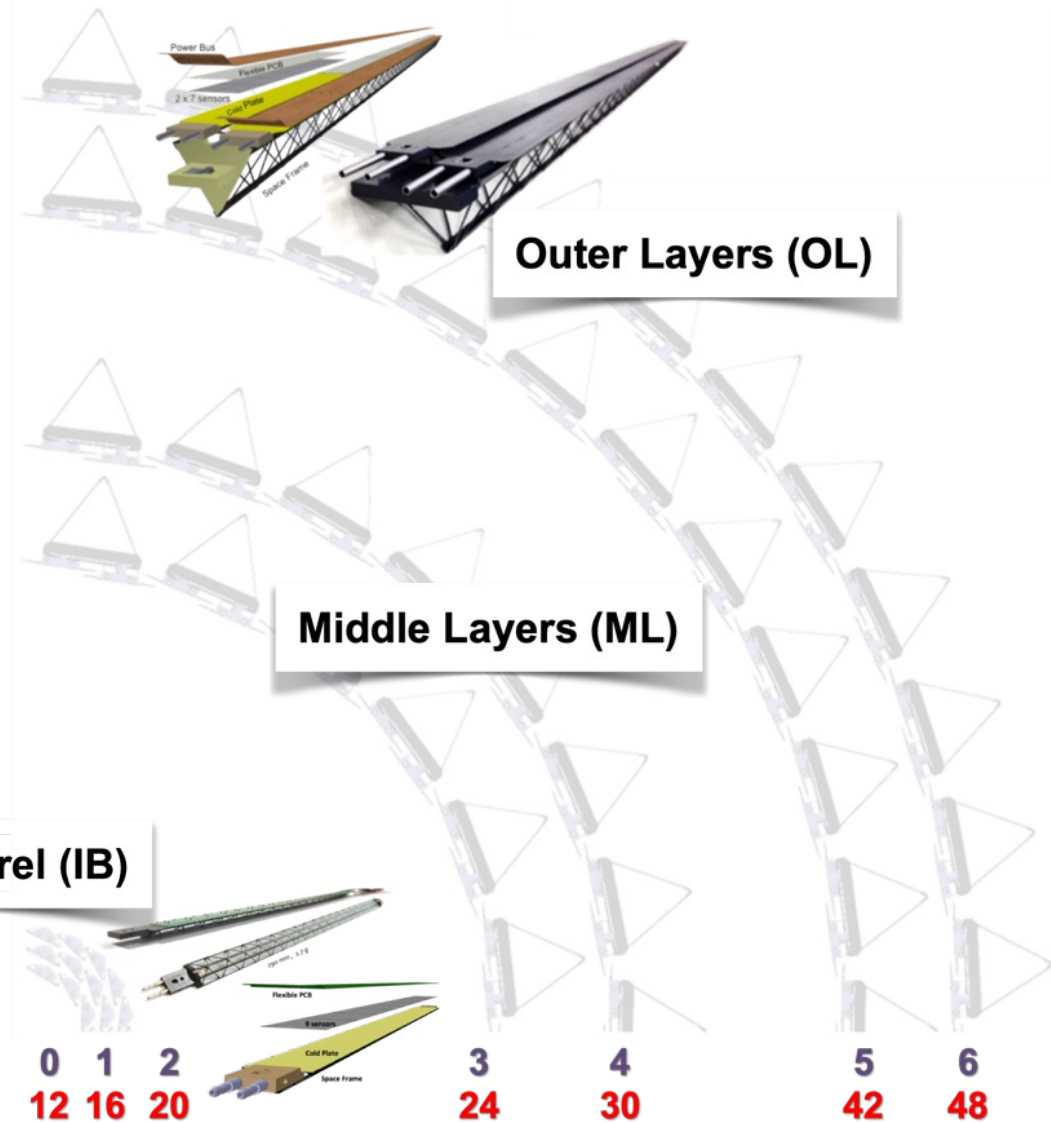


ITS2 Layout

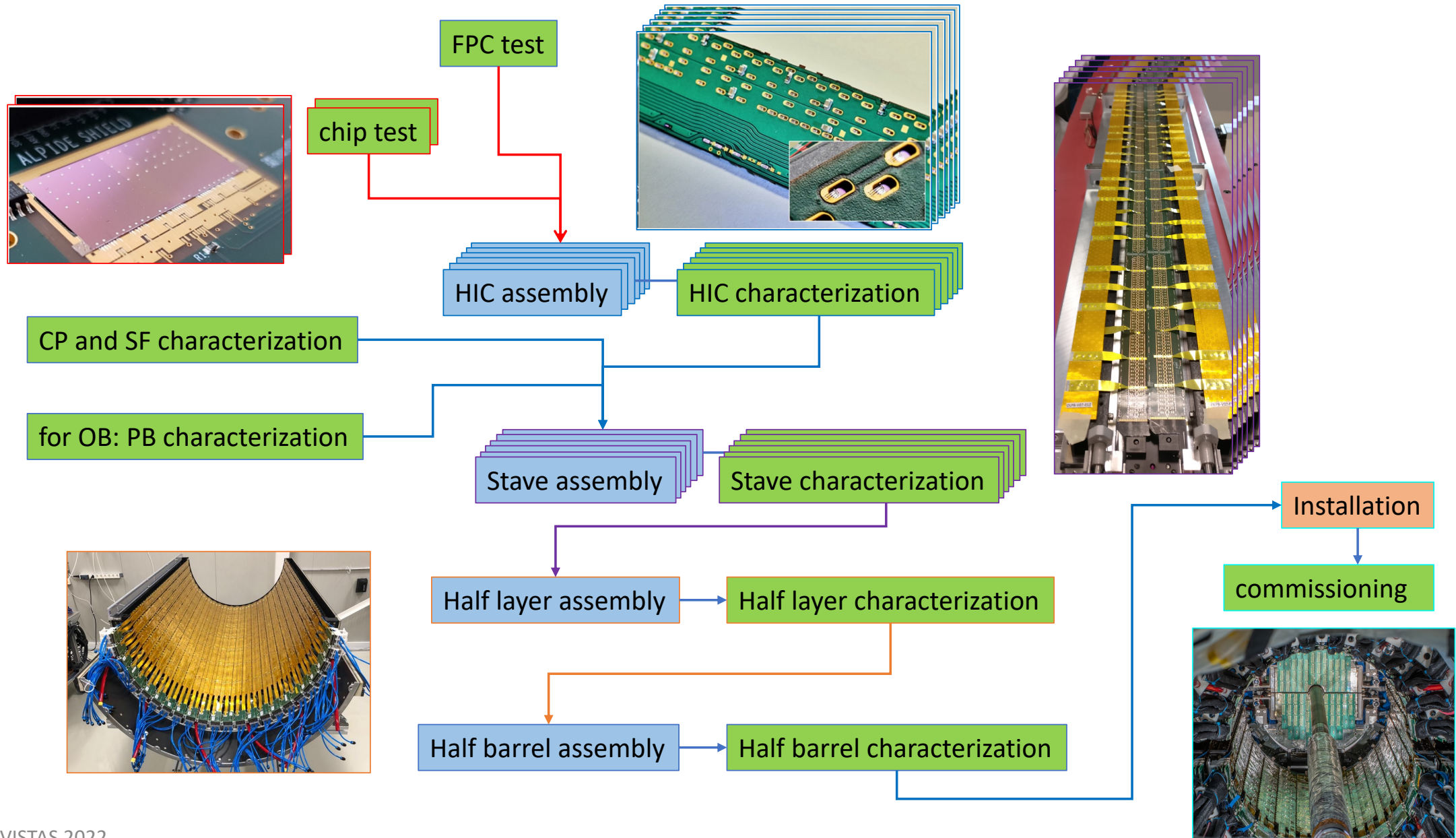
- 7 Layers (3 inner / 2 middle / 2 outer) from R = 22 mm to R = 400 mm
- 192 Staves (48 IL / 54 ML / 90 OL)
- Ultra-lightweight support structure and cooling
- 10 m² active silicon area, 12.5 x 10⁹ pixels



**Outer Barrel (OB)
= ML + OL**

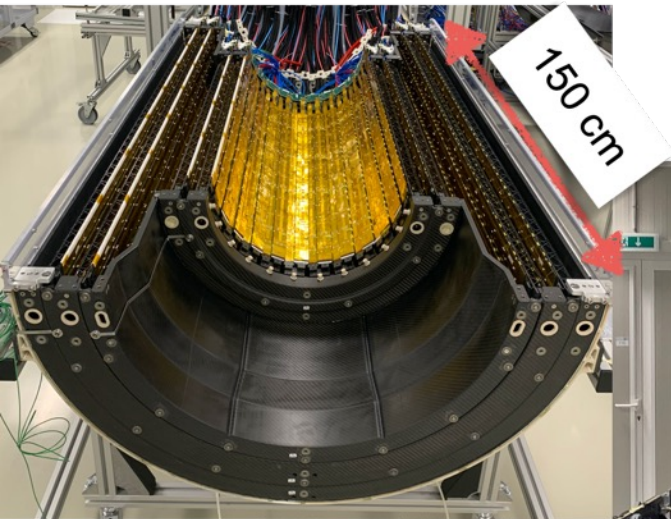


ITS components production workflow

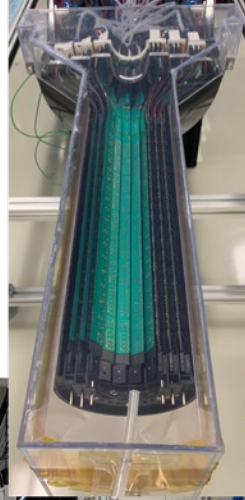


On-Surface Commissioning

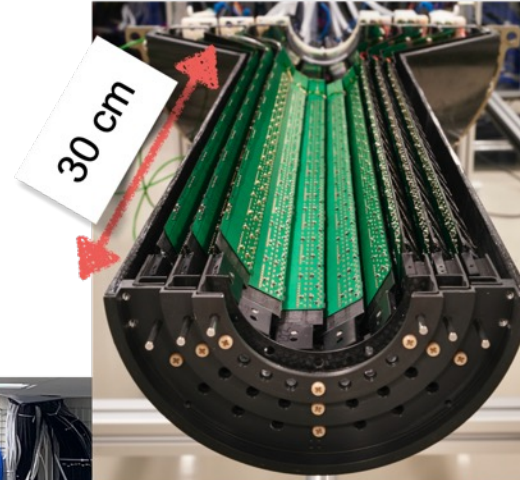
Outer Barrel Top



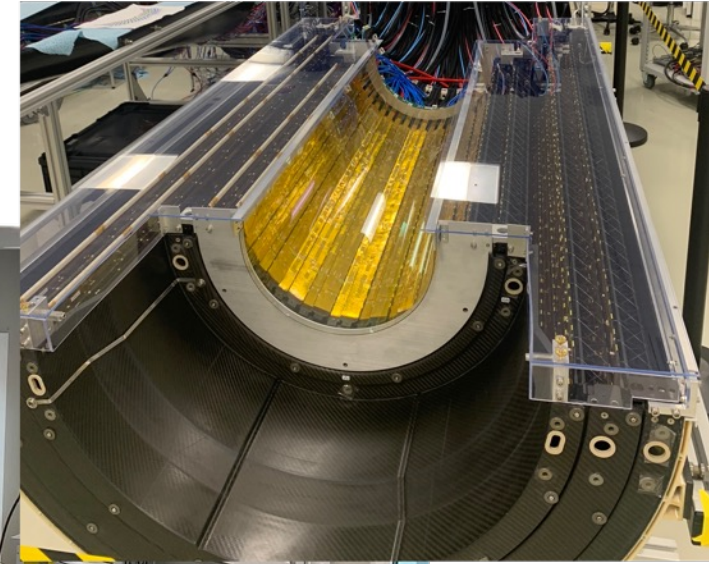
Inner Barrel Top



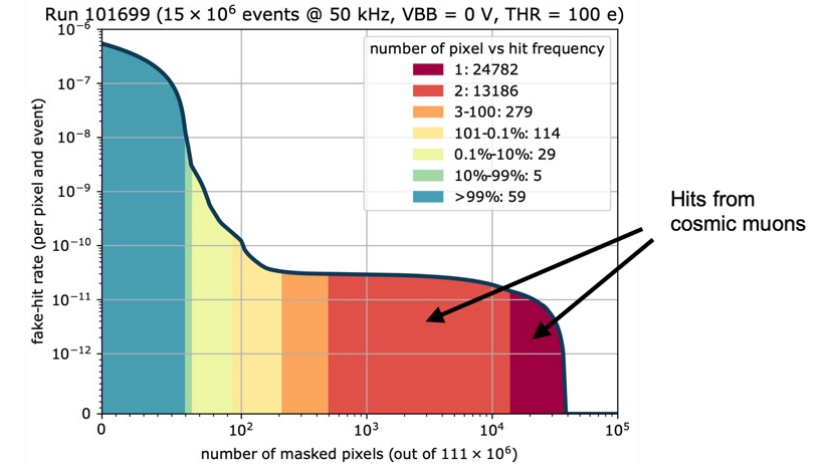
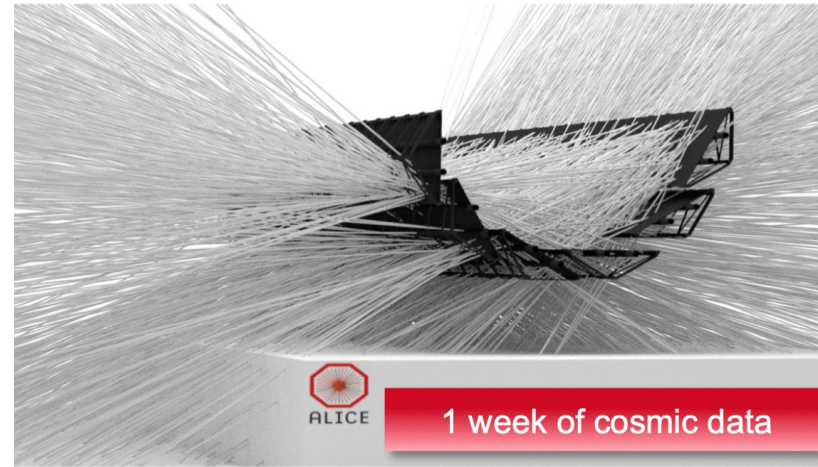
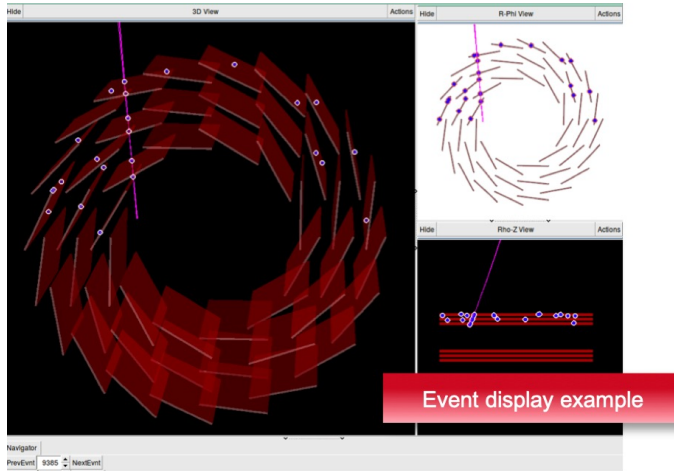
Inner Barrel Bottom



Outer Barrel Bottom

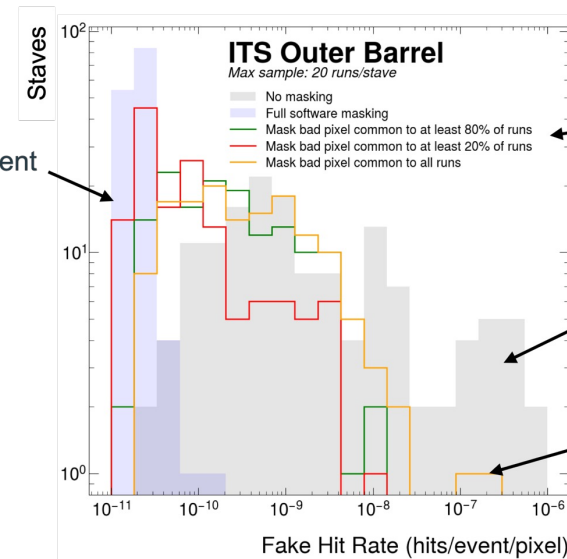


On-Surface Commissioning results



- Cosmics tracks reconstructed
- IB: fake-hit rate of 10^{-10} / pixel / event
 - Achieved by masking fraction of 10^{-8} pixels
- OB: fake-hit rate of 10^{-8} / pixel / event
 - Achieved by masking noisy pixels common to all runs
- Bit-error-free data transmission for several tens of hours at nominal operating conditions
 - Large operational margin in terms of occupancy and readout rate
 - Regular errors for extreme combinations of occupancy and trigger rate lead to negligible inefficiency ($\sim 1/s$ for full IB)

Offline masking:
FHR 10^{-10} / pixel / event

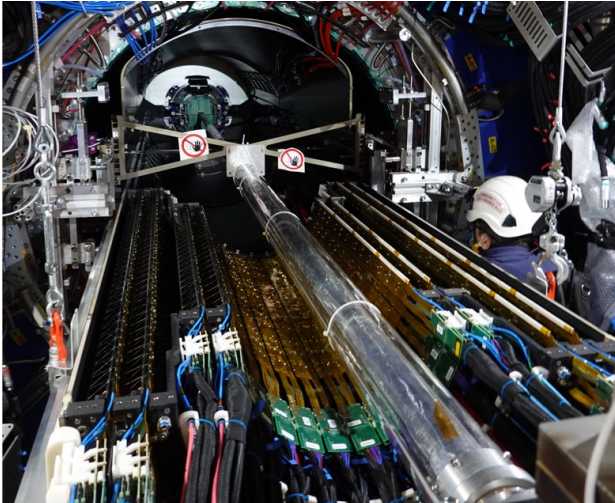


Requirement:
 10^{-6} / pixel / event

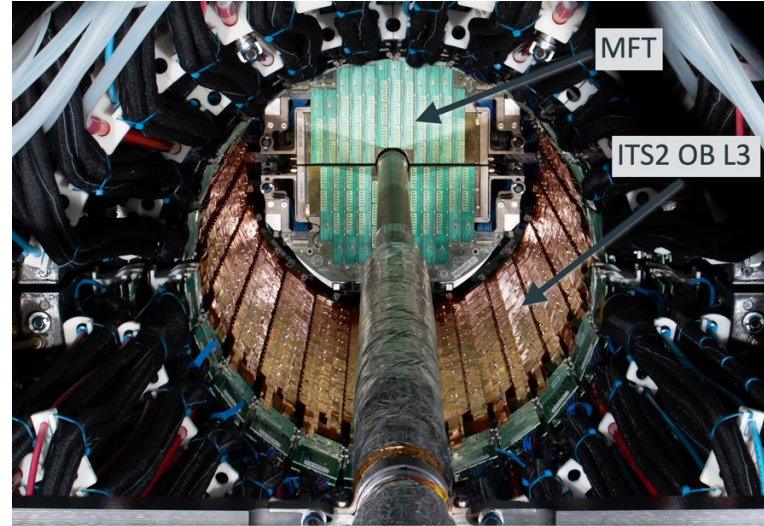
Exclusion of broken double-columns

Masking noisy pixels common to all runs
→ realistic estimate for hardware masking

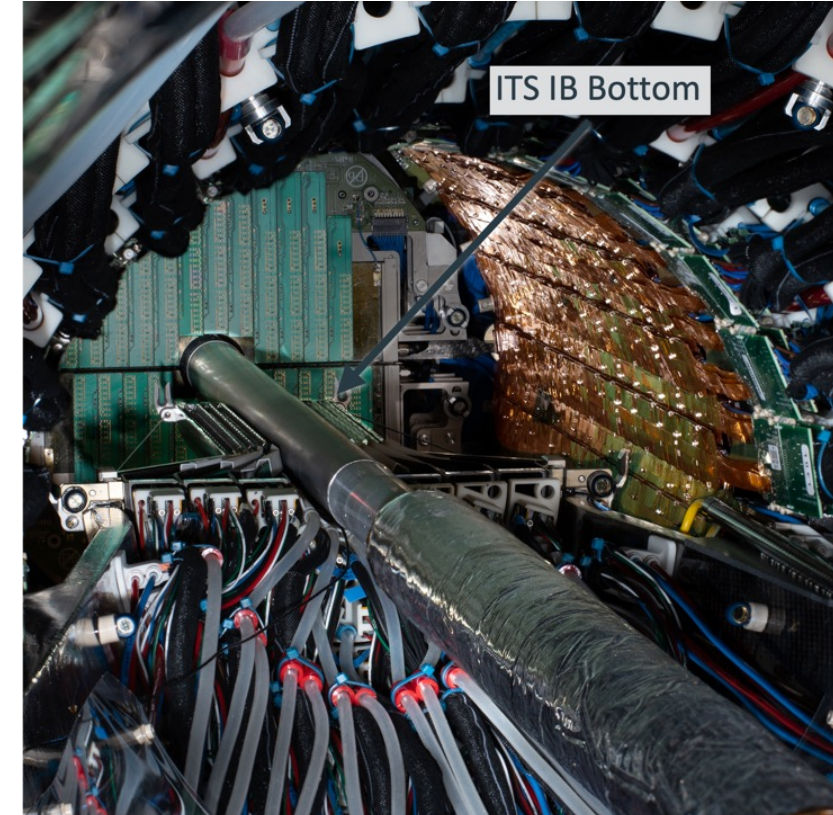
Excellent Fake-Hit Rate (FHR) in the entire OB



Outer Barrel Bottom being inserted on the rails inside the TPC



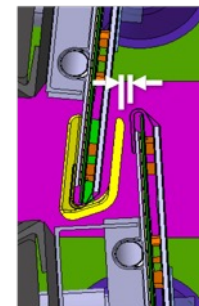
ITS Outer Barrel surrounding the beam pipe, MFT in the back



ITS Inner Barrel Bottom and Outer Barrel

- Installation challenges
 - Precise positioning around the beam pipe (nominal clearance ~ 2 mm)
 - Manipulating from 4 m distance
 - Difficult to see actual position by eye
 - precise mating of top and bottom barrel halves (clearance between adjacent staves ~ 1.2 mm)
- Dry-installation tests on the surface to test and exercise procedures
- Use of 3D scans, surveys and cameras

1.2 mm
nominal
clearance



OB stave edge clearance when fully mated

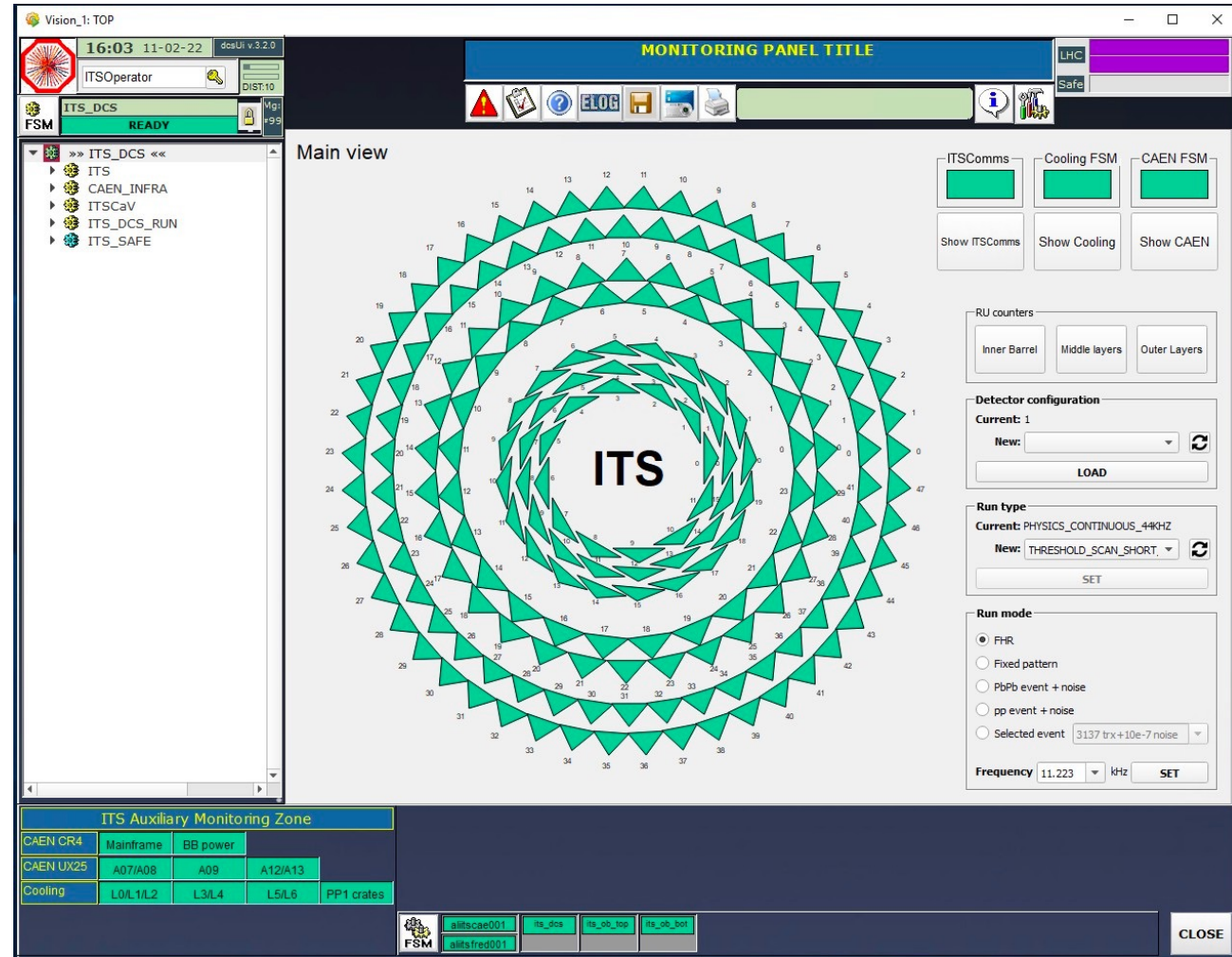
Detector Control System



ALICE

- DCS ready to control detector in all phases of operation:
 - Controls and configures pixel chips and entire infrastructure
 - Error recovery during a run to continue running with minimal data loss
 - Detector functionality implemented in C++ library (pixel chips, readout cards, regulator boards)
 - GUI, FSM and alarms in Siemens WinCC OA
 - fully integrated into ALICE DCS

- Routinely used during commissioning and Pilot Beams



The Challenge:

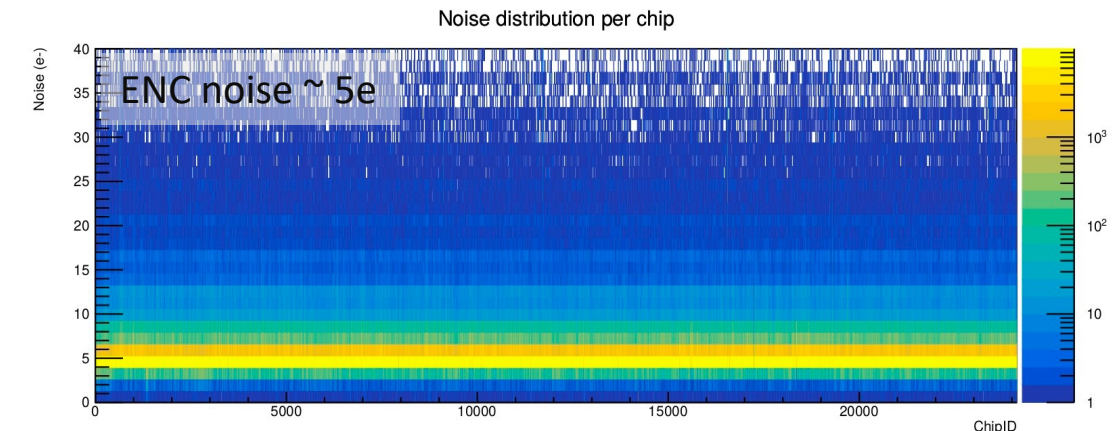
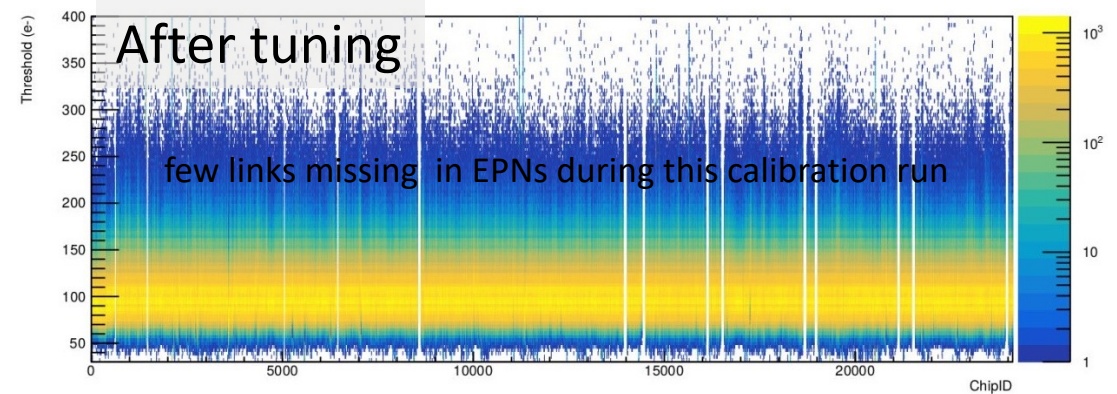
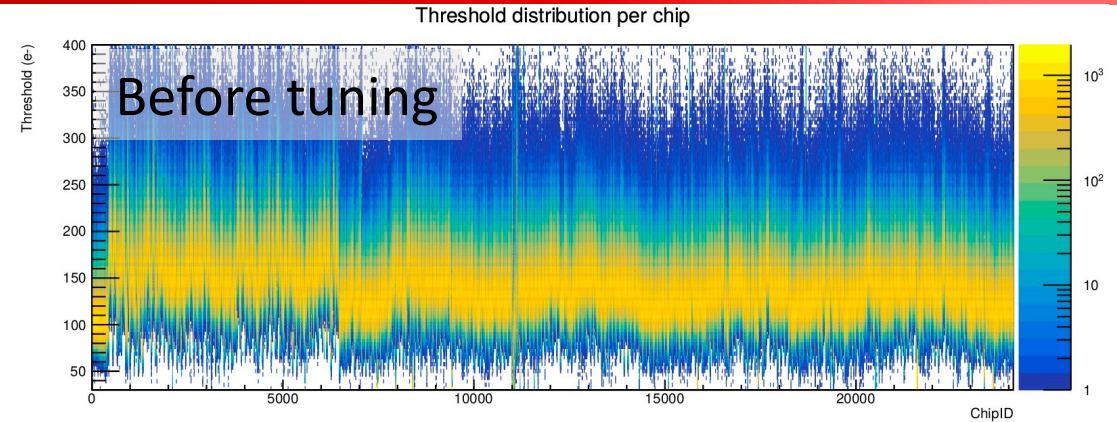
- Online calibration of **12.5 billion channels**
- Threshold scan of full detector: **> 50 TB of event data**
- Several scans to be run sequentially
 - Threshold tuning (adjust thresholds to target)
 - Threshold scan (measure actual thresholds)

Procedure:

- DCS performs actual scans: configure and trigger test injections
- Scan runs in parallel but independently on all staves
- Distributed analysis on event processing nodes
- full procedure takes **less than 30 minutes**

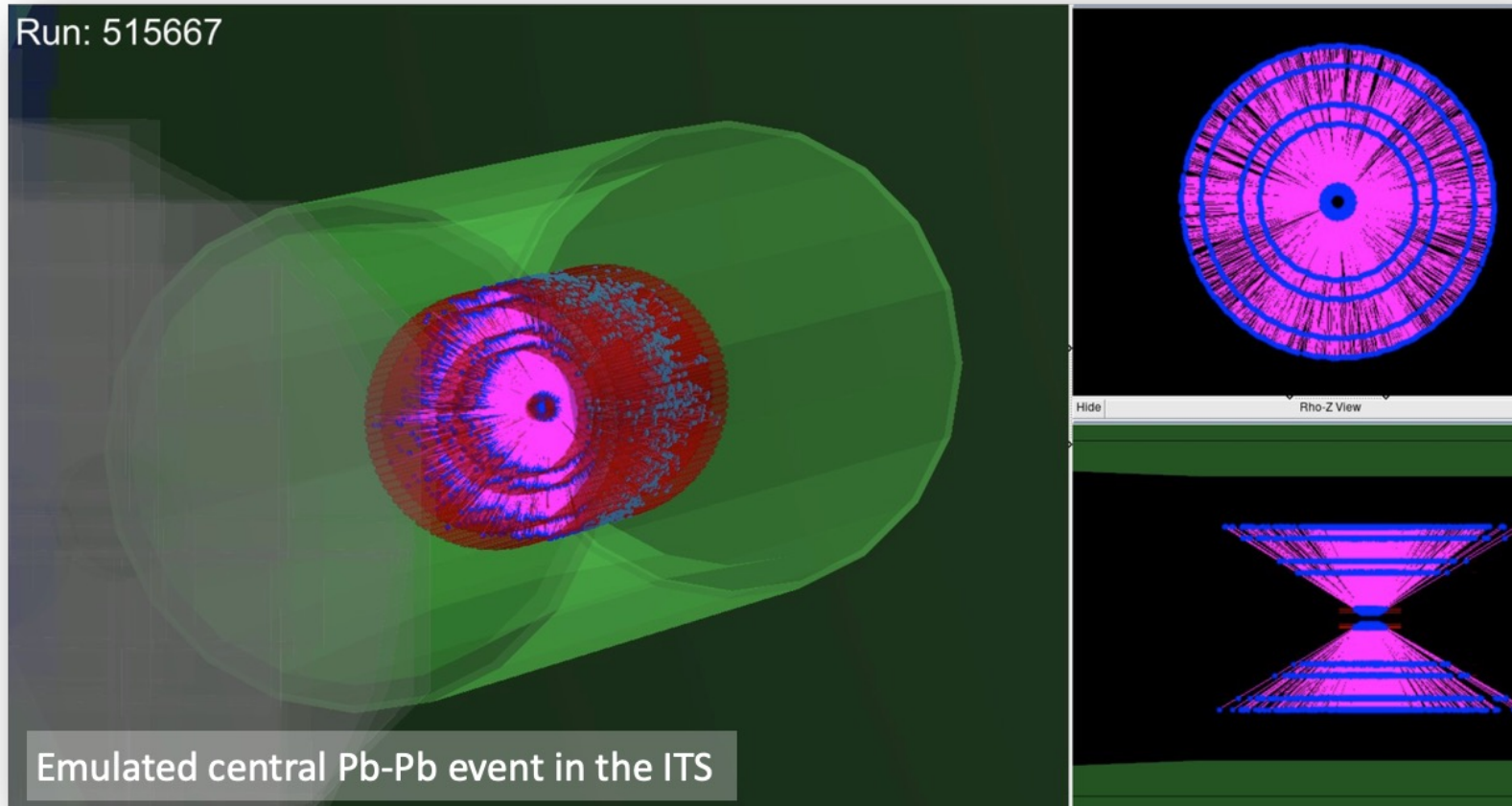
Results:

- Scan with **online analysis** successfully run on full detector
- before tuning: settings used in surface commissioning, **detector already fully efficient**
- After tuning: **Thresholds very stable on all the chips: RMS of threshold distribution** compatible with what we had during production
- ENC noise $\sim 5e^-$



Data Taking Preparation

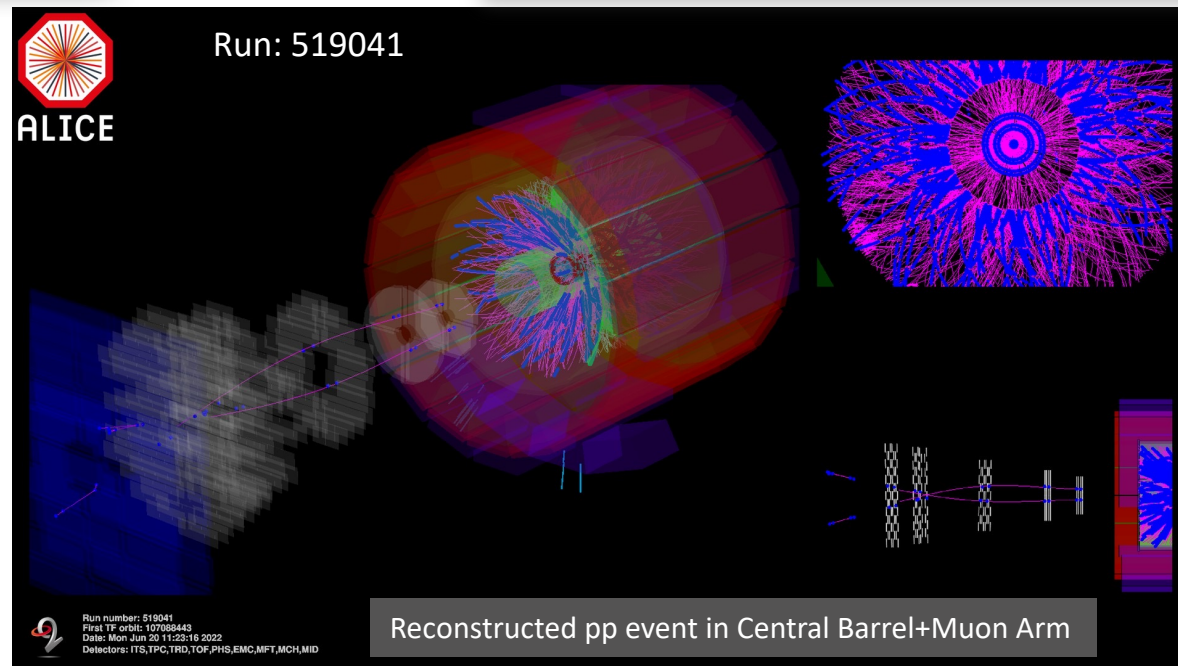
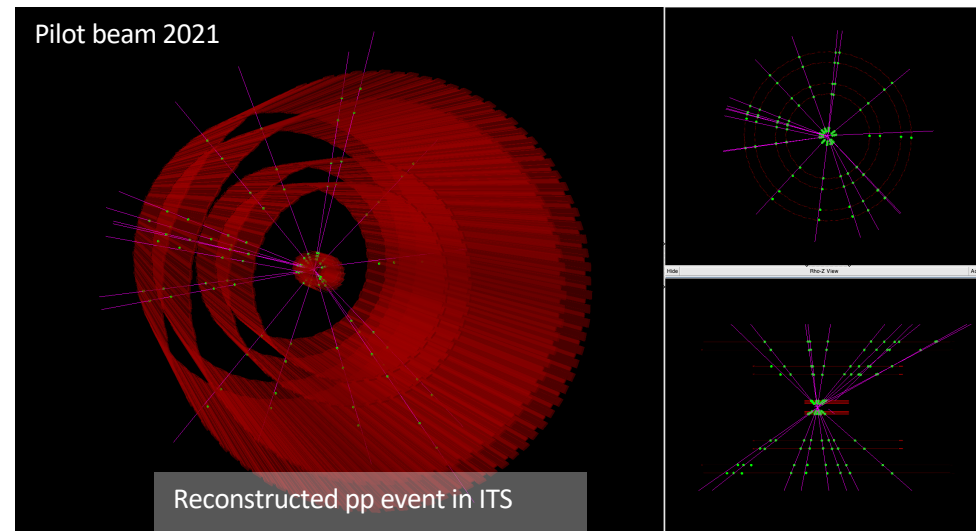
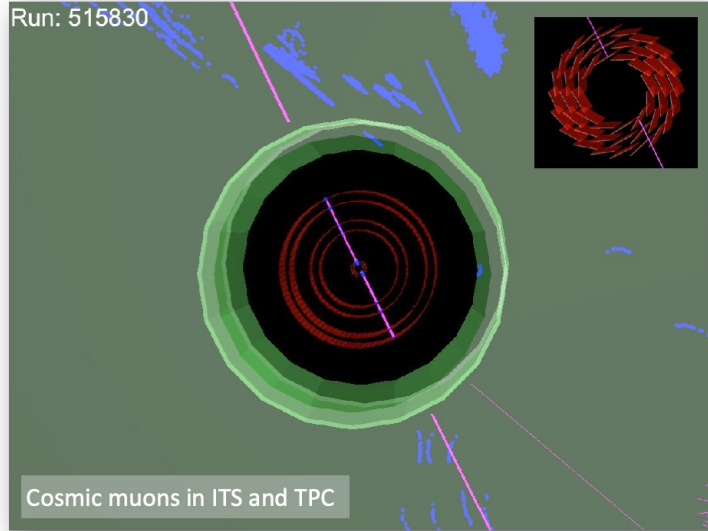
- Last part of commissioning phase devoted to prepare and test settings optimized for pp with 200 kHz framing rate (instead of 45 kHz for Pb-Pb) to achieve better time resolution reducing pile-up
 - successfully tested tested in pp Pilot Beam (2022)
- Extensive test runs with emulated Pb-Pb and pp events (injected into the detector front-end) to test detector, processing chain under realistic load



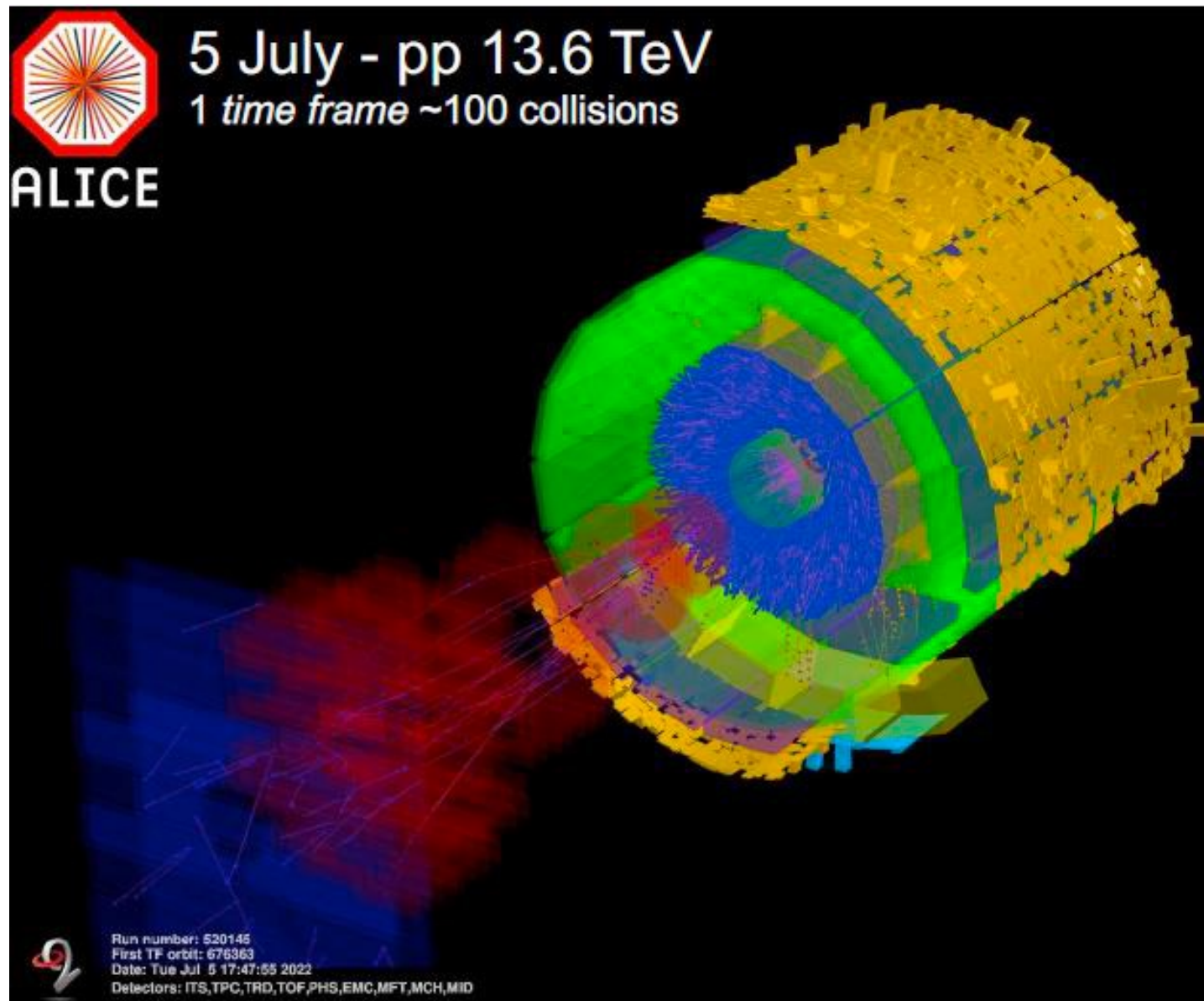
RUN 3 readiness



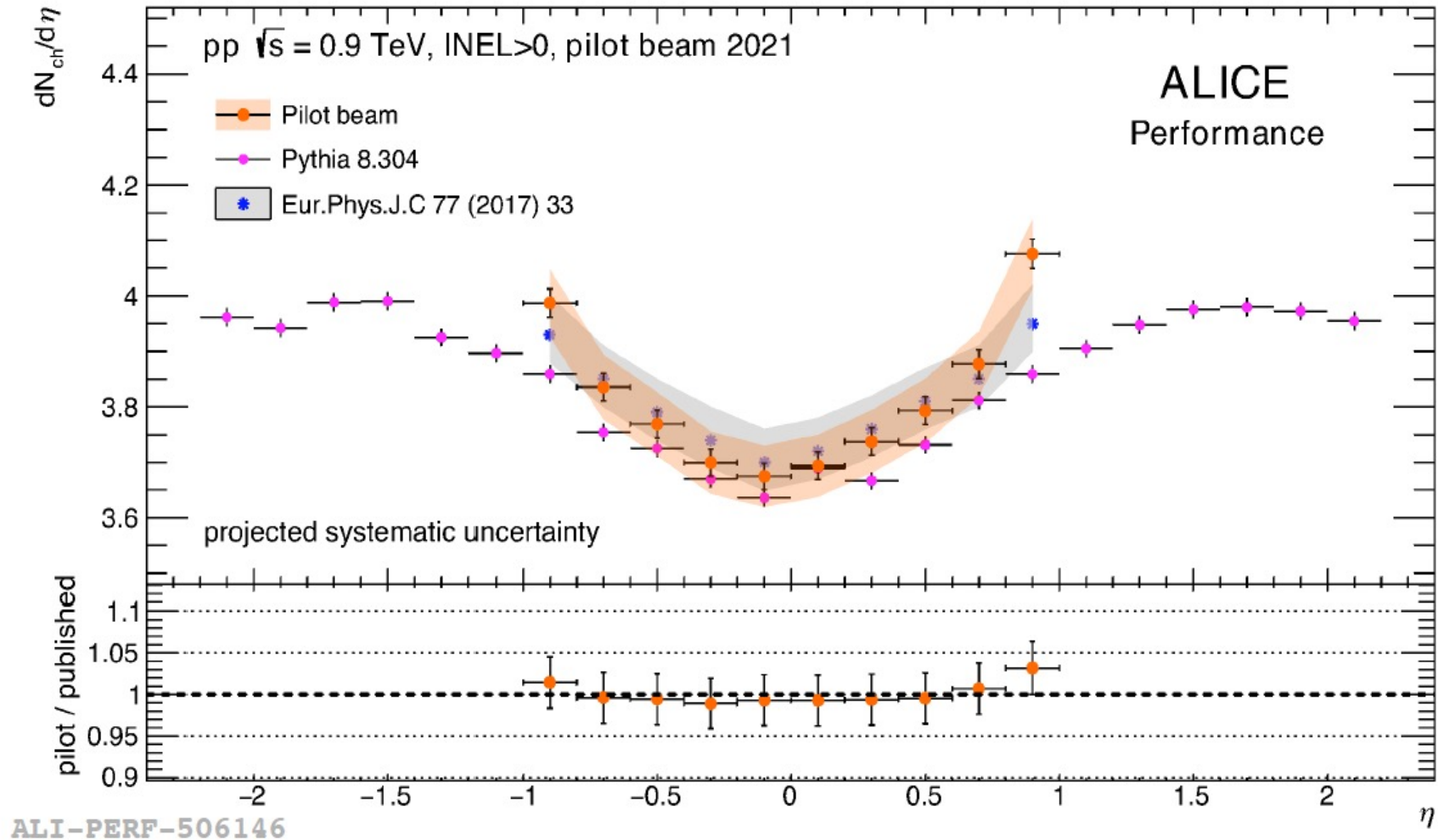
ALICE



RUN 3 data taking: high intensity pp beam



First physics results



Corrected pseudo-rapidity distribution for charged tracks measured in the pilot beam compared to published ALICE data and Pythia 8 simulation

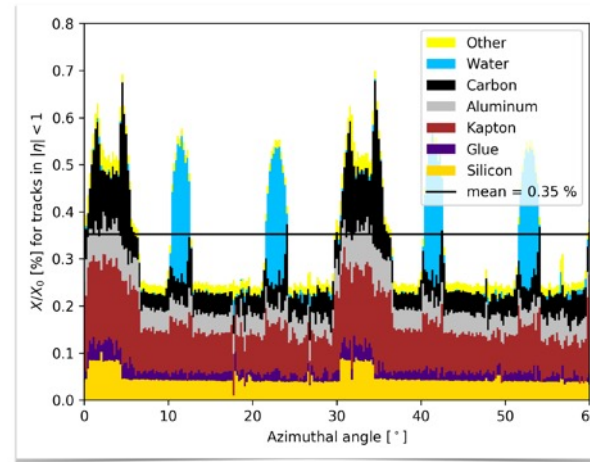
ALICE 2.1: ITS3

ALICE 2.1: ITS3 all silicon detector

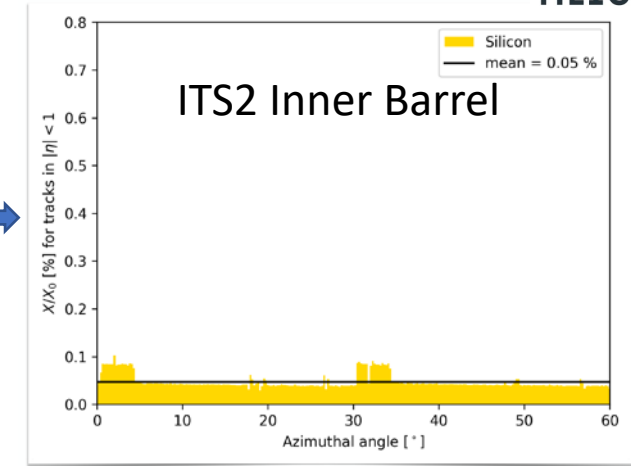


ALICE

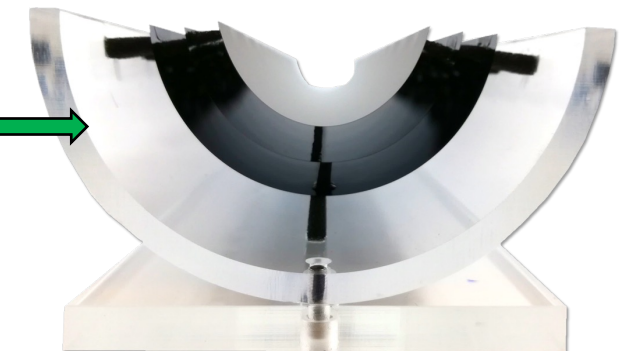
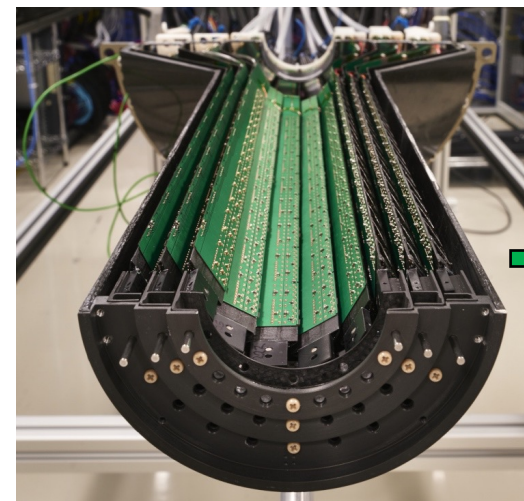
- Goal: improve determination of primary and secondary vertices at high rate
- Layout: 3 layers, replace ITS Inner Barrel,
 - beam pipe: smaller inner radius (18.2 mm to 16 mm) and reduced thickness (800 μm to 500 μm)
 - innermost layer: mounted around the beam pipe, radius 18mm (was 22 mm)
- Technology choices:
 - 65 nm CIS of Tower & Partners Semiconductor (TPSCo):
 - larger wafers: 300 mm instead of 200 mm,
 - single “chip” equips an ITS3 half-layer (through stitching technology)
 - 6 sensors in total
 - thinned down to 20-40 μm
 - -> flexible
 - bent to target radii
 - mechanically held by carbon foam ribs with low density and high thermal conductivity



ITS2 Layer 0: $X/X_0=0.35$

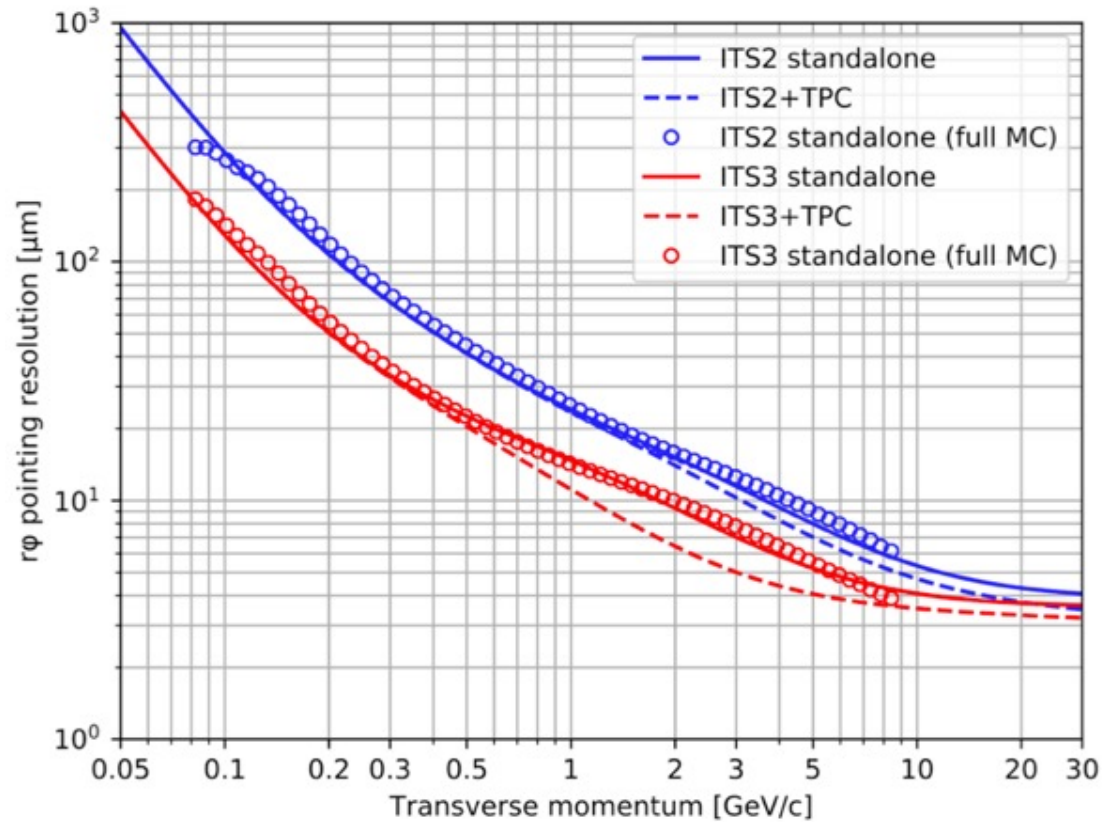


ITS3 only silicon: $X/X_0=0.05$



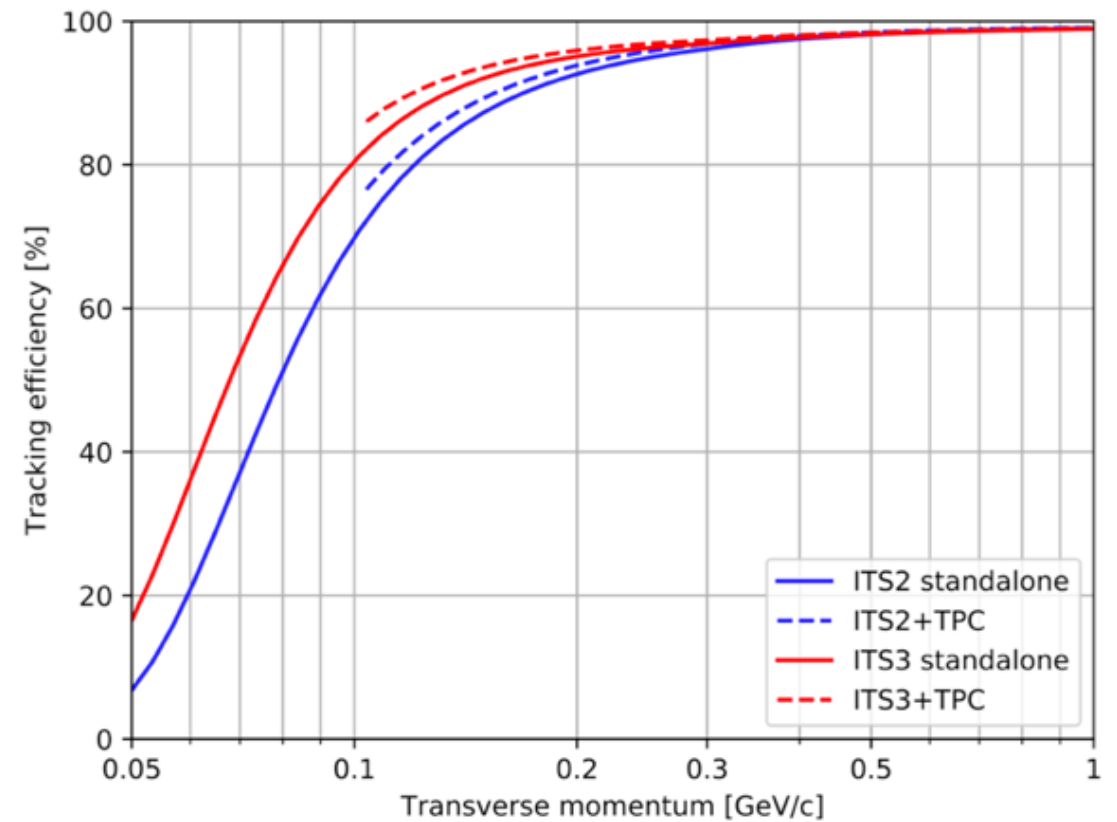
ITS3 expected performance

pointing resolution



Improvement of a factor 2 over all momenta

tracking efficiency

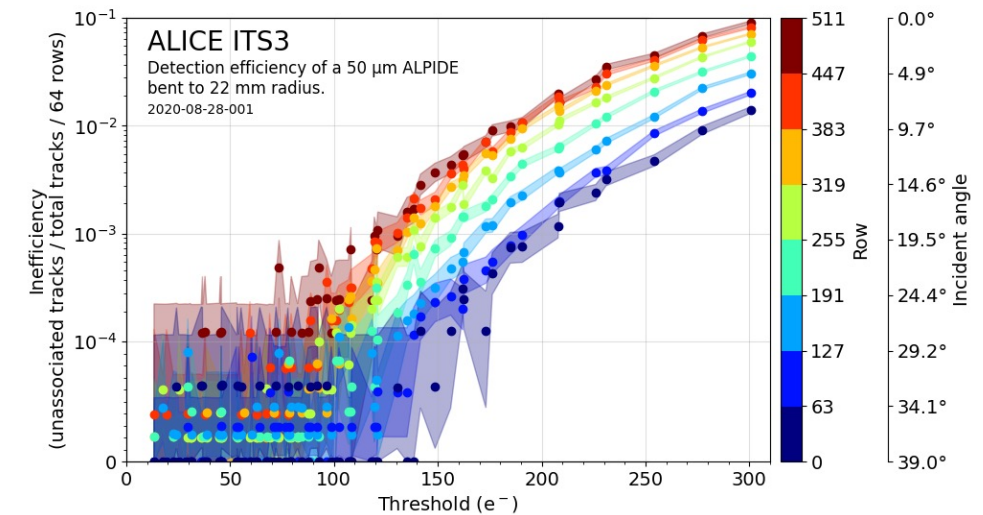
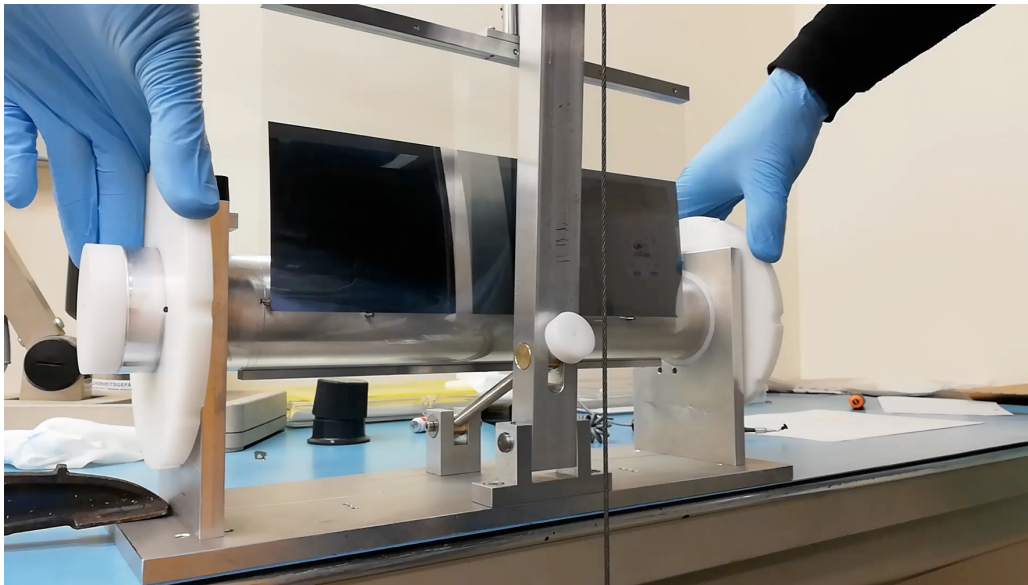
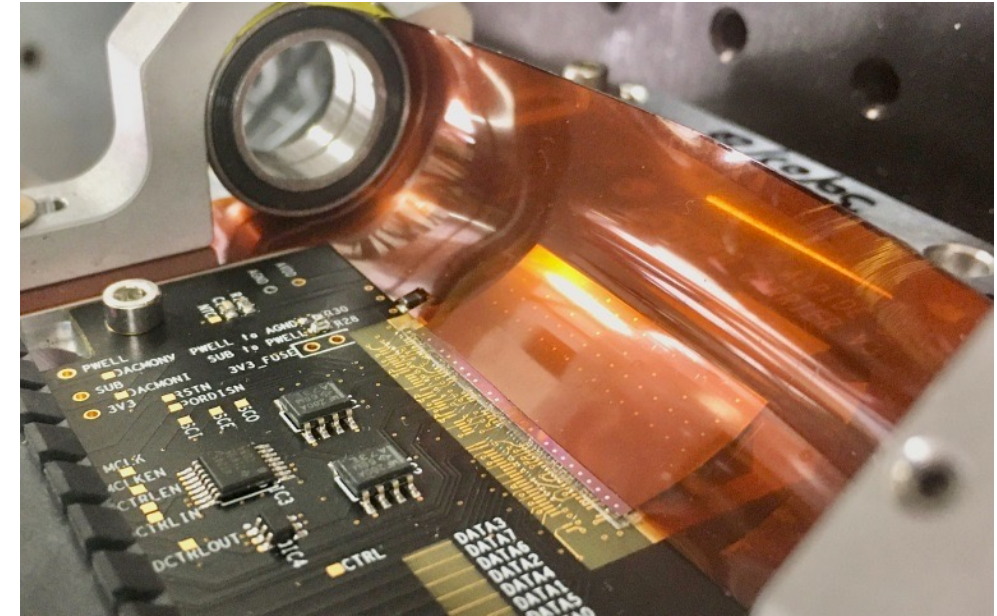


Large Improvement for low transverse momenta

Ongoing R&D: Thinning and Bending of CMOS sensors

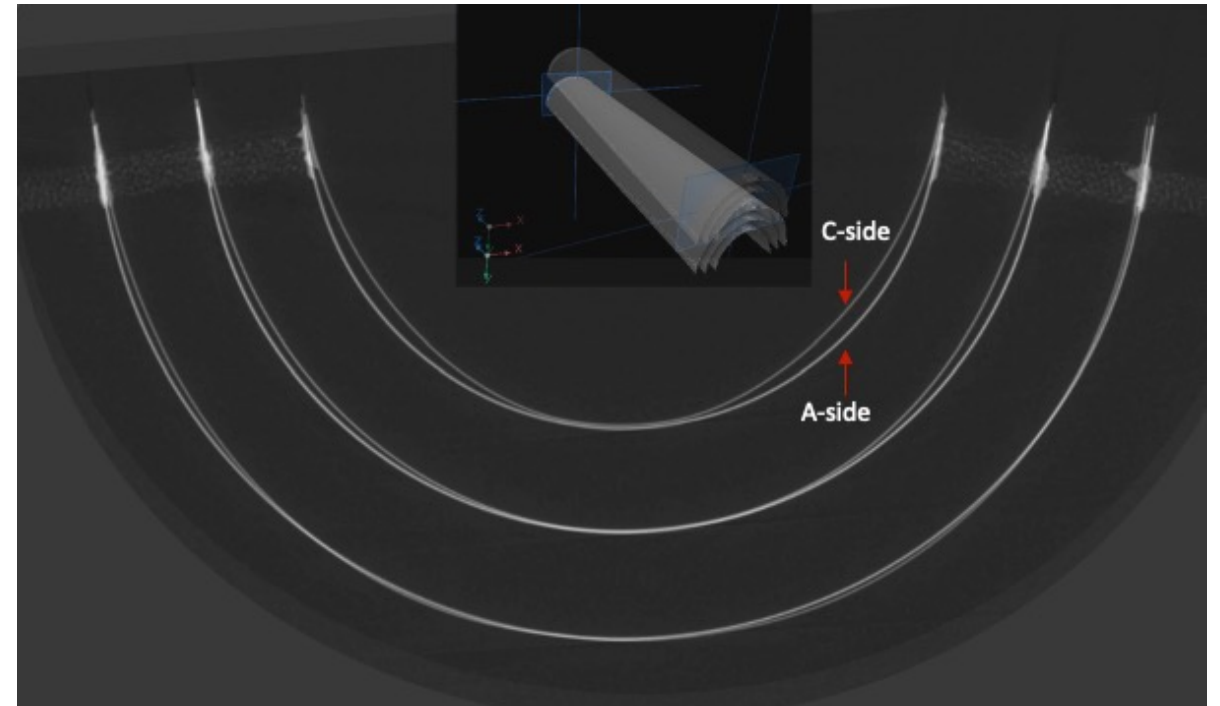
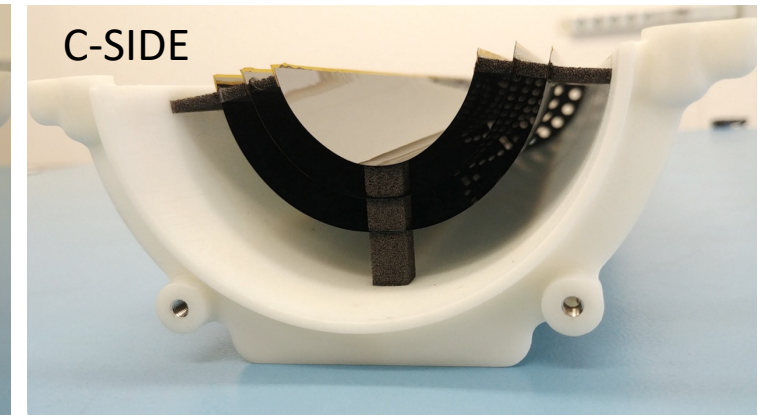
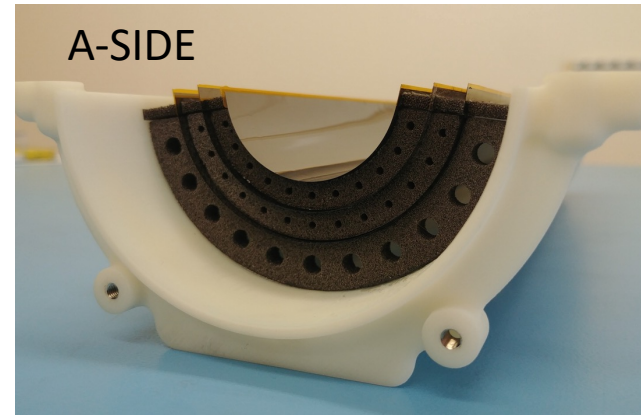


- Bending of 180nm small size MAPS
 - 50 μm thick ITS2 chip (ALPIDE) bent to 22 mm showed excellent efficiency in the beam test in 2020
- Development of tools to bend large area silicon sensors



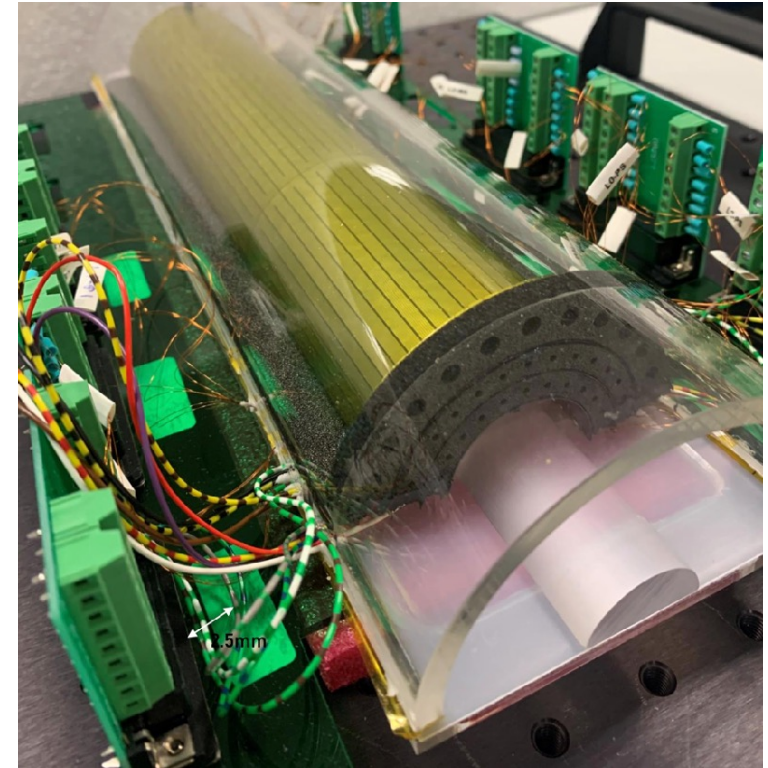
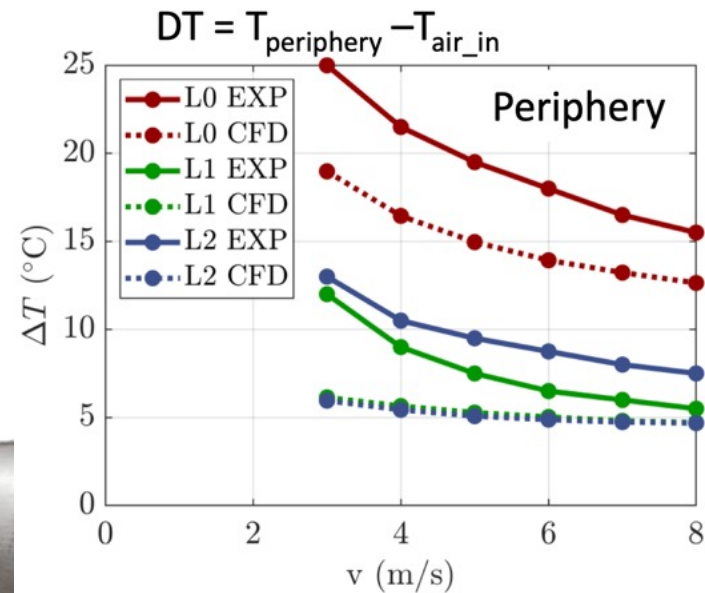
Mechanics:

- Engineering models of ITS3 are being produced
 - Equipped with dummy silicon
- Used to study:
 - support structures
 - bending
 - integration
 - resulting geometry
- Very successful integration of EM1 and EM2
- Off-shape distortions are identified and mitigation will be implemented in EM3



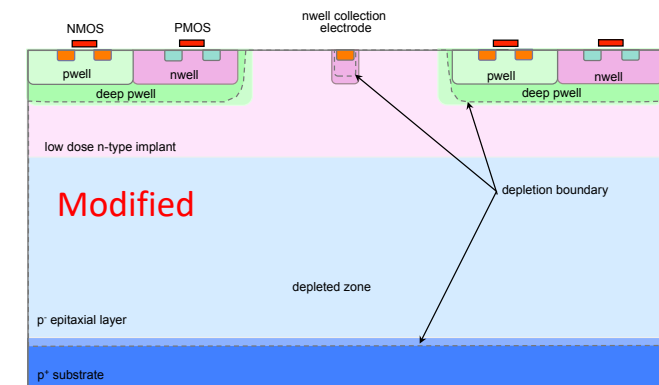
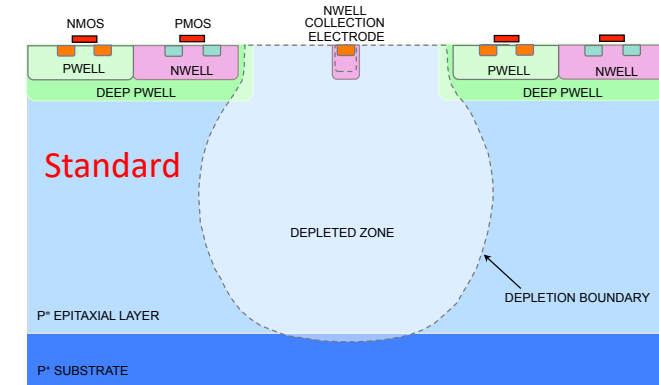
Cooling:

- Models including heating elements are being developed
- In a custom wind tunnel, thermal and mechanical properties are studied

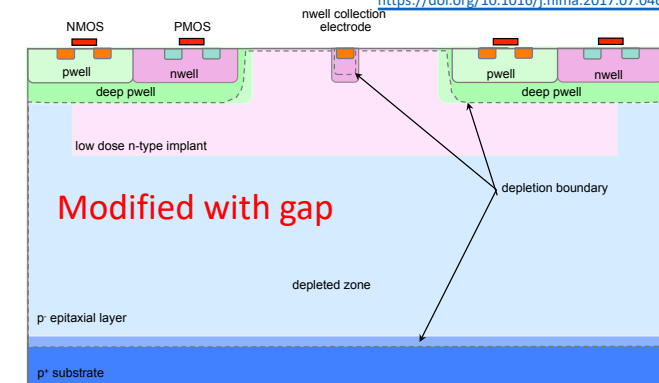


GOING BIGGER → 27×9 cm² final sensor

- Available on 300 mm wafers
- Provides 2D stitching
- 65 nm → lower power consumption
- 7 metal layers
- Process modifications for full depletion:
 - Standard (no modifications)
 - Modified (low dose n-type implant)
 - Modified with gap (low dose n-type implant with gaps)



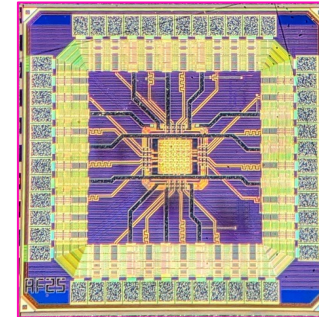
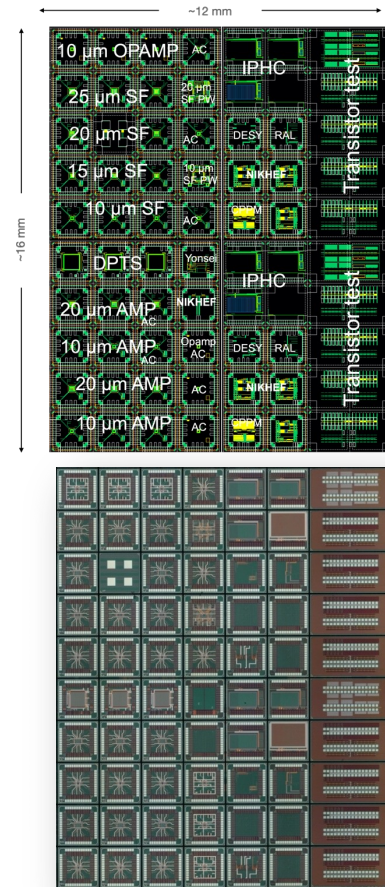
<https://doi.org/10.1016/j.nima.2017.07.046>



<https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013>

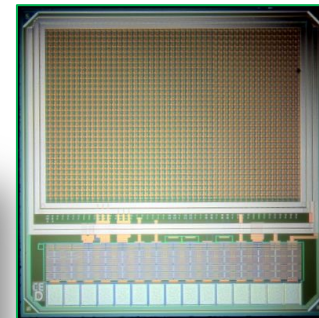
First test submission: MLR1

- Submitted in December 2020
- Main goals:
 - Learn technology features
 - Characterize charge collection
 - Validate radiation tolerance
- Each reticle (12×16 mm²):
 - 10 transistor test structures (3×1.5 mm²)
 - 60 chips (1.5×1.5 mm²)
 - Analogue blocks
 - Digital blocks
 - Pixel prototype chips: APTS, CE65, DPTS
- Testing since September 2021:
 - huge effort shared among many institutes
 - laboratory tests with ⁵⁵Fe source
 - beam tests @ PS, SPS, Desy, MAMI



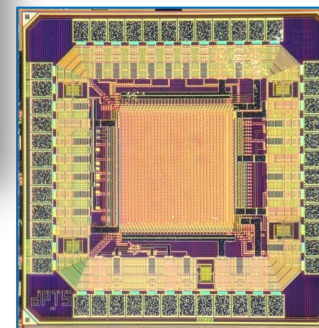
APTS:

- 6×6 pixel matrix
- Direct analogue readout of central 4×4 submatrix
- Two types of output drivers:
 1. Traditional source follower (APTS-SF)
 2. Very fast OpAmp (APTS-OA)
- 4 pitches: 10, 15, 20, 25 μm



CE65:

- 2 matrix sizes, 15 or 25 μm pitch
- Rolling shutter readout (50 μs integration time)
- 3 in-pixel architectures:
 1. AC-coupled amplifier
 2. DC-coupled amplifier
 3. Source follower



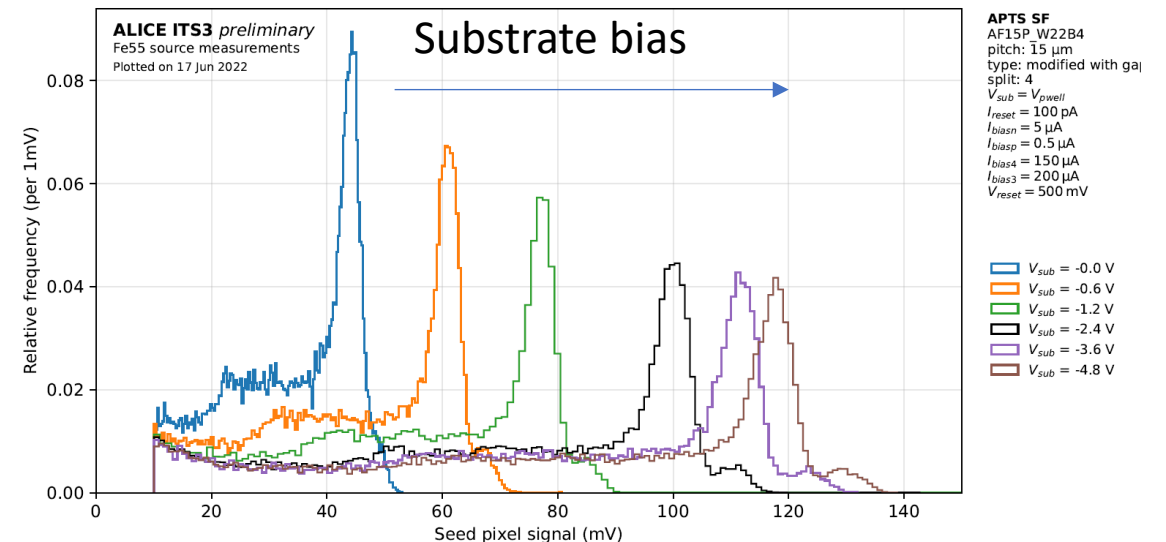
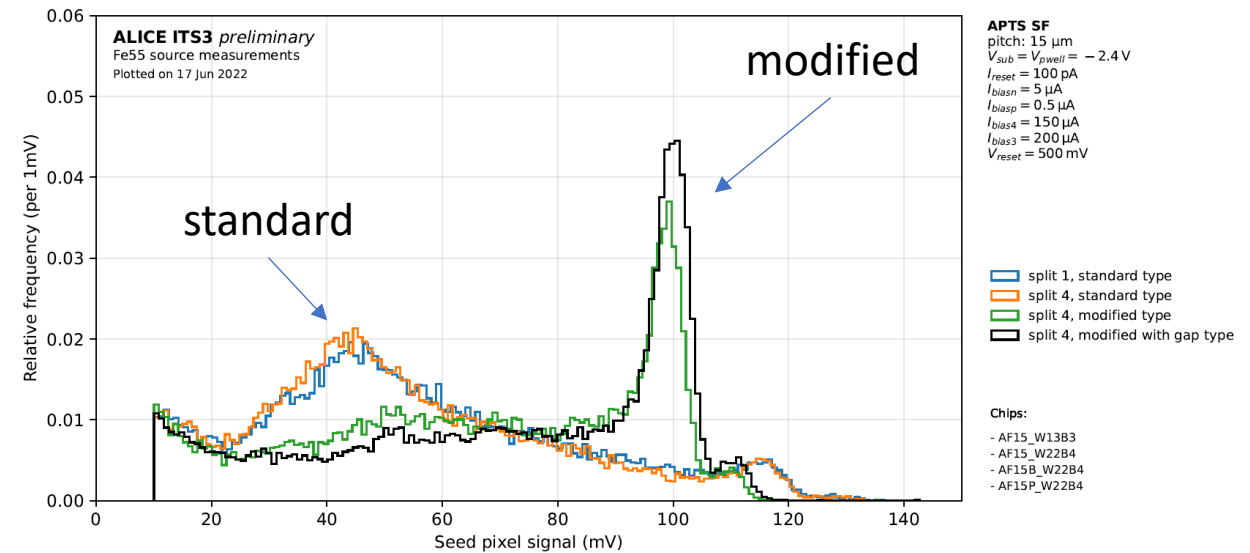
DPTS:

- 32×32 pixel matrix
- Asynchronous digital readout
- Time-over-Threshold information
- Pitch: 15×15 μm²

RESULTS: APTS SourceFollower

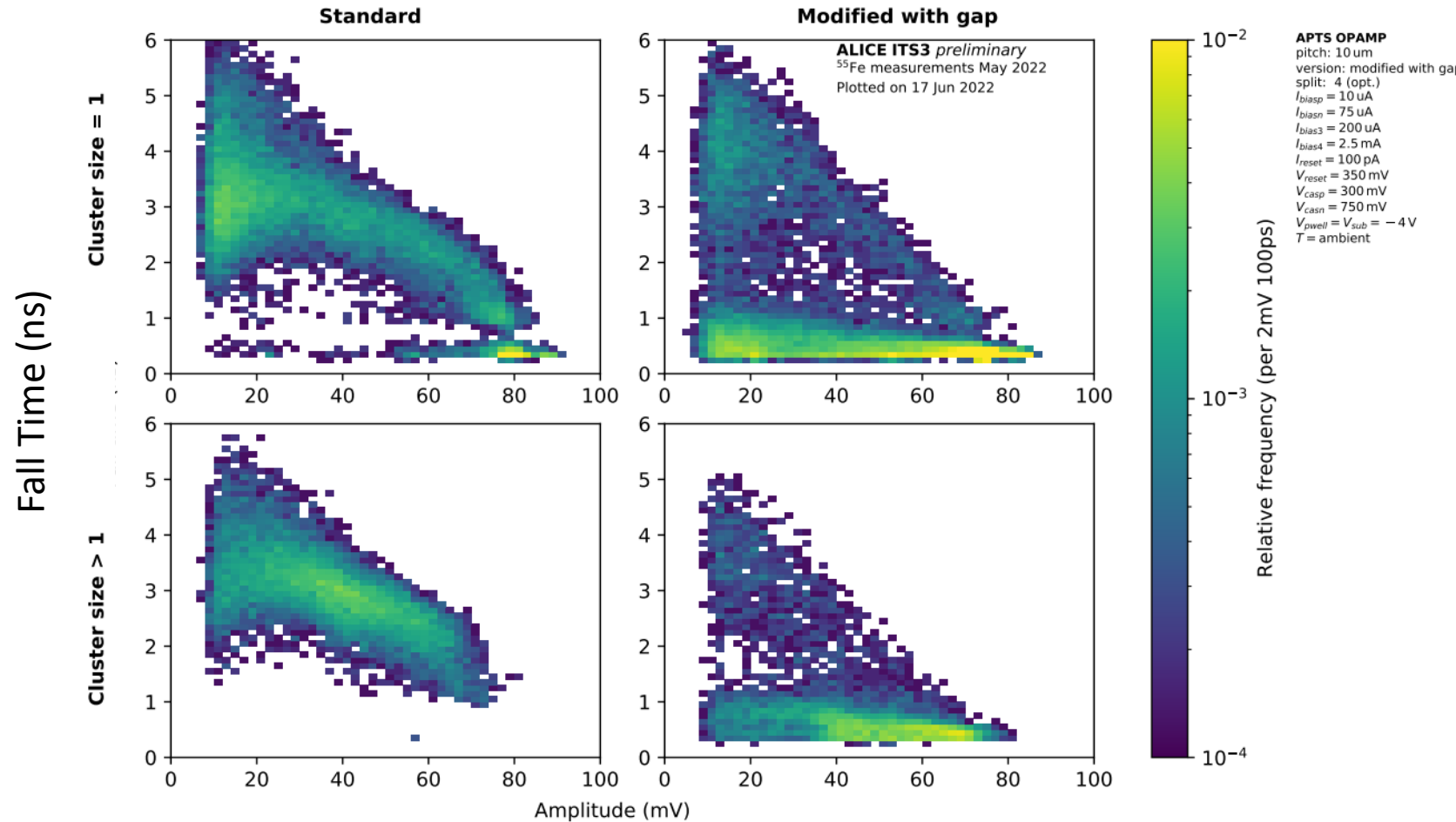


- Process modification reduces charge sharing:
 - In standard process seed pixel takes ~50% of the charge
 - In modified process most of the charge is collected in one pixel
 - Effect on efficiency and spatial resolution verified at beam test: analysis ongoing
- Substrate bias amplifies the signal
 - Substrate bias lowers the node capacitance to as low as 2.2 fF
 - Signal amplitude increases



RESULTS: APTS OpAmp

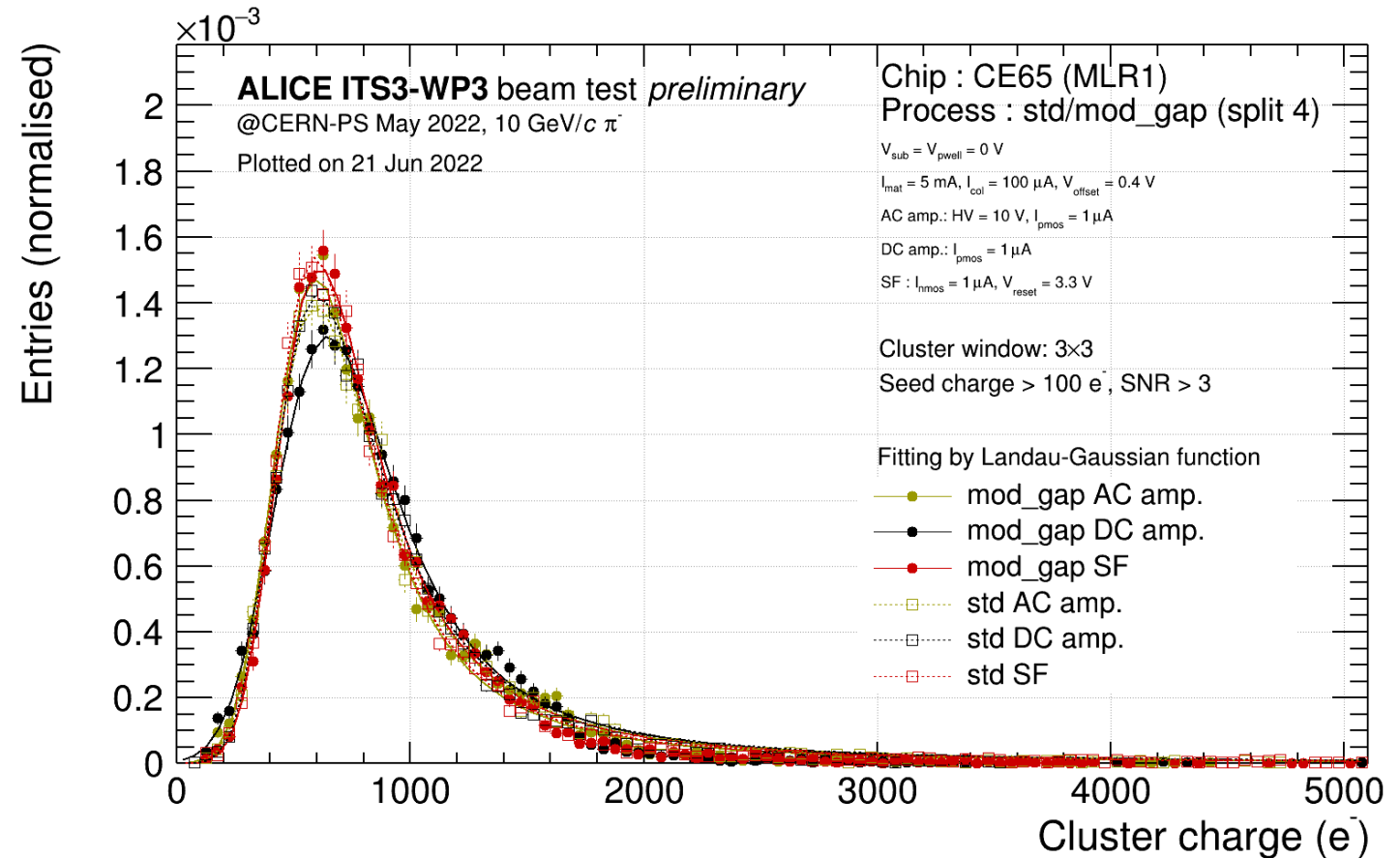
- Process modification reduces charge collection time
 - Fast readout allows to estimate the charge collection time via signal fall time
 - In modified process the charge is collected faster



- Cluster charge doesn't depend on process modification and pixel architecture

- All submatrices in standard and modified processes collect the same total charge
- Charge distribution parameters roughly correspond to effective epitaxial layer of 11 μm

(via H. Bichsel <https://doi.org/10.1103/RevModPhys.60.663>)

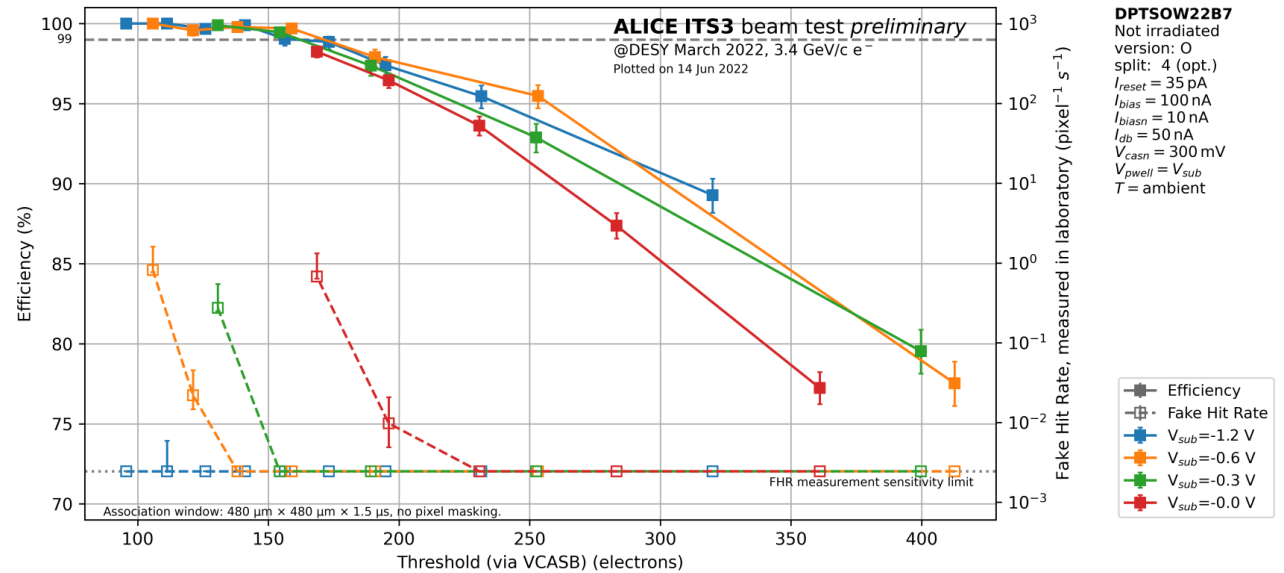


RESULTS: DPTS



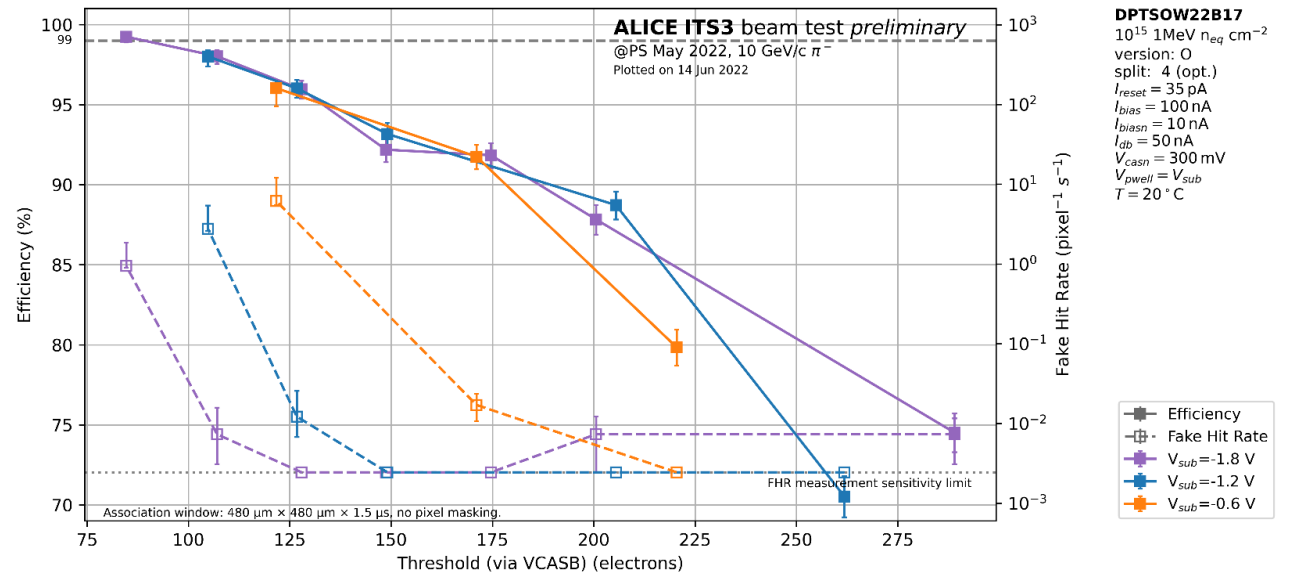
- Non-Irradiated DPTS:

- Excellent efficiency and low fake hit rate



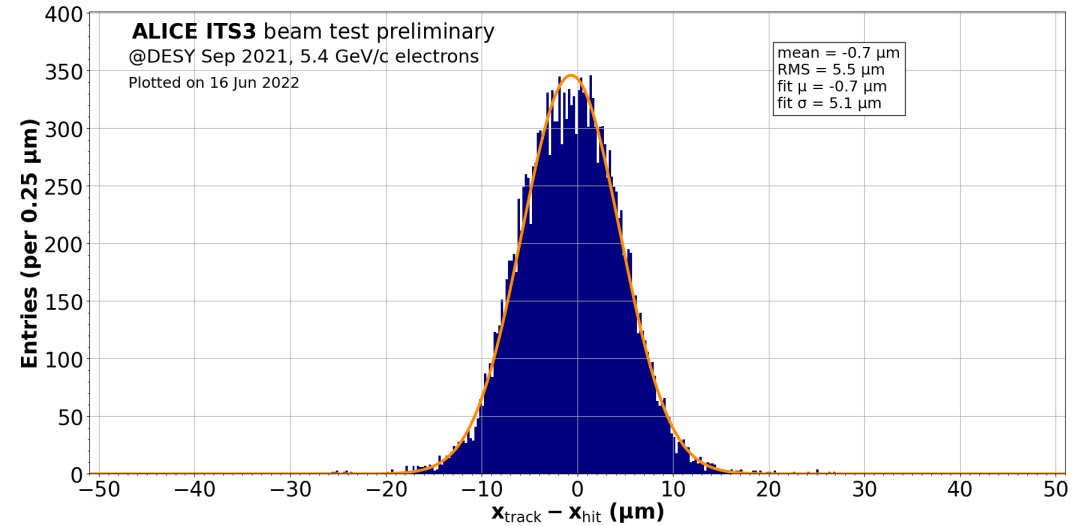
- Irradiated DPTS (10^{15} n_{eq}):

- Efficient at 20°C with limited fake hit rate



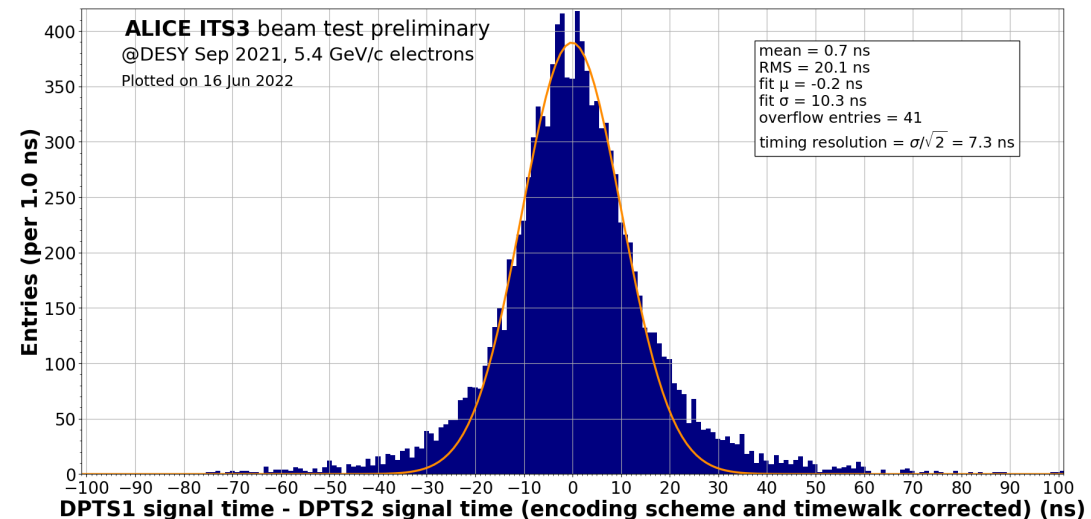
RESULTS: DPTS

- Spatial resolution $\sim 5 \mu\text{m}$



DPTSOW22B3 (not irradiated)
version: O
split: 4 (opt.)
 $I_{\text{reset}} = 10 \text{ pA}$
 $I_{\text{bias}} = 100 \text{ nA}$
 $I_{\text{biasn}} = 10 \text{ nA}$
 $I_{\text{db}} = 100 \text{ nA}$
 $V_{\text{casn}} = 300 \text{ mV}$
 $V_{\text{casb}} = 250 \text{ mV}$
 $V_{\text{pwell}} = V_{\text{sub}} = -1.2\text{V}$

- Timing resolution $\sim 7 \text{ ns}$



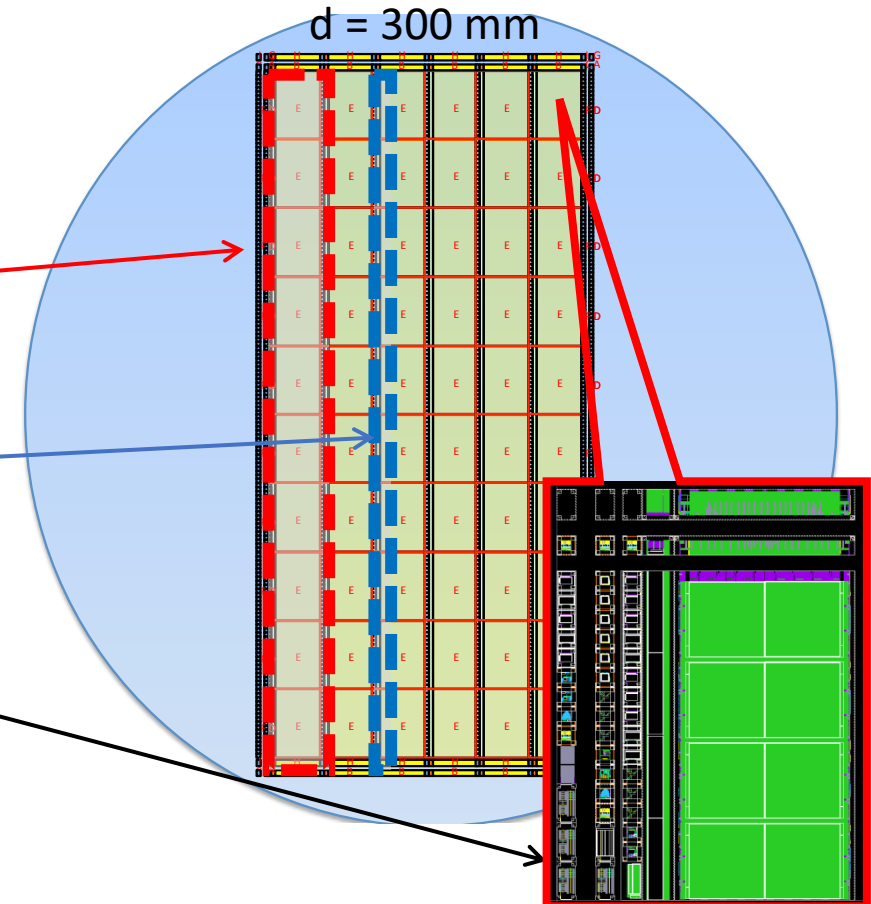
DPTSOW22B3 (not irradiated)
version: O
split: 4 (opt.)
 $I_{\text{reset}} = 10 \text{ pA}$
 $I_{\text{bias}} = 100 \text{ nA}$
 $I_{\text{biasn}} = 10 \text{ nA}$
 $I_{\text{db}} = 100 \text{ nA}$
 $V_{\text{casn}} = 300 \text{ mV}$
 $V_{\text{casb}} = 250 \text{ mV}$
 $V_{\text{pwell}} = V_{\text{sub}} = -1.2\text{V}$

DPTSXW22B1 (not irradiated)
version: X
split: 4 (opt.)
 $I_{\text{reset}} = 10 \text{ pA}$
 $I_{\text{bias}} = 100 \text{ nA}$
 $I_{\text{biasn}} = 10 \text{ nA}$
 $I_{\text{db}} = 100 \text{ nA}$
 $V_{\text{casn}} = 300 \text{ mV}$
 $V_{\text{casb}} = 280 \text{ mV}$
 $V_{\text{pwell}} = V_{\text{sub}} = -1.2\text{V}$

Next step: stitching -> large area sensors

First run with 2 stitched sensors about to be submitted (ER1):

- **MOSS**
260×14 mm² 6.72 Mpixels
- **MOST**
260×2.5 mm² 900 kPixels
- + multiple small chips for further technology exploration
- Test structures expected to be delivered early 2023



Summary of ITS2 & ITS3

ITS2

- ITS2 installed and commissioned for LHC RUN3
 - Calibration procedure established and tested
 - DCS and QC tools ready for data taking
 - Detector settings optimized both for pp and PbPb collisions
- ITS2 successfully took data with top energy pp collisions:
 - framing rate at 202kHz
 - collision rate up > 1MHz



ITS2 Outer Barrel during insertion tests

ITS3

- project well on track
- very encouraging results from first chip prototypes:
 - Efficiency > 99% at FHR < 1 hit/second/1024 pixels
 - Spatial resolution ~5 μm
 - Timing resolution ~7 ns
 - Withstands NIEL irradiation of up to $10^{15} n_{\text{eq}}/\text{cm}^2$
- large scale stitched structures about to be produced in ER1



ITS3 mechanical mock up

Thank you for your attention!

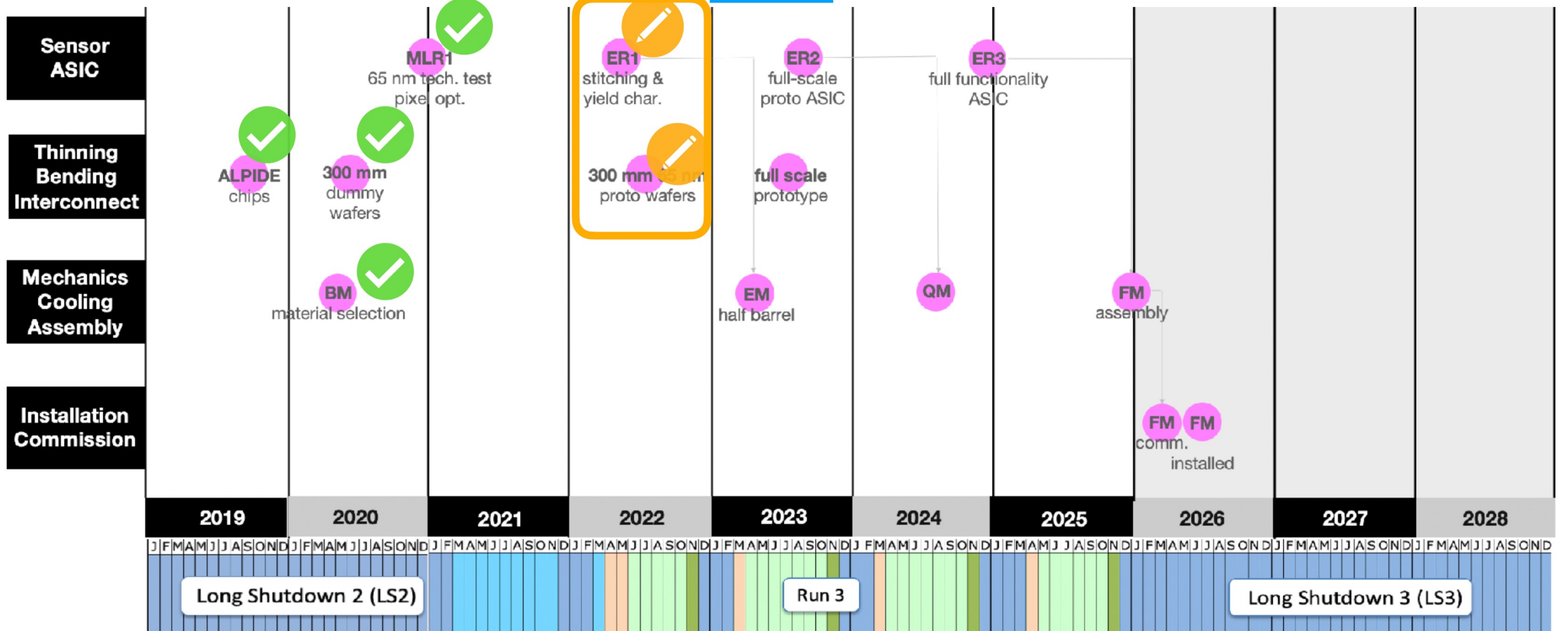
BACK UP SLIDES

ITS3 project timeline



ALICE

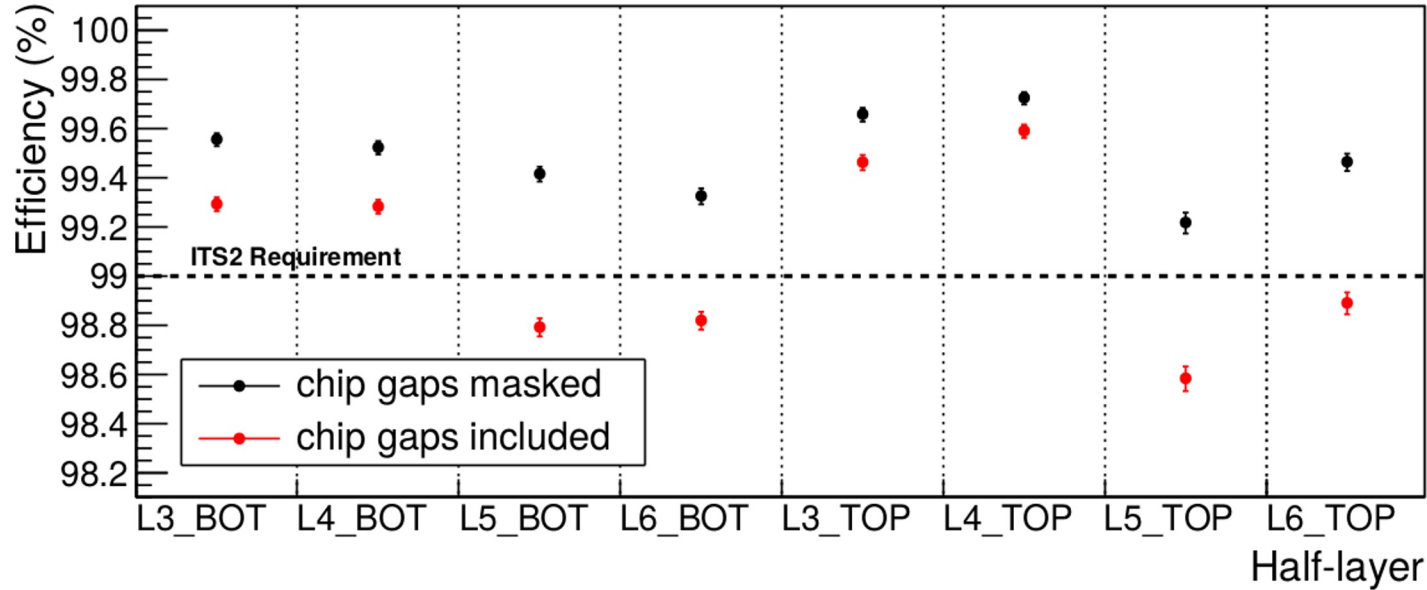
update on main milestones



MLR: multiple layer per reticle, **ER:** engineering run,
BM: breadboard module, **EM:** engineering module, **QM:** qualification module, **FM:** final module

On-Surface Commissioning – Outer Barrel Efficiency

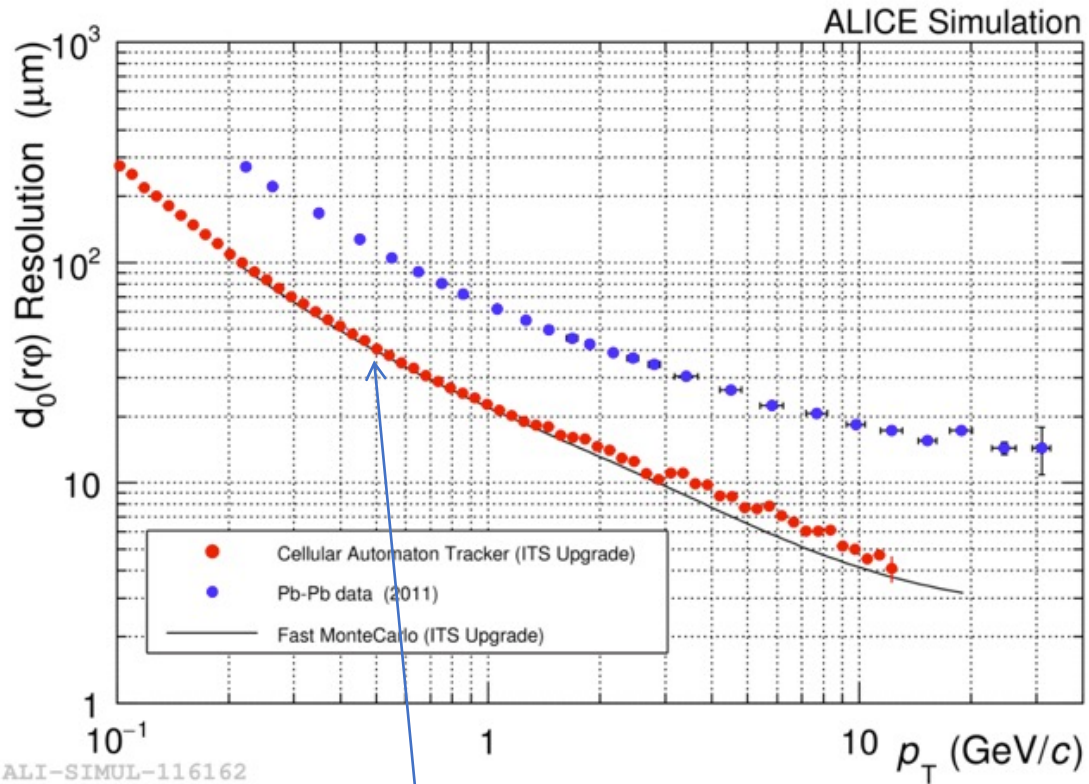
- [Preliminary study] Efficiency of OB using cosmic tracks



- Restricted to cosmic tracks passing through 10 cm sphere around interaction point for realistic track geometry
- Preliminary cut on chip gaps to restrict region-of-interest to sensitive area
- Measured efficiency well above 99% for all layers

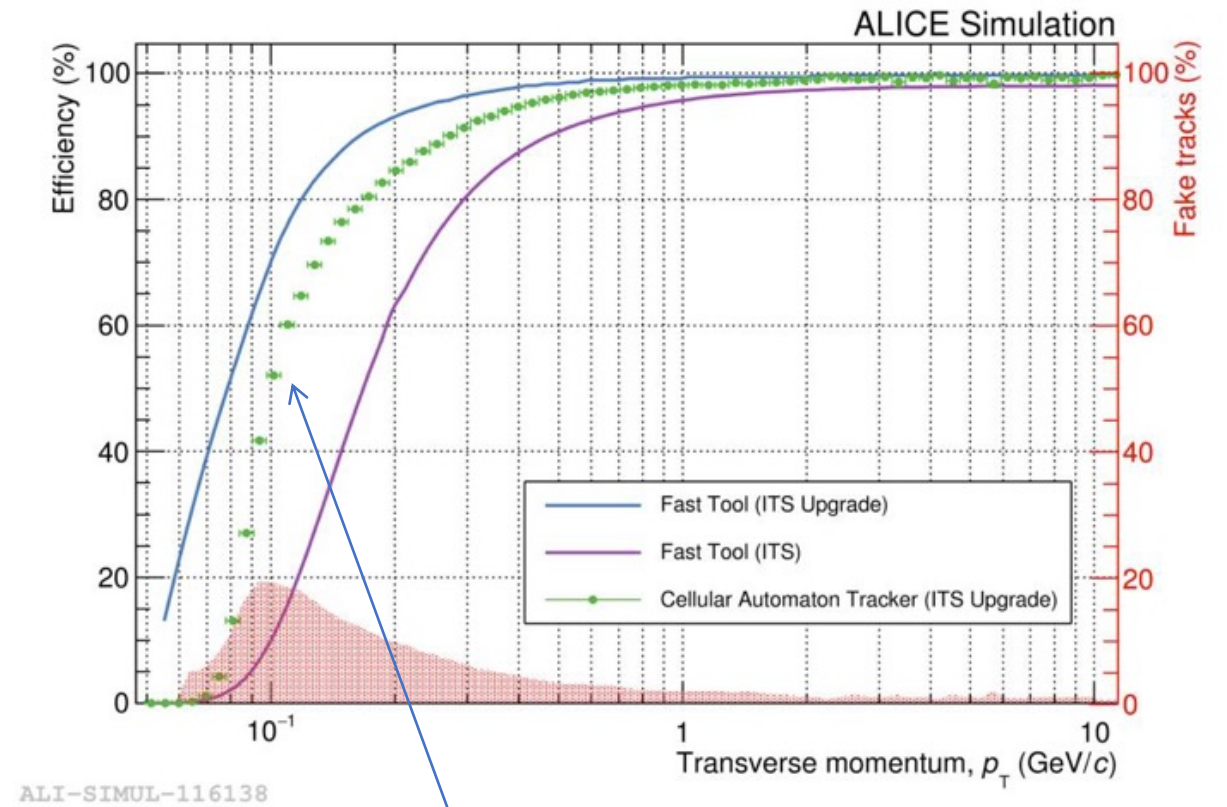
Expected ITS2 performance

Impact parameter resolution



40 μm at $p_T = 500$ MeV/c

Tracking efficiency (ITS standalone)



$\sim 60\%$ at $p_T = 100$ MeV/c

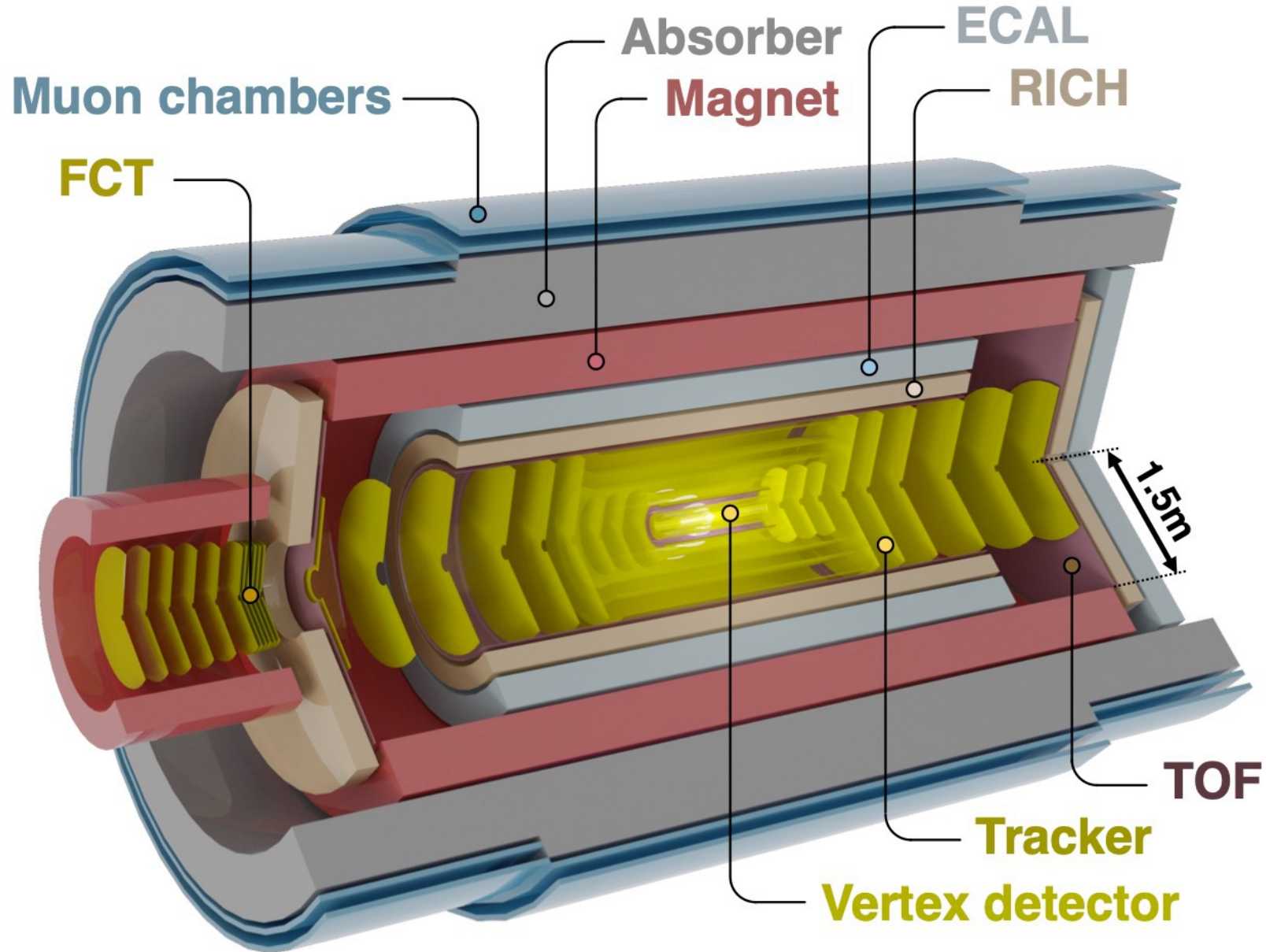
The ALICE experiment



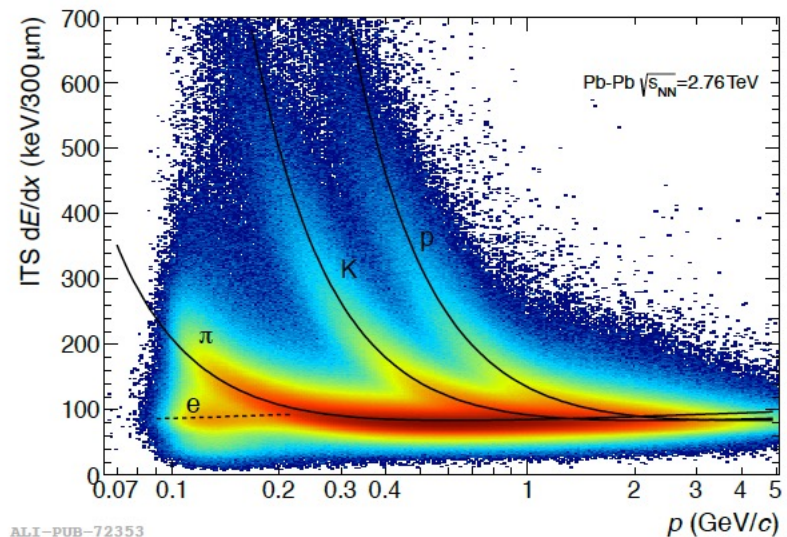
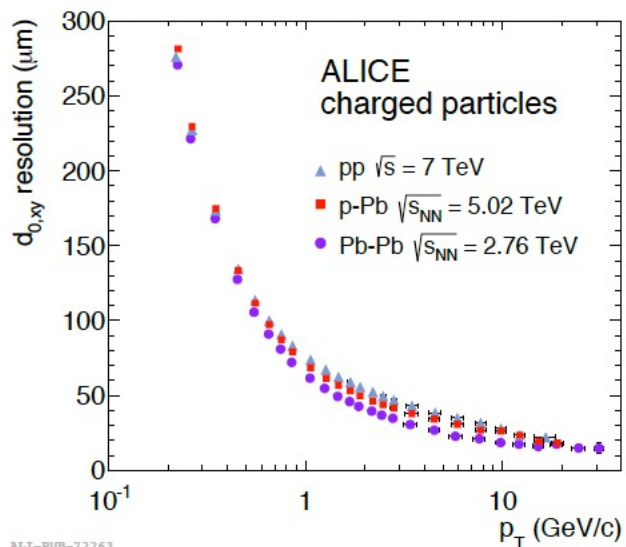
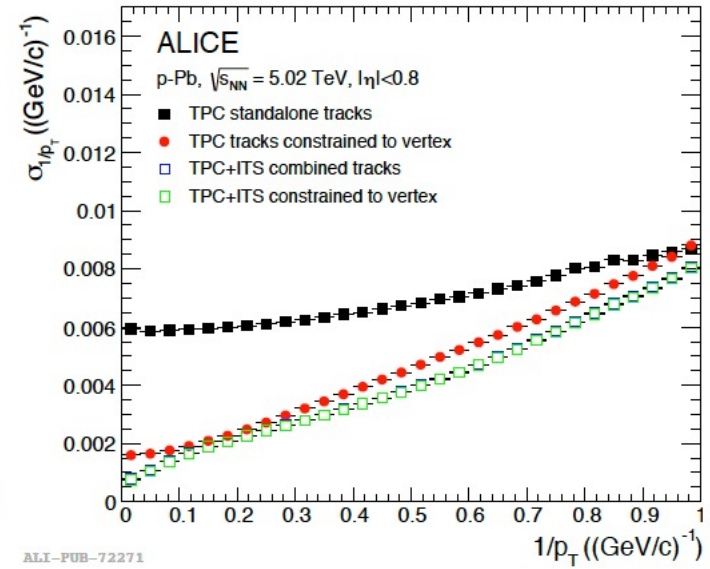
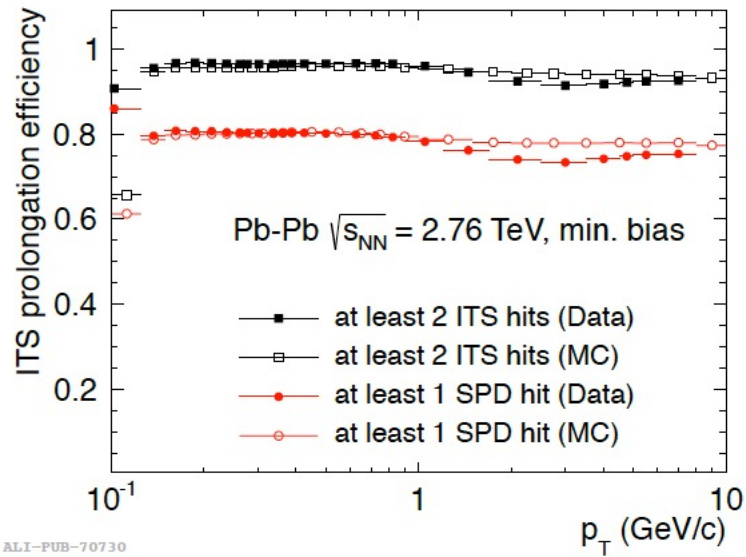
- **1012 Authors**
- **174 Institutes**
- **40 Countries**

What next? ALICE3

- xxx



ITS1 performance

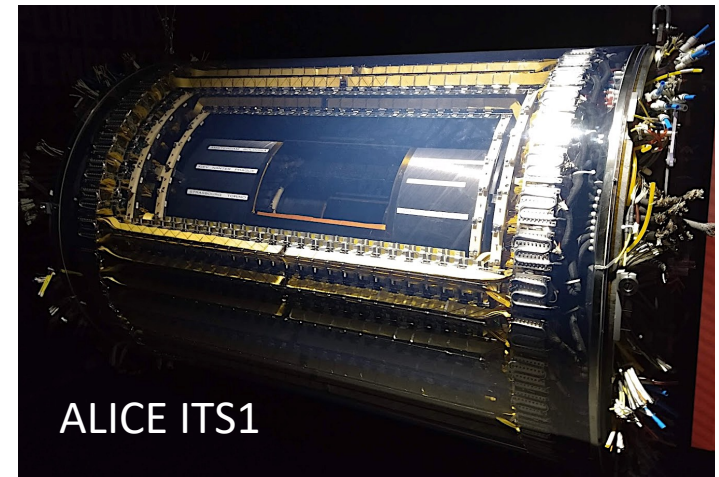
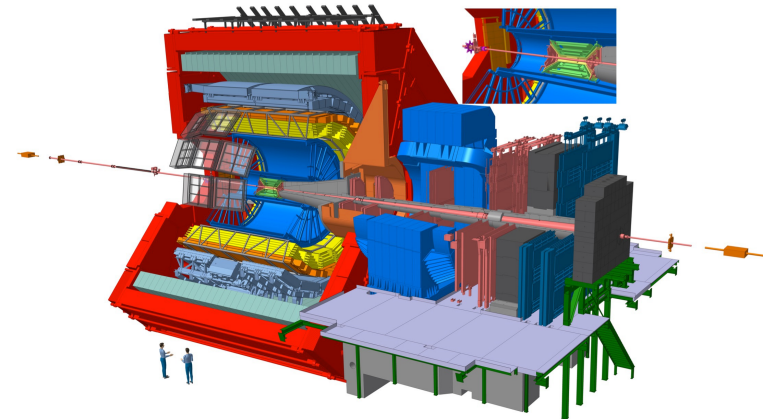
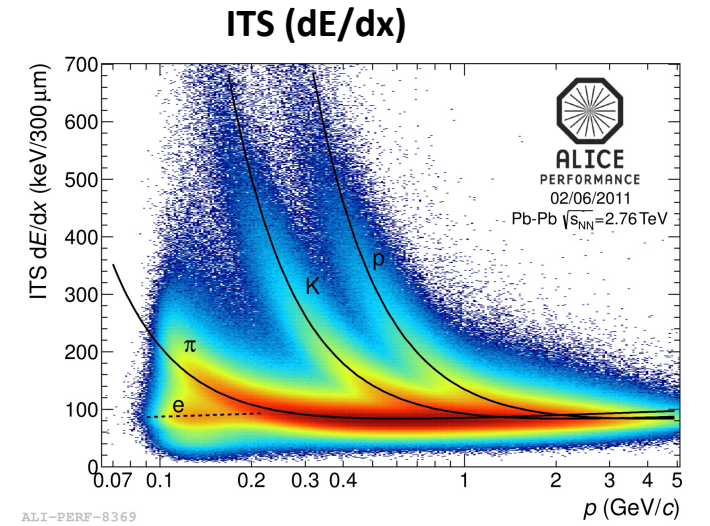
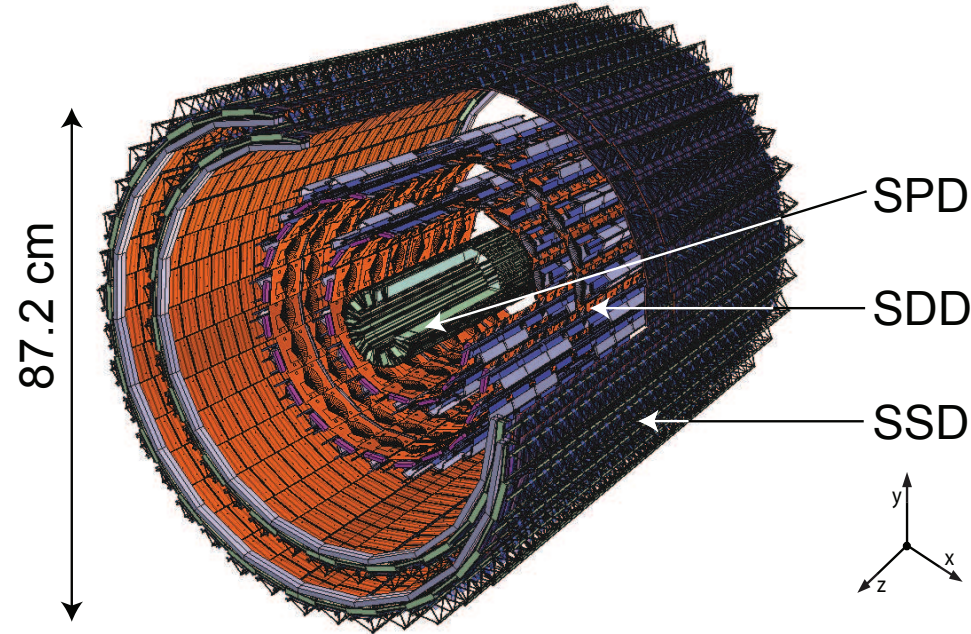


• XXXX

The first Inner Tracking System

- Inner Tracking System:

- Vertexing
- Tracking
- PID



Charged particle tracker

- GOALS

- Reconstruct charged particles trajectories = “tracks”
- measure position of primary and secondary vertices
- identify particles

- Traditional silicon sensor technologies:

- microstrips
- hybrid pixels
- drift detectors (ALICE only)

All trackers need to be upgraded (sensors replaced) to satisfy HL requirements:

- Peak luminosity: $5-7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
- Average pile-up (PU) in pp: up to ~ 200
- Collision rates for ions: 50kHz
- Total Ionizing Dose (TID) up to 1 Grad
- Particle fluence up to $2 \times 10^{16} \text{ n}_{\text{eq}}\text{cm}^{-2}$ in the vertex region

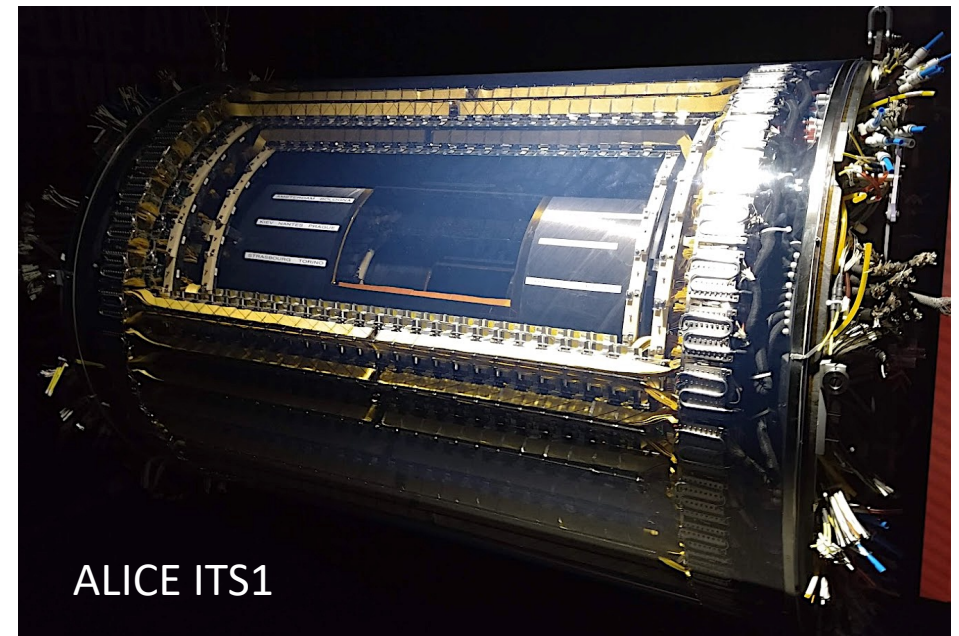
- improved traditional technologies

- new technologies for present and future upgrades

- CMOS sensors
- 4D sensors

- Challenging requirements:

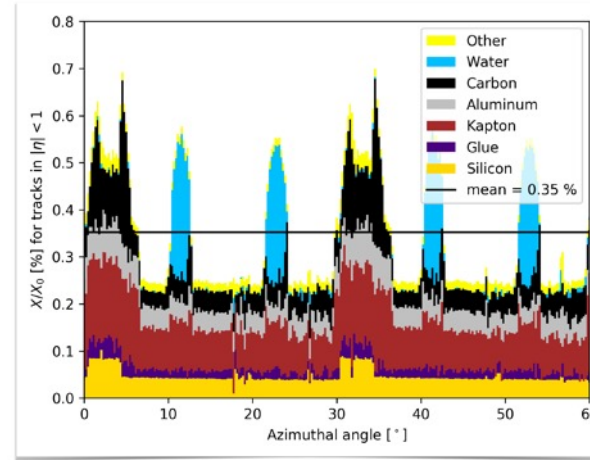
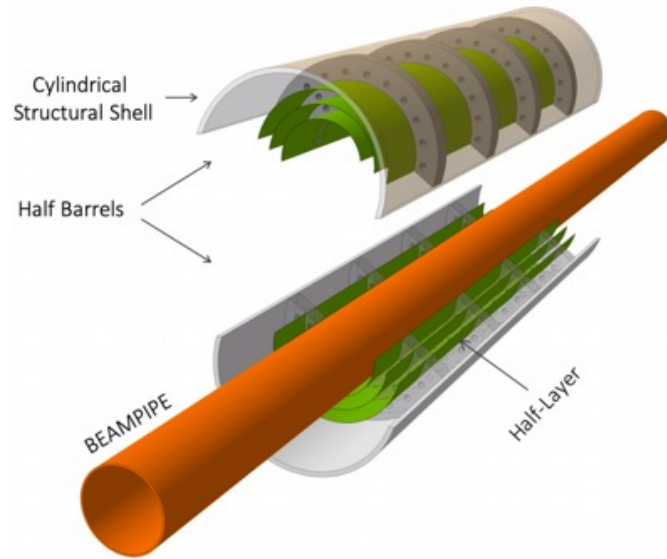
- excellent pointing resolution
 - position resolution
 - material budget
 - distance from IP of the first layer
- high data rates
- radiation tolerant



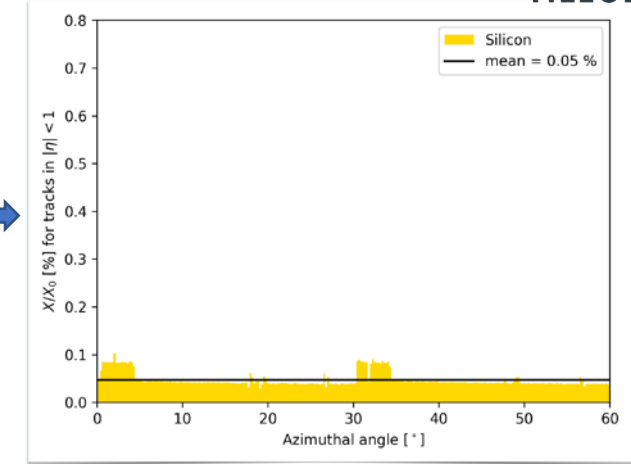
ALICE 2.1: ITS3 all silicon detector



ALICE



ITS2 Layer 0: $X/X_0=0.35$



ITS3 only silicon: $X/X_0=0.05$

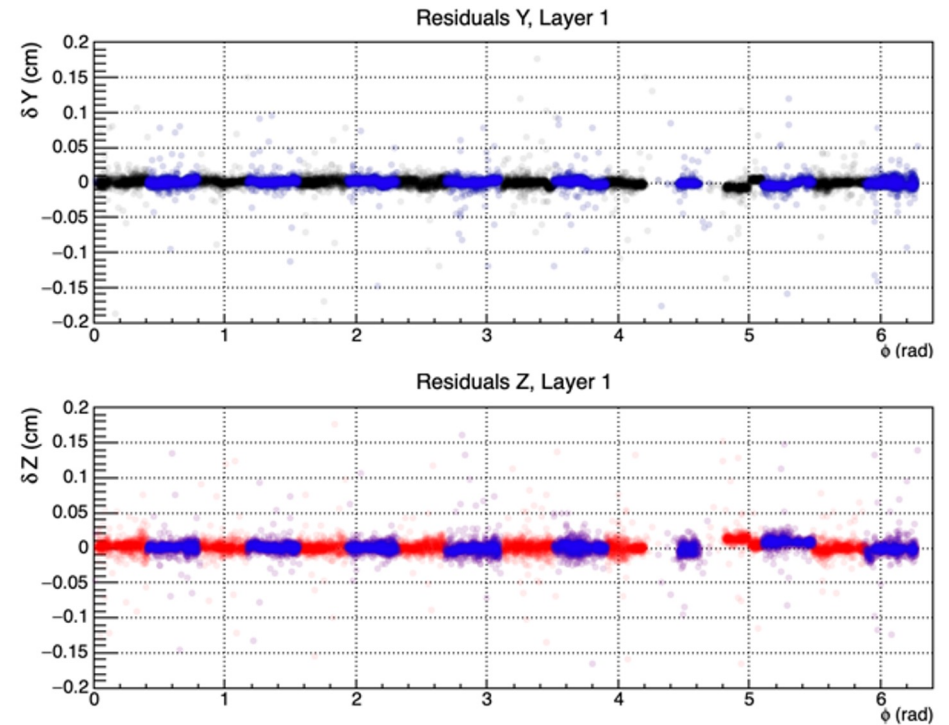
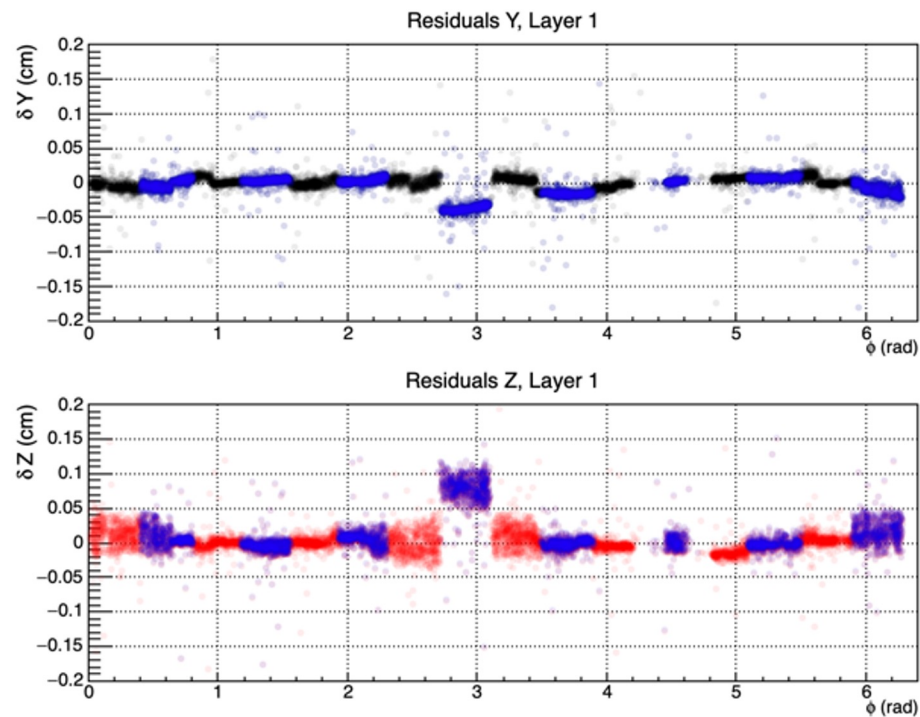
- Goal: improve vertexing at high rate
- Layout: 3 layers, replace ITS Inner Barrel,
 - beam pipe: smaller inner radius (18.2 mm to 16 mm) and reduced thickness (800 μm to 500 μm)
 - innermost layer: mounted around the beam pipe, radius 18mm (was 22 mm)
- Technology choices:
 - 65 nm CIS of Tower & Partners Semiconductor (TPSCo):
 - larger wafers: 300 mm instead of 200 mm,
 - single “chip” equips an ITS3 half-layer (through stitching technology)
 - 6 sensors in total
 - thinned down to 20-40 μm
 - -> flexible
 - bent to target radii
 - mechanically held by carbon foam ribs with low density and high thermal conductivity



Data Preparation: alignment

- Manual pre-alignment concluded with precision of $O(100 \mu\text{m})$
- Ongoing: pre-alignment in R, Rf and Z using Millepede
 - currently at $O(10 \mu\text{m})$ for Inner Barrel and $O(50 \mu\text{m})$ for Outer Barrel)
- Next step: fine alignment targeting a precision of a few μm (using Millipede, or AI approaches)

Below: example, Y and Z residuals in L1, before and after alignment with Millepede

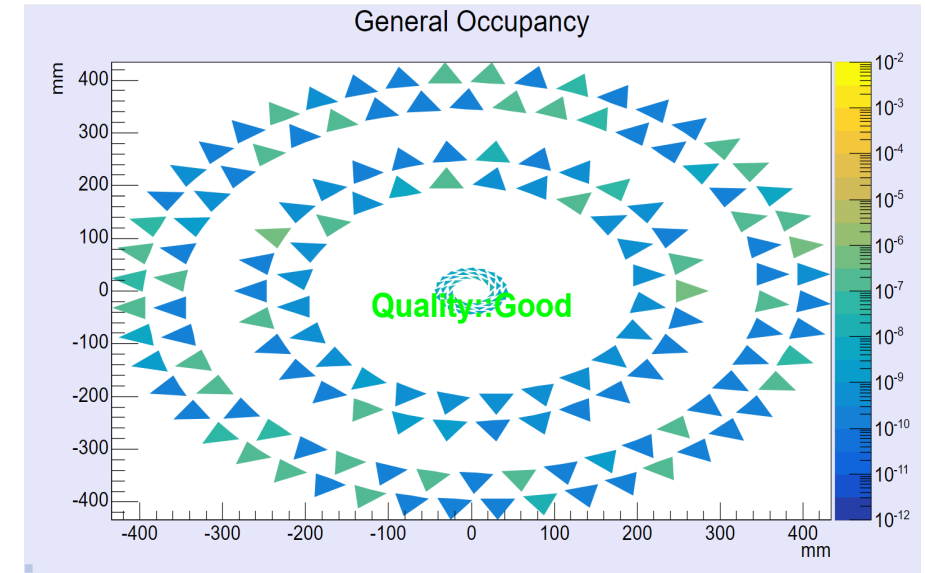


Data Quality Control (QC)



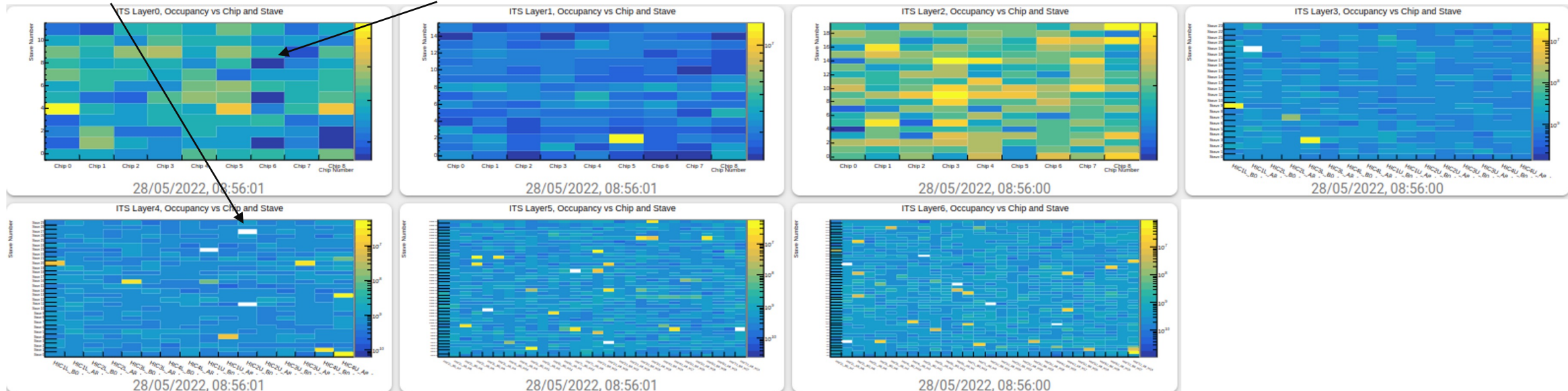
ALICE

- Comprehensive online QC to check data quality and spot problems early
- 6 QC online tasks to monitor DATA/MC quality: FHR, FEE, Cluster, Track, Noisy Pix, Monte Carlo
 - *Front-end electronics*: data integrity check with payload decoding of all events
 - *Occupancy*: monitoring of detector occupancy
 - *Cluster*: monitoring cluster size, topology etc.
 - *Tracks*: monitoring of track multiplicity, angular distribution, clusters etc.
 - *Noisy pixels*: extraction of noisy pixels for offline noise masks
 - *Threshold*: monitoring during calibration scans (threshold, ENC, dead pixels)
- Offline version of track and cluster task
- QC post-processing online and offline: FHR, FEE, Tracks, Clusters, Thresholds
 - Analysis and trending of QC online plots (run by run)



Empty lane (entire run)

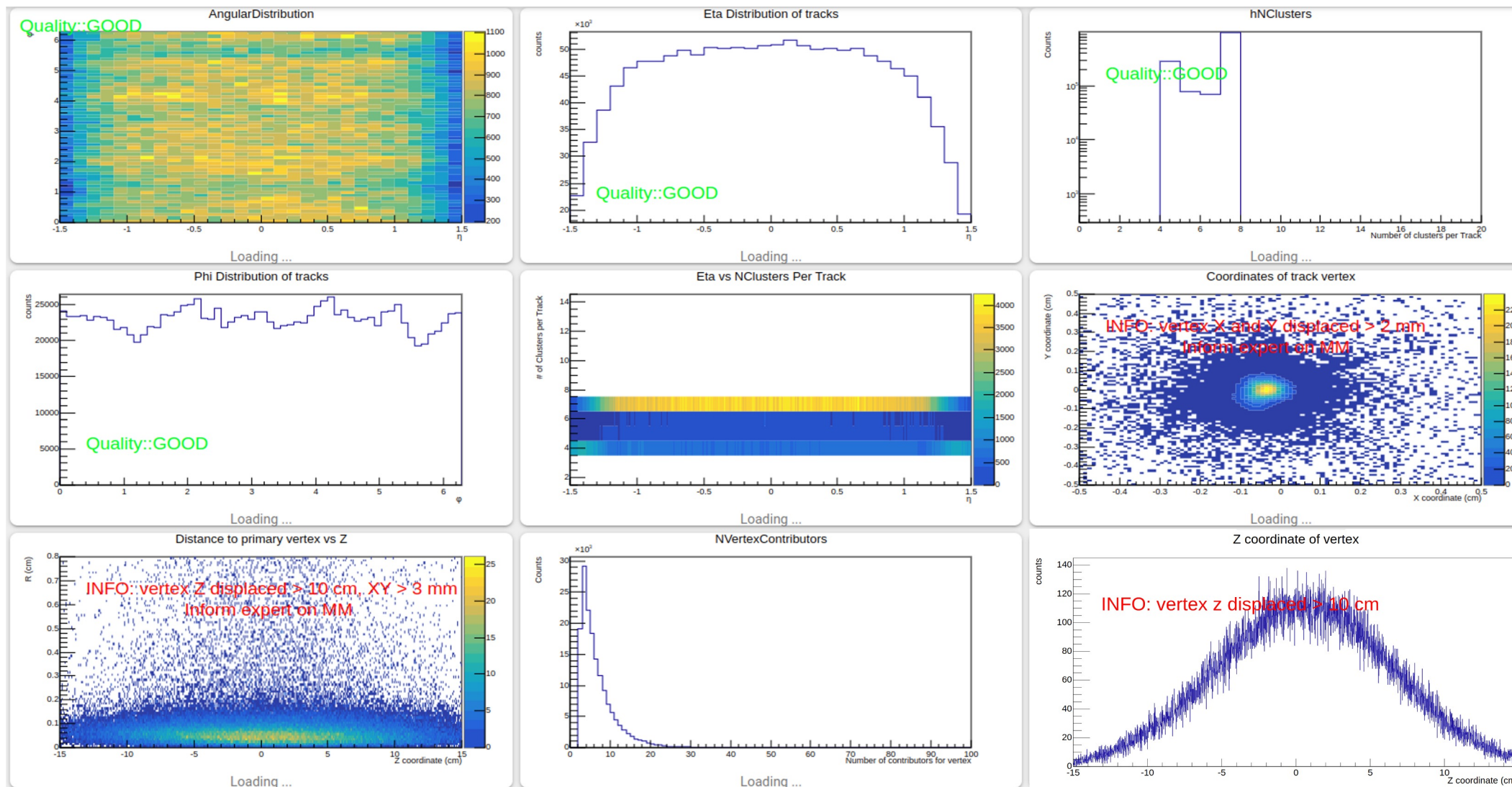
Lane stopped sending data during run



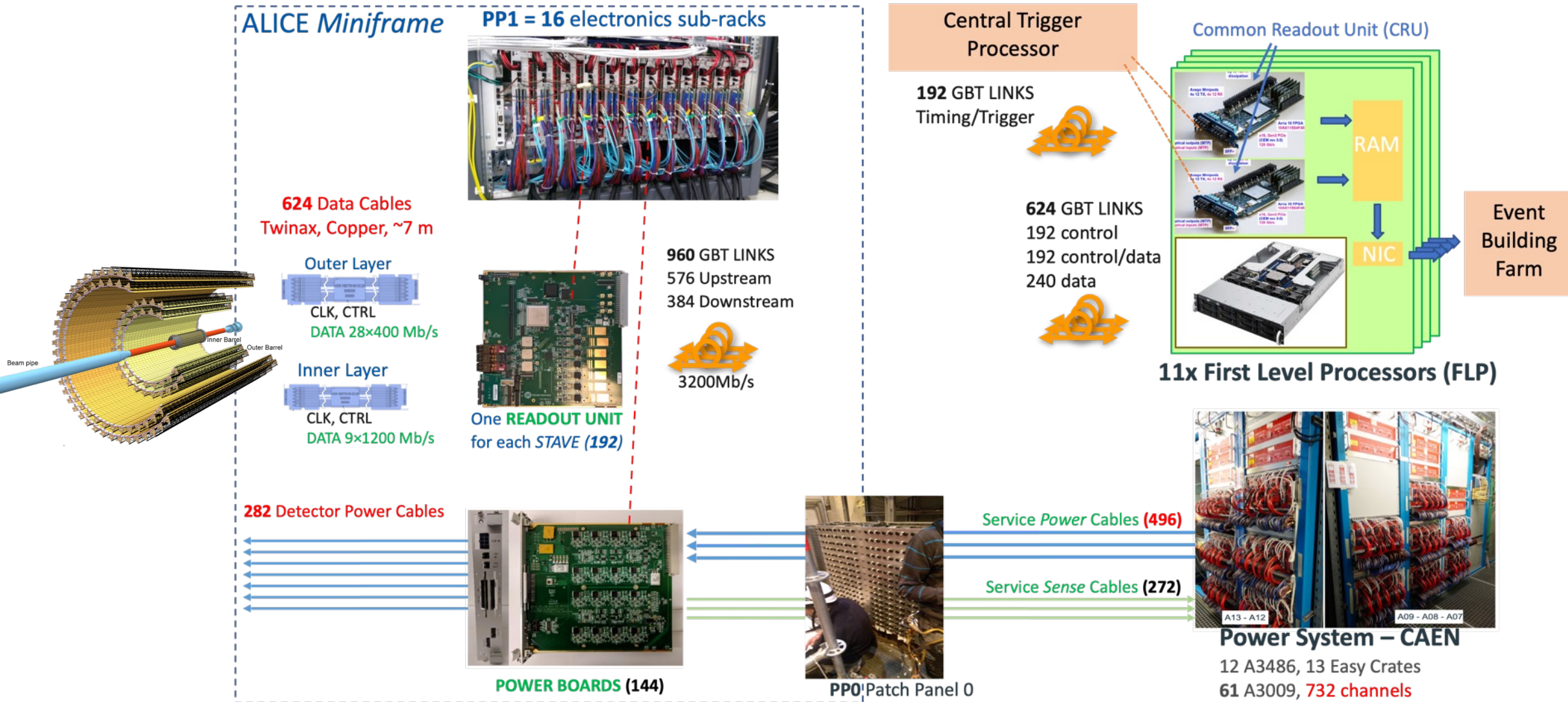
Plots from collisions (pp @900 GeV)



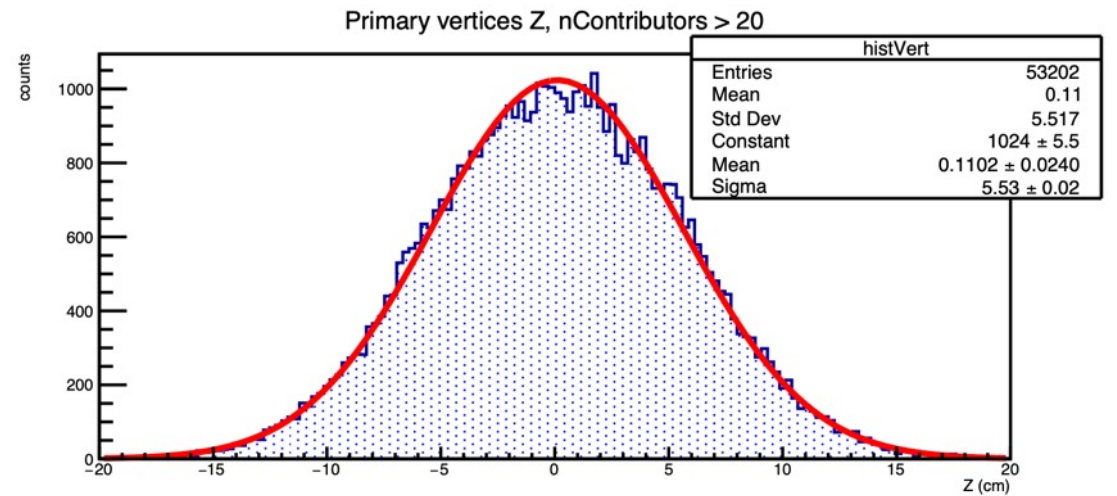
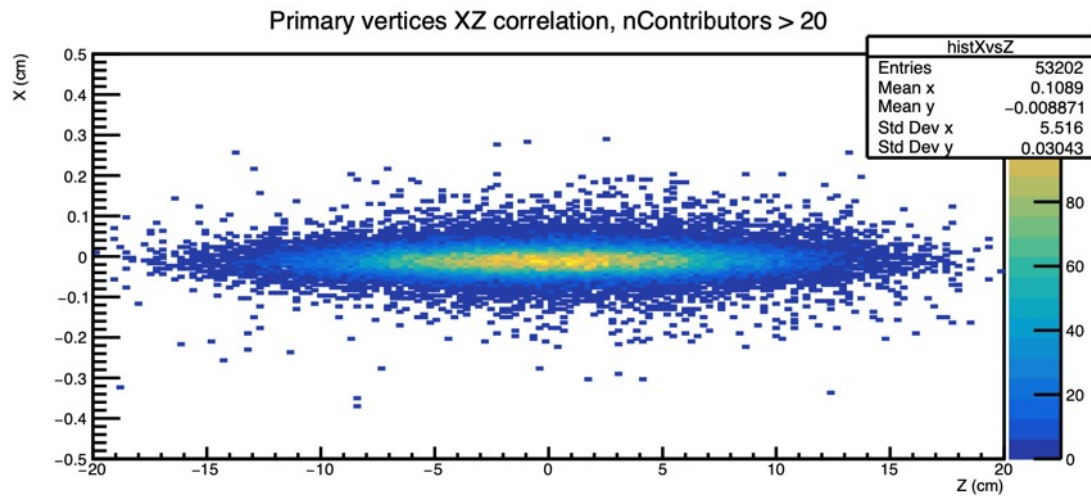
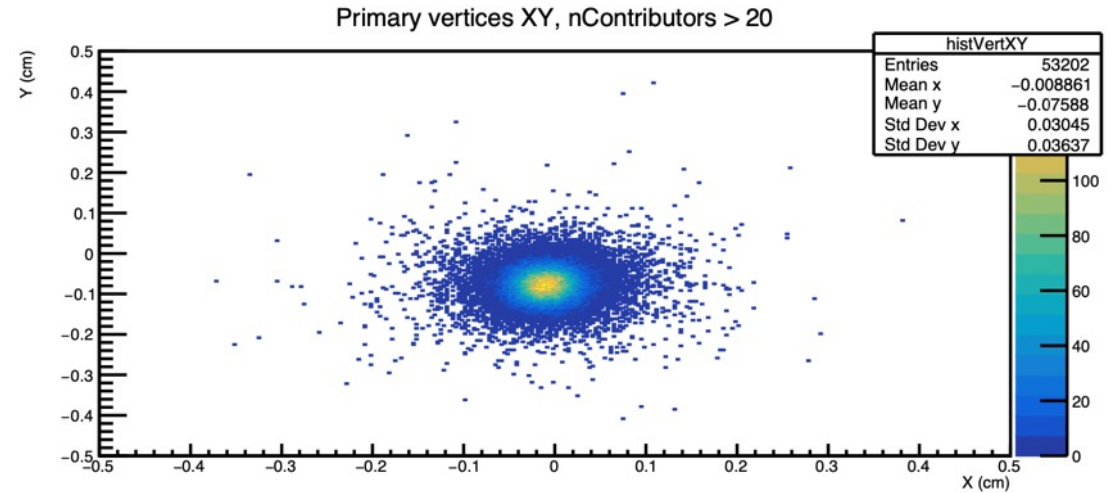
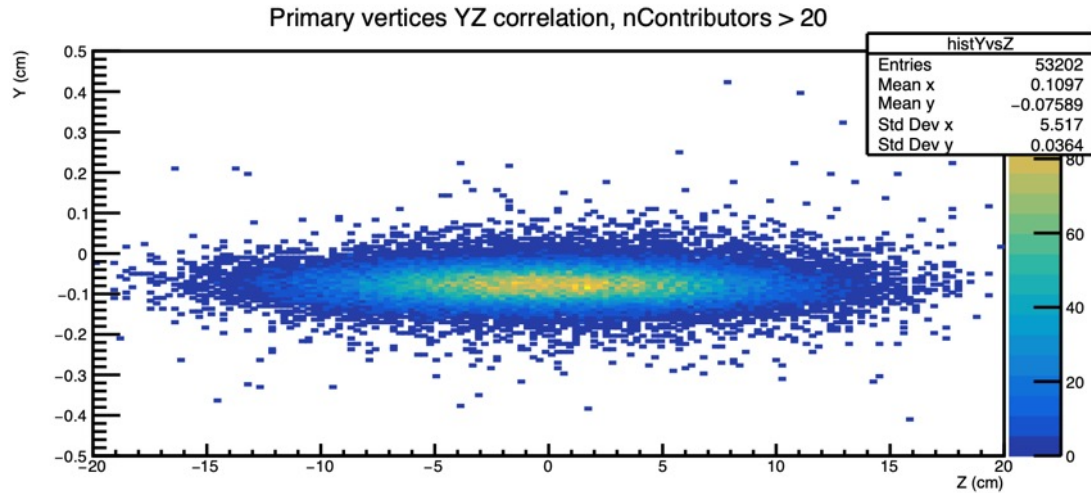
ALICE



Power and Readout System Overview

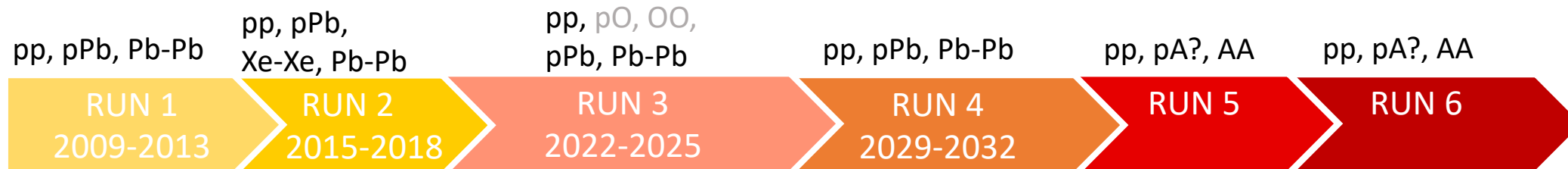


Vertex reconstruction



Collision systems

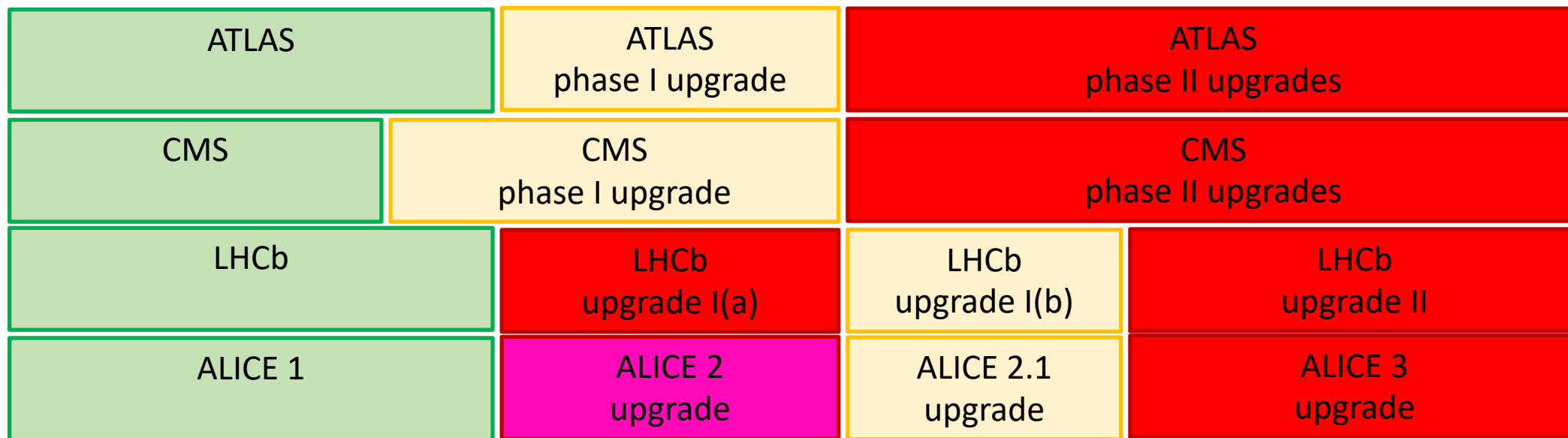
LHC schedule



High luminosity for ions ($\sim 7 \cdot 10^{27} \text{ cm}^{-2} \text{ s}^{-1}$)

HL-LHC ($\sim 5-7.5 \cdot 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$)

Higher luminosities for ions



intermediate upgrade

major upgrade

ALICE2 UPGRADE: ITS + MFT



ALICE

Inner Tracking System

GOALS:

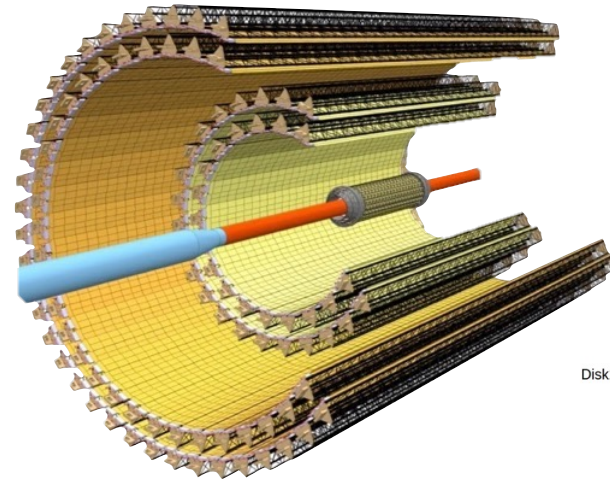
- improve pointing resolution
 - reduced material
 - closer to IP (39mm -> 22mm)
 - better spatial resolution (-> $5 \times 5 \mu\text{m}^2$)
- faster readout (1->100kHz)

Detector layout

- **Inner Barrel:** 3 layers, 48 staves
- **Outer Barrel:** 4 layers, 144 staves

In total **~24000 chips** = 12.5 Gpixels

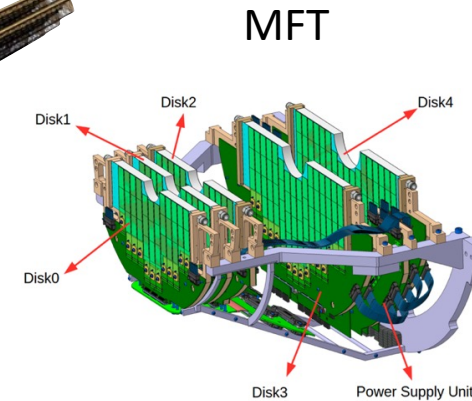
~10m² of silicon pixel sensors



ITS

Technology:

- CMOS sensors (ALPIDE)



MFT



ITS Inner and outer barrels + MFT disk 0 during installation

Muon Forward Tracker

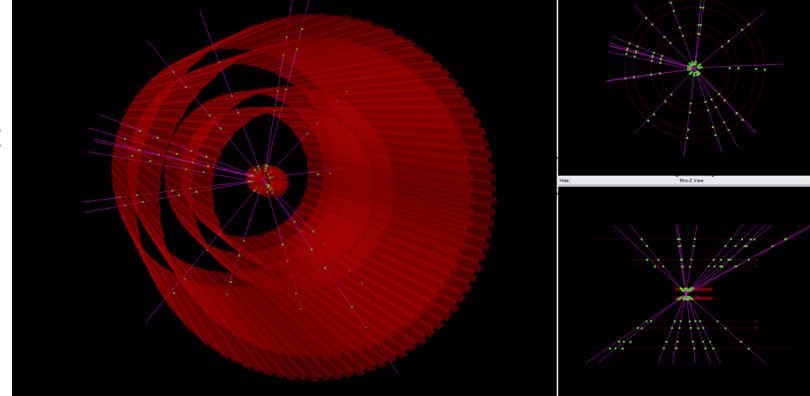
GOALS:

- add capabilities for secondary vertex measurement at forward rapidity

Detector layout

- upstream of the absorber
- **10 half-disks**, 2 detection planes each
- 280 ladders of 25 sensors each: **920 chips (0.4 m²)**

First p-p collisions during pilot beam, October 2021



ALICE

TED shots in ITS and MFT, April 2022

