

Status of WP2 (On-detector power distribution)

F.Faccio, S.Michelis, G.Blanchot, C.Fuentes, B.Allongue

- decrease in manpower as from Jan 1st with departure of S.Orlandi (fellow)

Outline

- ASIC
 - ✦ Technology
 - ✦ Design
- Full converter boards
 - ✦ Air-core inductor
 - ✦ Low-noise board design
 - ✦ Integration in detector systems

ASIC design

| | AMIS2 |
|----------------------|-----------|
| Full control loop | ✓ |
| Dead times' handling | Fixed |
| On-chip regulator | No |
| Soft Start | Simple RC |
| Over-I protection | No |
| Over-T protection | No |
| Under-V disable | No |

ASIC design

| | AMIS2 | IHP1 |
|----------------------|-----------|----------------------------|
| Full control loop | ✓ | ✓ |
| Dead times' handling | Fixed | Adaptive (QSW) |
| On-chip regulator | No | No |
| Soft Start | Simple RC | Simple RC with comparators |
| Over-I protection | No | No |
| Over-T protection | No | No |
| Under-V disable | No | No |

ASIC design

| | AMIS2 | IHP1 | IHP2 |
|----------------------|-----------|----------------------------|--------------------------------|
| Full control loop | ✓ | ✓ | ✓ |
| Dead times' handling | Fixed | Adaptive (QSW) | Adaptive (QSW and CCM, sharp) |
| On-chip regulator | No | No | ✓ |
| Soft Start | Simple RC | Simple RC with comparators | Full sequence with comparators |
| Over-I protection | No | No | ✓ |
| Over-T protection | No | No | No |
| Under-V disable | No | No | No |

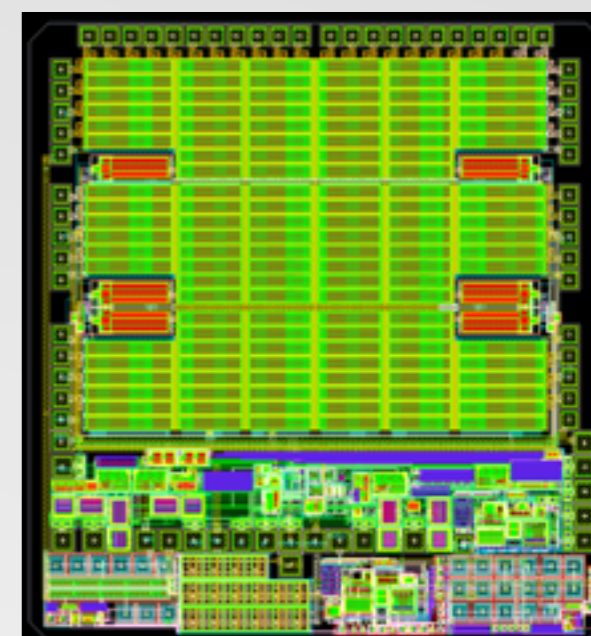
ASIC design

| | AMIS2 | IHP1 | IHP2 | AMIS3 |
|----------------------|-----------|----------------------------|--------------------------------|-----------|
| Full control loop | ✓ | ✓ | ✓ | ✓ |
| Dead times' handling | Fixed | Adaptive (QSW) | Adaptive (QSW and CCM, sharp) | Fixed |
| On-chip regulator | No | No | ✓ | ✓ |
| Soft Start | Simple RC | Simple RC with comparators | Full sequence with comparators | Simple RC |
| Over-I protection | No | No | ✓ | No |
| Over-T protection | No | No | No | No |
| Under-V disable | No | No | No | No |

ASIC design

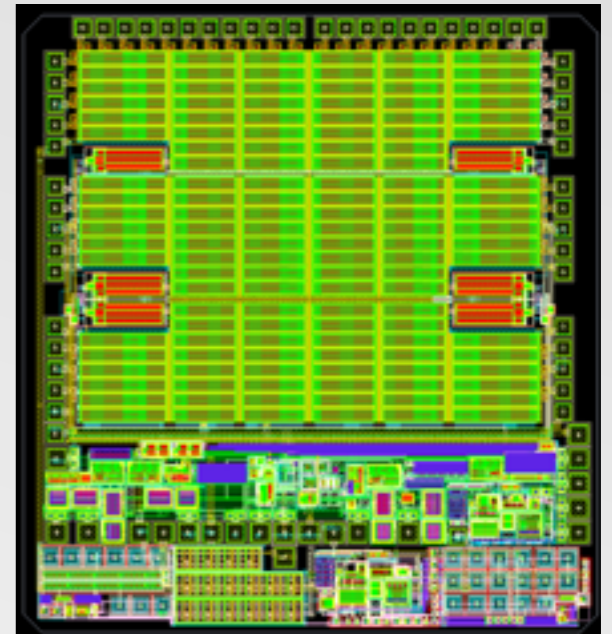
| | AMIS2 | IHP1 | IHP2 | AMIS3 | AMIS4 |
|----------------------|-----------|----------------------------|--------------------------------|-----------|--------------------------------|
| Full control loop | ✓ | ✓ | ✓ | ✓ | ✓ |
| Dead times' handling | Fixed | Adaptive (QSW) | Adaptive (QSW and CCM, sharp) | Fixed | Adaptive (QSW and CCM, smooth) |
| On-chip regulator | No | No | ✓ | ✓ | ✓ |
| Soft Start | Simple RC | Simple RC with comparators | Full sequence with comparators | Simple RC | State machine |
| Over-I protection | No | No | ✓ | No | ✓ |
| Over-T protection | No | No | No | No | ✓ |
| Under-V disable | No | No | No | No | ✓ |

AMIS3



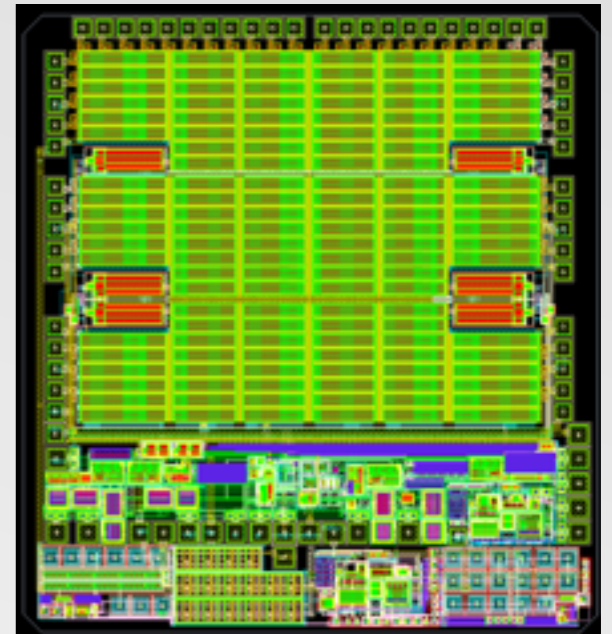
AMIS3

- Converter identical to AMIS2, but with the only addition of on-chip Linear Voltage Regulator to provide 3.3V from the unique input line (10V)



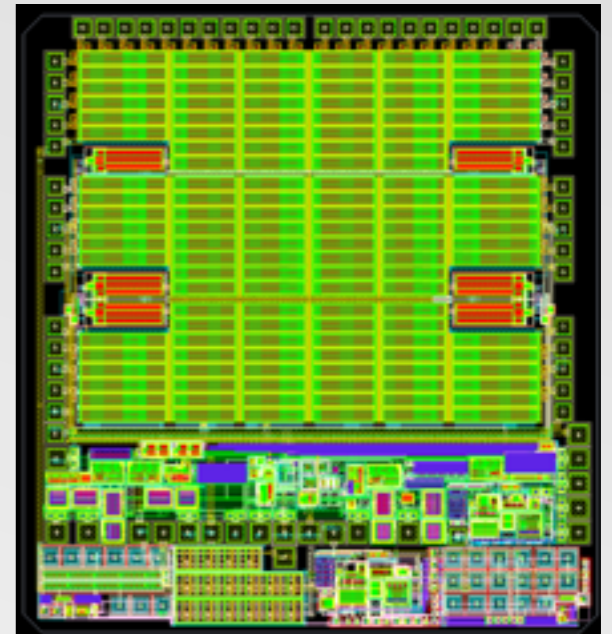
AMIS3

- Converter identical to AMIS2, but with the only addition of on-chip Linear Voltage Regulator to provide 3.3V from the unique input line (10V)
- Quickly prepared by S.Michelis after TWEPP and submitted for manufacturing in October 2010



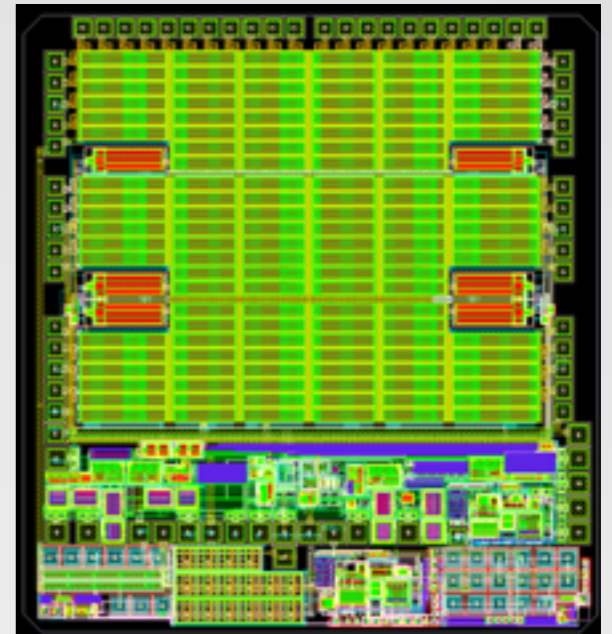
AMIS3

- Converter identical to AMIS2, but with the only addition of on-chip Linear Voltage Regulator to provide 3.3V from the unique input line (10V)
- Quickly prepared by S.Michelis after TWEPP and submitted for manufacturing in October 2010
- Expected delivery: mid-March



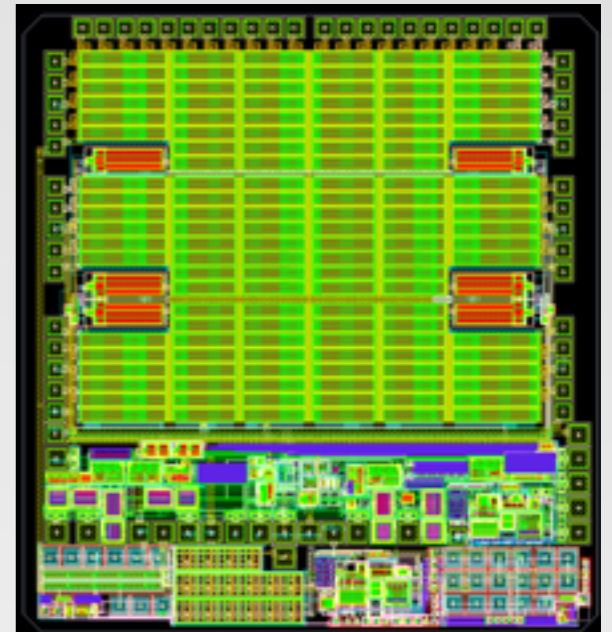
AMIS3

- Converter identical to AMIS2, but with the only addition of on-chip Linear Voltage Regulator to provide 3.3V from the unique input line (10V)
- Quickly prepared by S.Michelis after TWEPP and submitted for manufacturing in October 2010
- Expected delivery: mid-March
- Purpose:



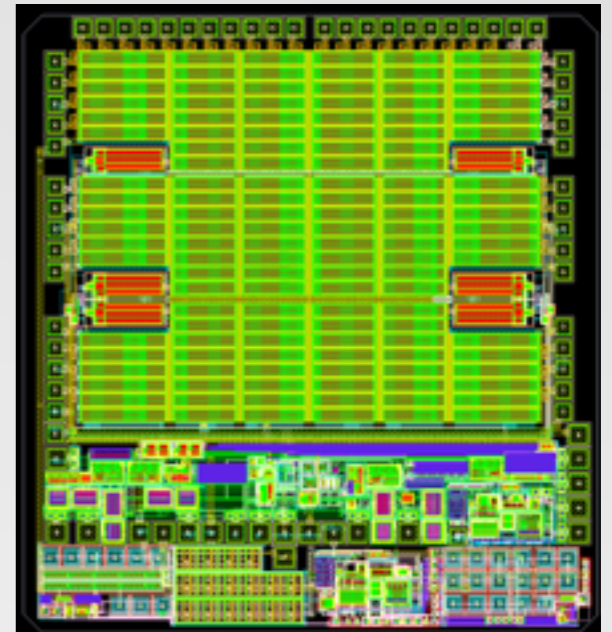
AMIS3

- Converter identical to AMIS2, but with the only addition of on-chip Linear Voltage Regulator to provide 3.3V from the unique input line (10V)
- Quickly prepared by S.Michelis after TWEPP and submitted for manufacturing in October 2010
- Expected delivery: mid-March
- Purpose:
 - ❖ Test again On-Semi hardware (AMIS2 manufactured in first semester 2009), especially radiation



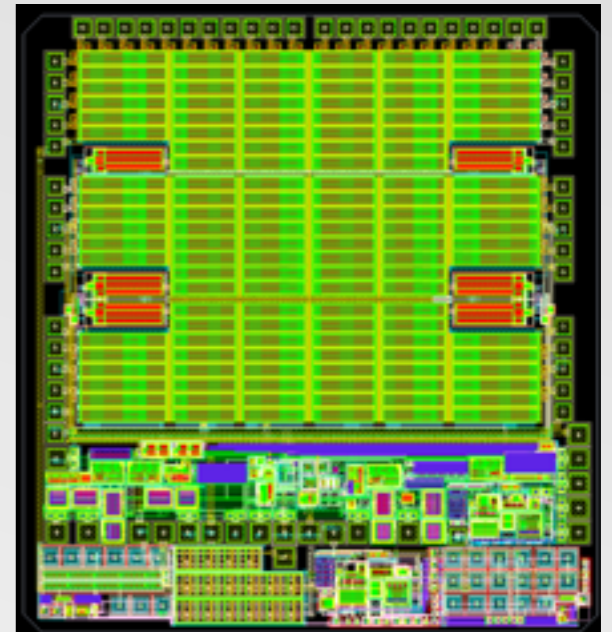
AMIS3

- Converter identical to AMIS2, but with the only addition of on-chip Linear Voltage Regulator to provide 3.3V from the unique input line (10V)
- Quickly prepared by S.Michelis after TWEPP and submitted for manufacturing in October 2010
- Expected delivery: mid-March
- Purpose:
 - ❖ Test again On-Semi hardware (AMIS2 manufactured in first semester 2009), especially radiation
 - ❖ Provide a working rad-tol converter not needing external regulator to colleagues working on system integration

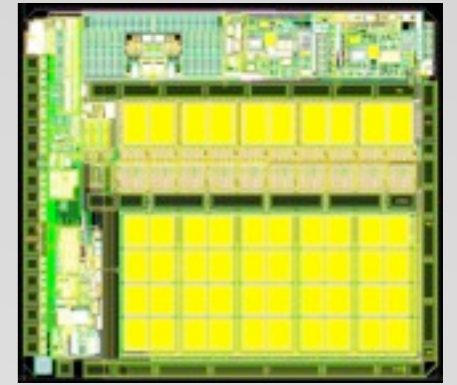


AMIS3

- Converter identical to AMIS2, but with the only addition of on-chip Linear Voltage Regulator to provide 3.3V from the unique input line (10V)
- Quickly prepared by S.Michelis after TWEPP and submitted for manufacturing in October 2010
- Expected delivery: mid-March
- Purpose:
 - ❖ Test again On-Semi hardware (AMIS2 manufactured in first semester 2009), especially radiation
 - ❖ Provide a working rad-tol converter not needing external regulator to colleagues working on system integration
- Packaged in QFN32 for system testing (as AMIS2)



AMIS4



- Internal BGP ref (as AMIS2) and Linear Voltage Regulators to provide on-chip 3.3V from unique input rail
- Integrated feedback loop with bandwidth of 100Khz - can be lowered with external passives
- Internal oscillator fixed at 2MHz, tunable with external components
- Vout set to 2.5V, tunable with external components
- Protection features:
 - ❖ SEU-protected state machine rules entrance and exit from failure states and beginning of Soft Start (about 2ms long)
 - ❖ Under-voltage detection at the input enables converter only above 5V
 - ❖ Over-T detection turns off the converter when on-chip T exceeds 100C
 - ❖ Over-current detection is implemented on a cycle-by-cycle basis, and limits max current on HS transistor on each cycle. After 32 consecutive detections (synchronous with clock), the converter is reset and a Soft Start begins
- Other features:
 - ❖ Enable pin to turn on-off the converter
 - ❖ Power good output flag (only asserted during 'good' state of the converter, with regulated Vout)
- Chip Size: ~2.875 x 2.55 mm²
- Packaged in QFN-EP 32 (first lot in QFN48 for functional test)
- To reduce parasitic resistance, unusual bonding configuration chosen (pads in the middle of the chip). Discussions on-going via IMEC with packaging house (ASE) to find appropriate, cheap and reliable assembly
- Submitted to IMEC MPW on January 24th. Purchase of 1 extra wafer should ensure availability of at least 100 parts (probably more)
- We expect testing in summer

“Behavioral” model for the converter

“Behavioral” model for the converter

- A simplified model for the converter has been developed in the Simetrix Simplis simulation tool

“Behavioral” model for the converter

- A simplified model for the converter has been developed in the Simetrix Simplis simulation tool
 - ✦ It contains all features of the AMIS4 ASIC

“Behavioral” model for the converter

- A simplified model for the converter has been developed in the Simetrix Simplis simulation tool
 - ✦ It contains all features of the AMIS4 ASIC
 - ✦ It was very useful for the design of the protection scheme (quick full simulation of the full converter enables prompt detection of potential conflicts)

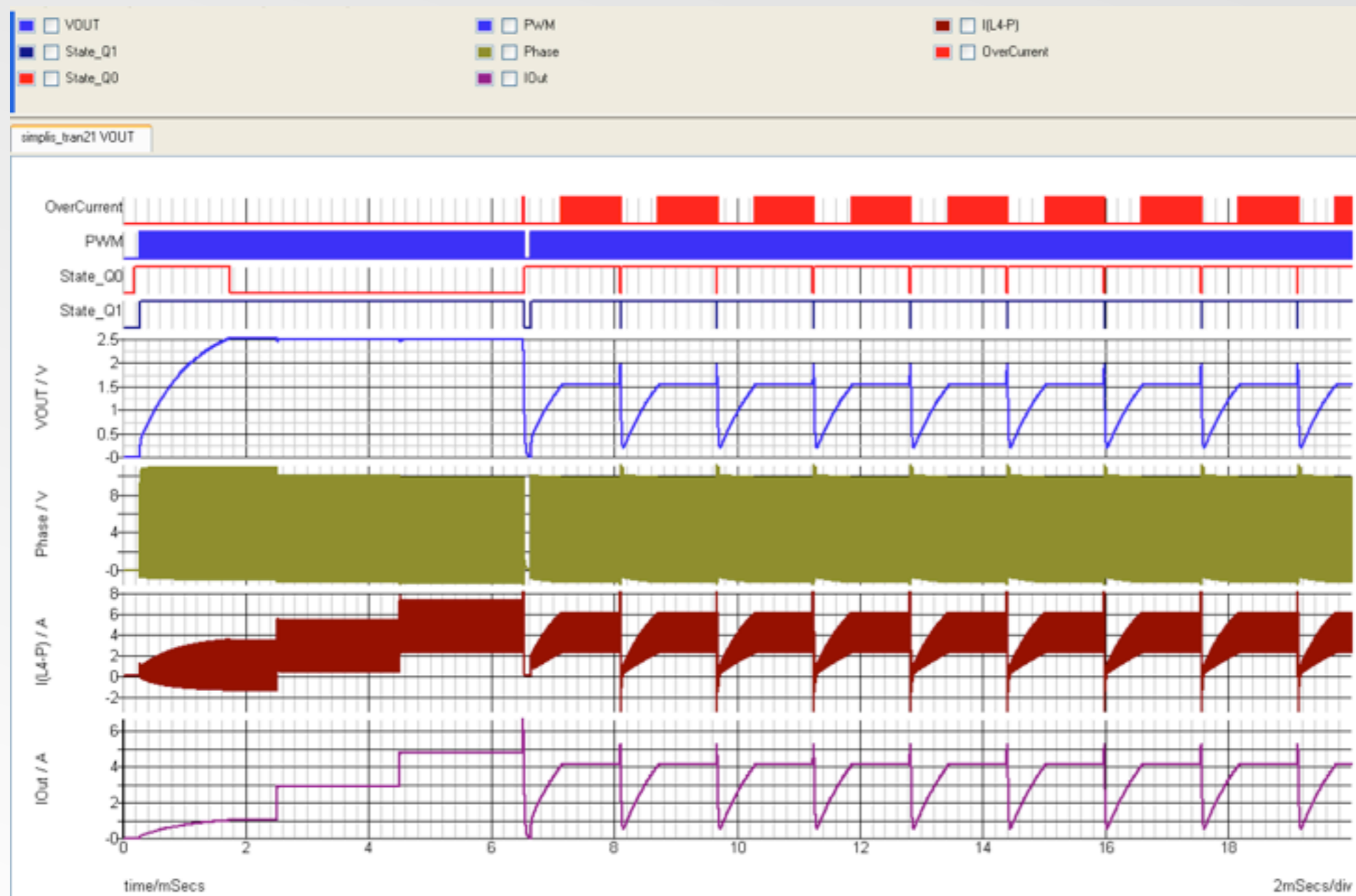
“Behavioral” model for the converter

- A simplified model for the converter has been developed in the Simetrix Simplis simulation tool
 - ❖ It contains all features of the AMIS4 ASIC
 - ❖ It was very useful for the design of the protection scheme (quick full simulation of the full converter enables prompt detection of potential conflicts)
 - ❖ It is used to simulate the full converter - including in and out filters - and analyze the transient behavior at start-up and shut down, and in case of under-voltage or over-current

“Behavioral” model for the converter

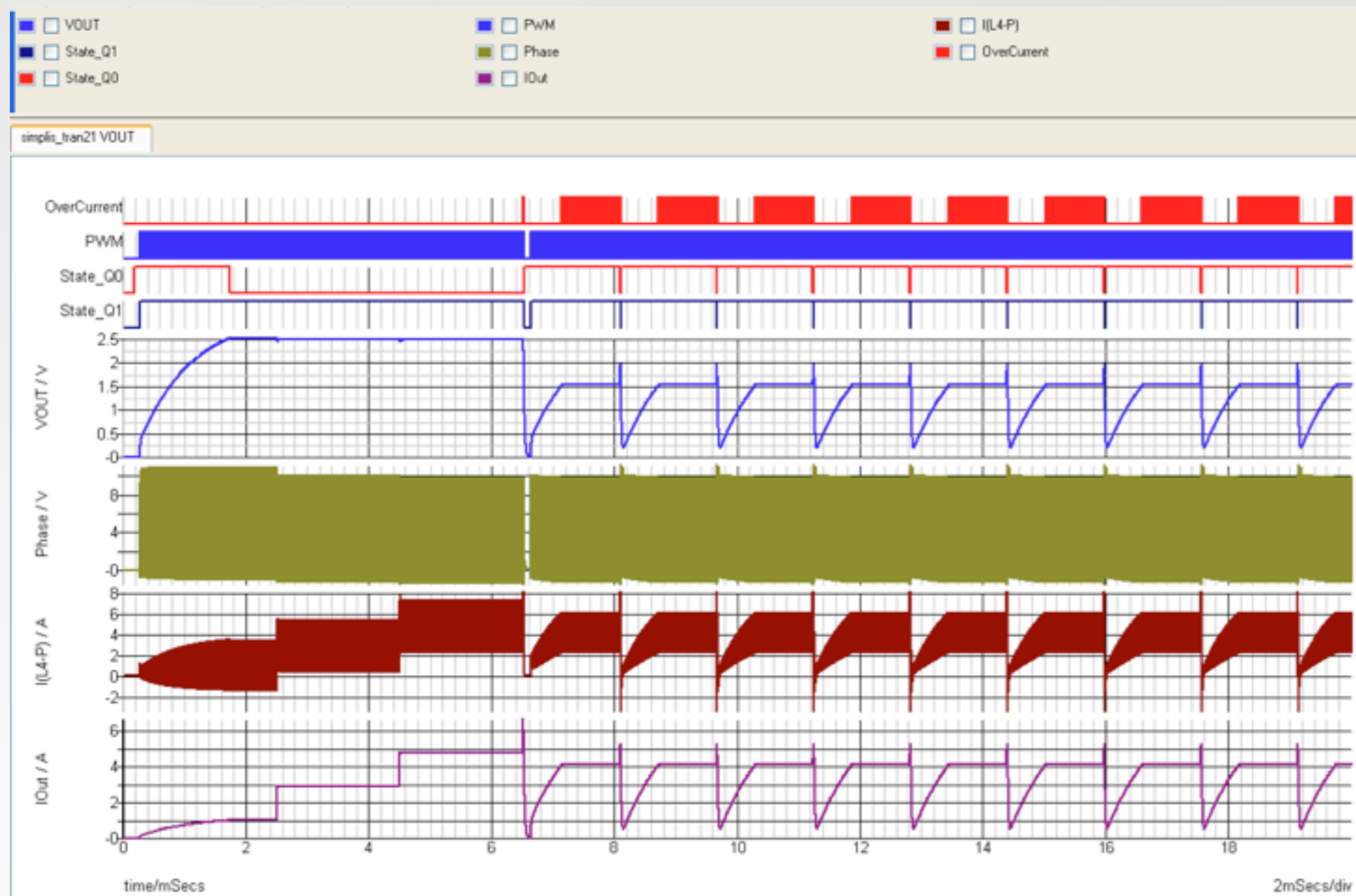
- A simplified model for the converter has been developed in the Simetrix Simplis simulation tool
 - ❖ It contains all features of the AMIS4 ASIC
 - ❖ It was very useful for the design of the protection scheme (quick full simulation of the full converter enables prompt detection of potential conflicts)
 - ❖ It is used to simulate the full converter - including in and out filters - and analyze the transient behavior at start-up and shut down, and in case of under-voltage or over-current
 - ❖ It will be used to simulate the converter embedded in a detector system

“Behavioral” model for the converter

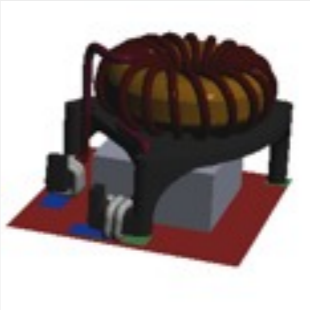
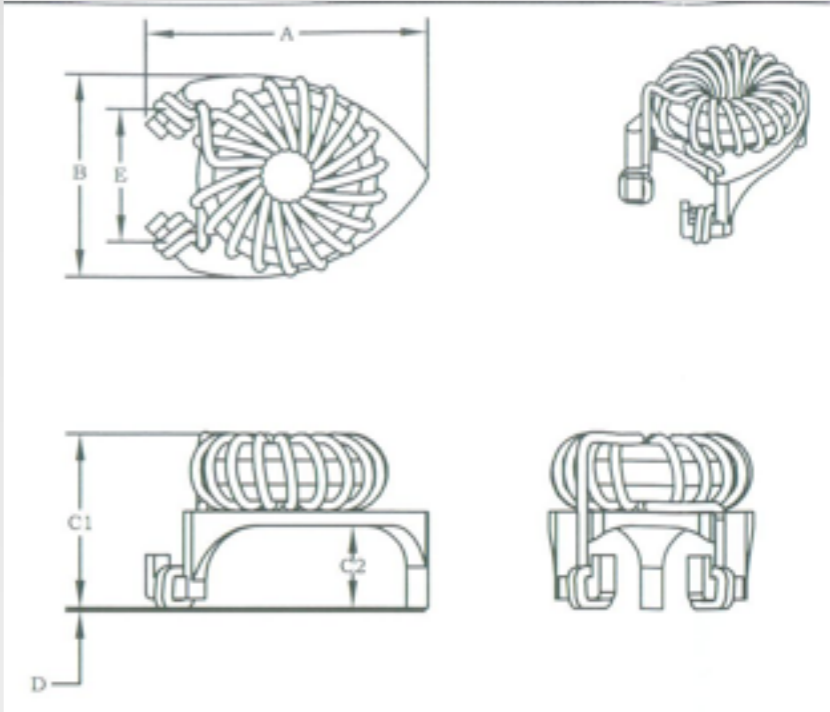


“Behavioral” model for the converter

- ❖ Example: start-up at 1A load followed by step-increases of 2A. At 7A, overcurrent protection is active.

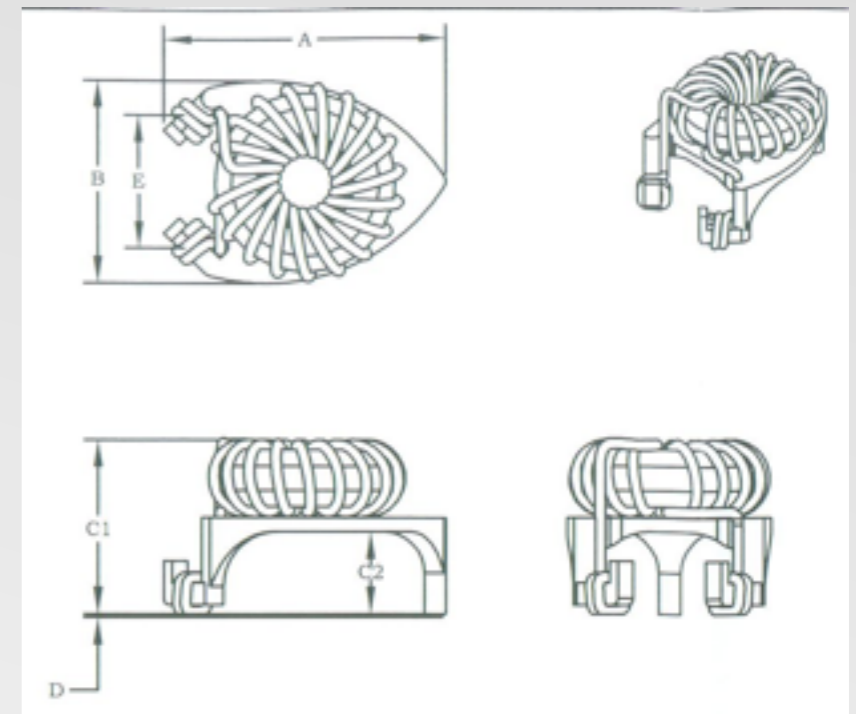


Air-core inductor



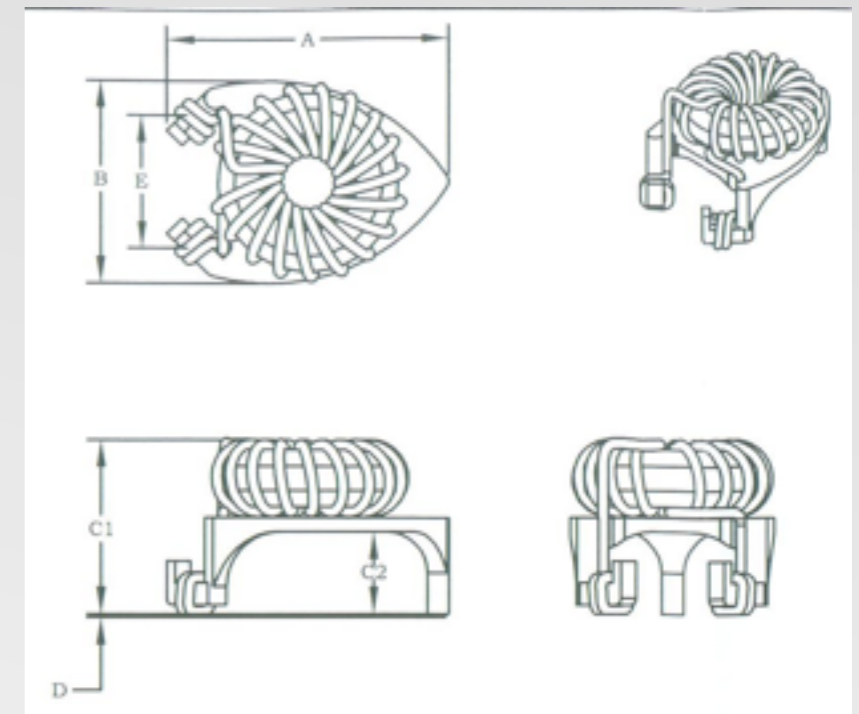
Air-core inductor

- Tolerance to B field imposes air core coils
 - ❖ Air core typical inductance values: 5-700 nH MAX



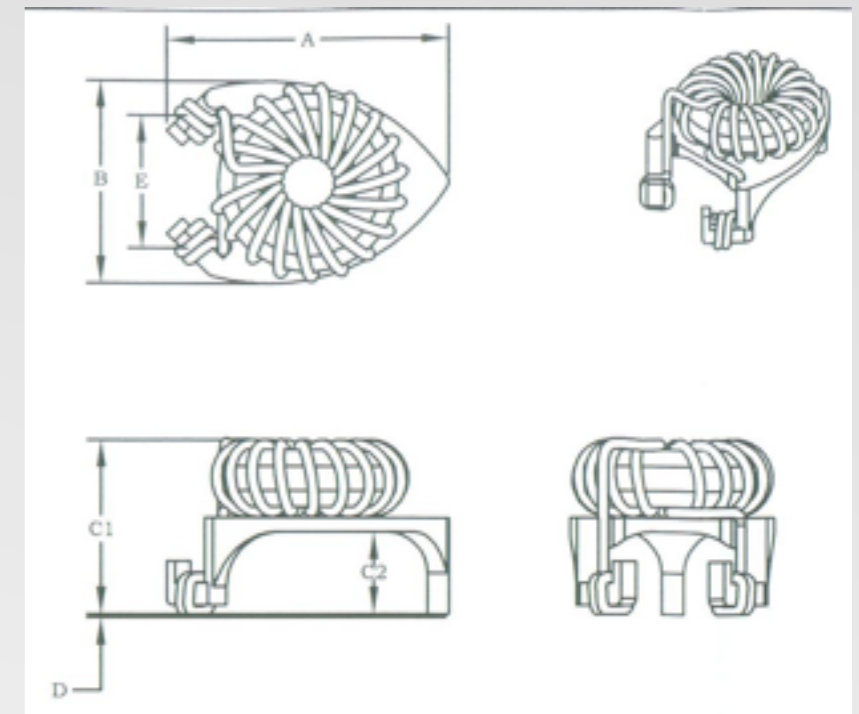
Air-core inductor

- Tolerance to B field imposes air core coils
 - ❖ Air core typical inductance values: 5-700 nH MAX
- Toroidal topology was selected in 2009
 - ❖ Compact geometry
 - ❖ Radiates significantly less magnetic field than other topologies
 - ❖ Air core toroidal inductors not available commercially: custom development enabled for mass production is required

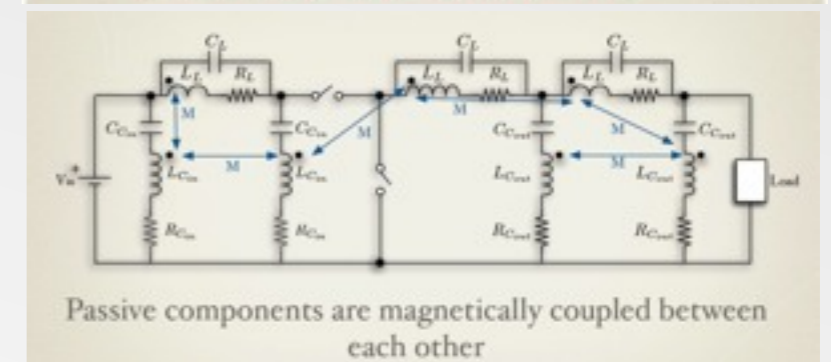
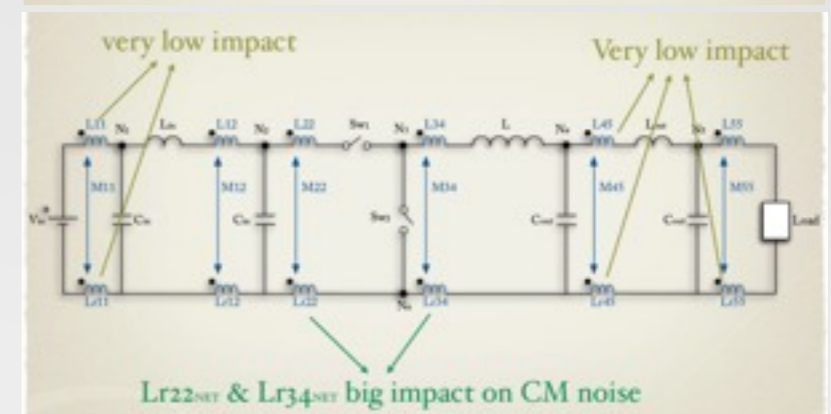
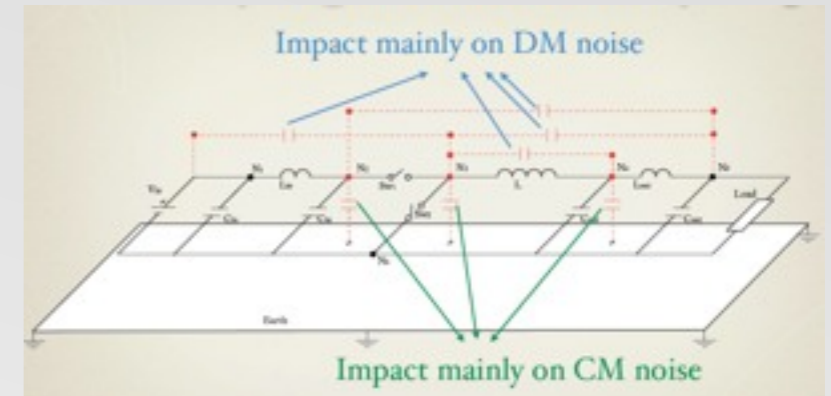


Air-core inductor

- Tolerance to B field imposes air core coils
 - ❖ Air core typical inductance values: 5-700 nH MAX
- Toroidal topology was selected in 2009
 - ❖ Compact geometry
 - ❖ Radiates significantly less magnetic field than other topologies
 - ❖ Air core toroidal inductors not available commercially: custom development enabled for mass production is required
- Development succeeded with Coilcraft:
 - ❖ 220nH/30m Ω air core toroid
 - ❖ Coil mounted on plastic stand-off to fit precisely above the converter ASIC
 - ❖ Prototypes delivered in 2010. One sample successfully radiation tested at PS (8E15 p/cm²)
 - ❖ Order for production of 500 samples issued, delivery end of March
 - ❖ Expected total mass: slightly less than 0.4g



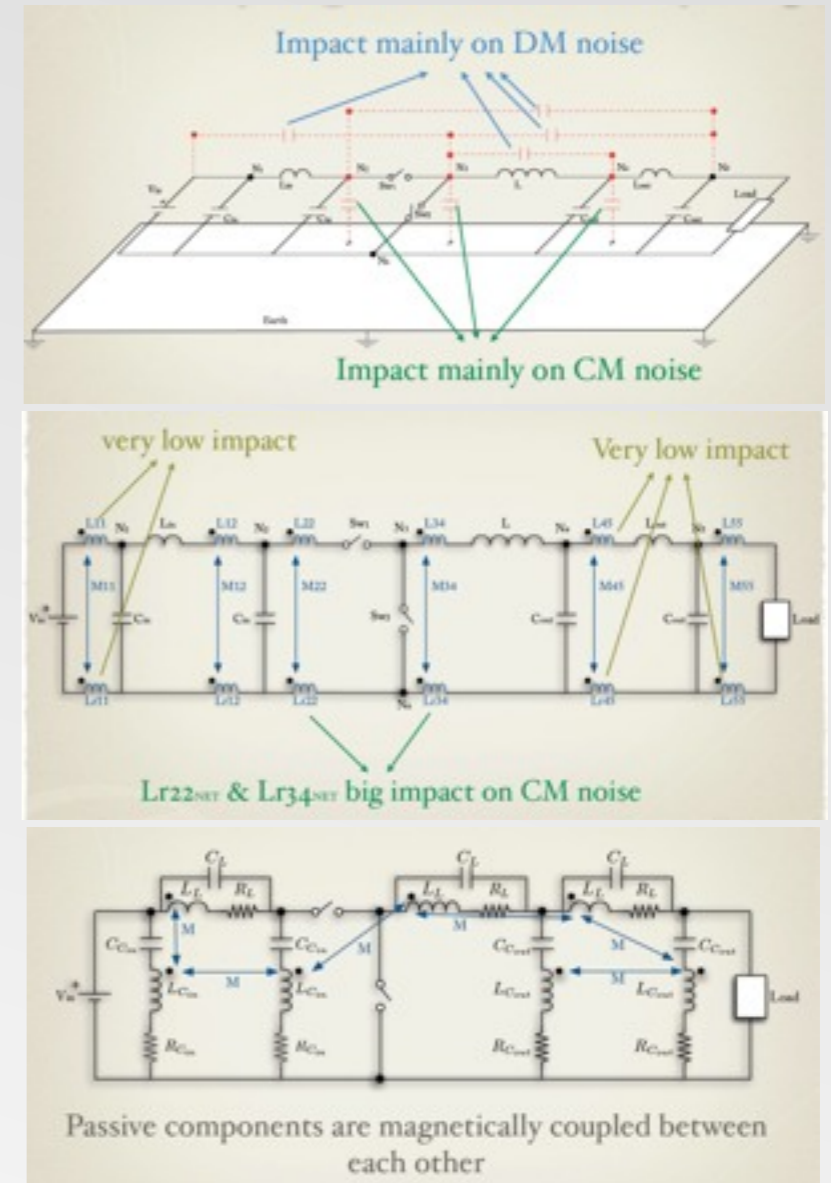
Optimization of full DCDC converter boards



C.Fuentes talk @ TWEPP

Optimization of full DCDC converter boards

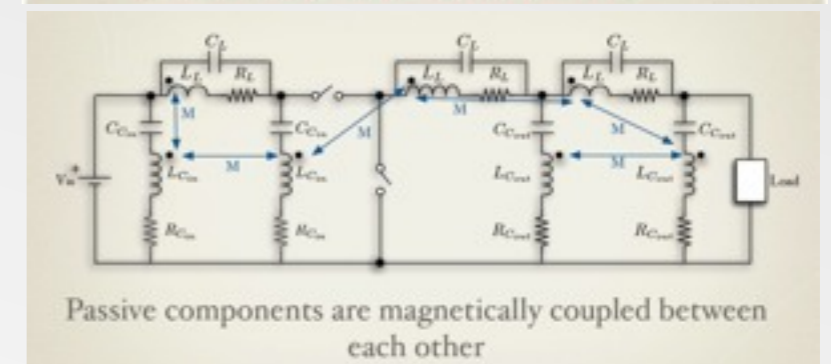
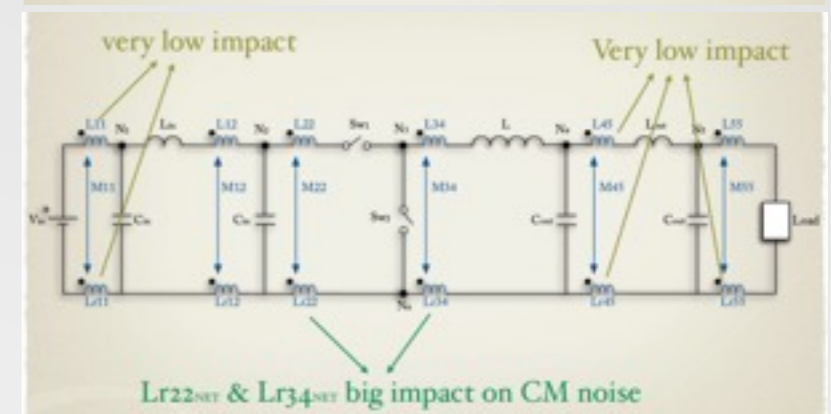
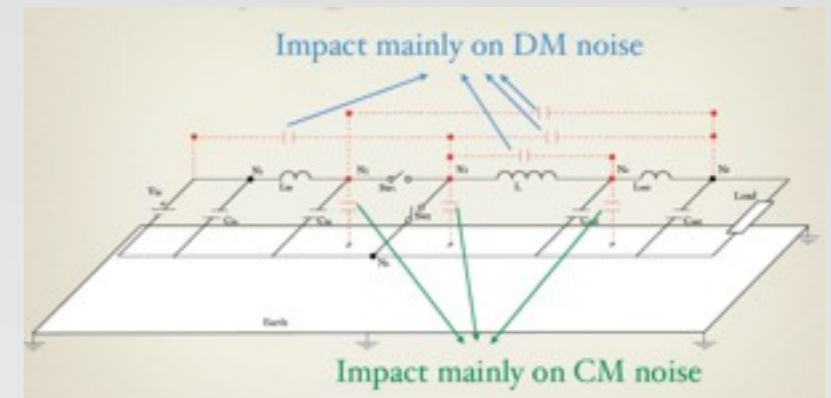
- Roadmap for EMC optimization of DCDCs



C.Fuentes talk @ TWEPP

Optimization of full DCDC converter boards

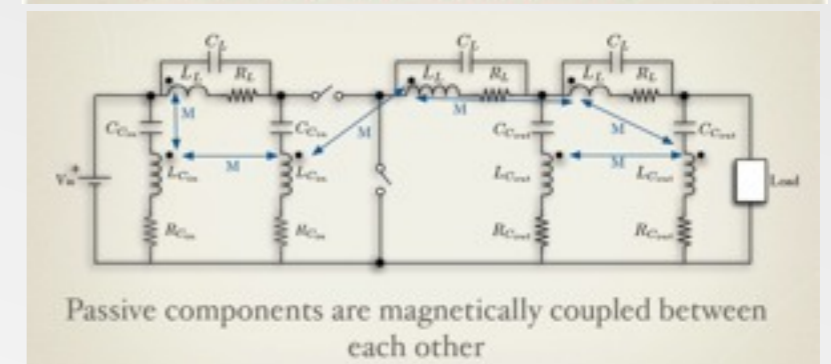
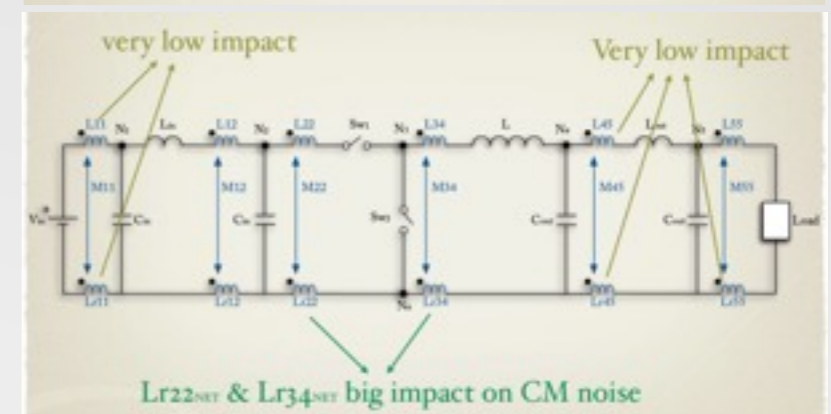
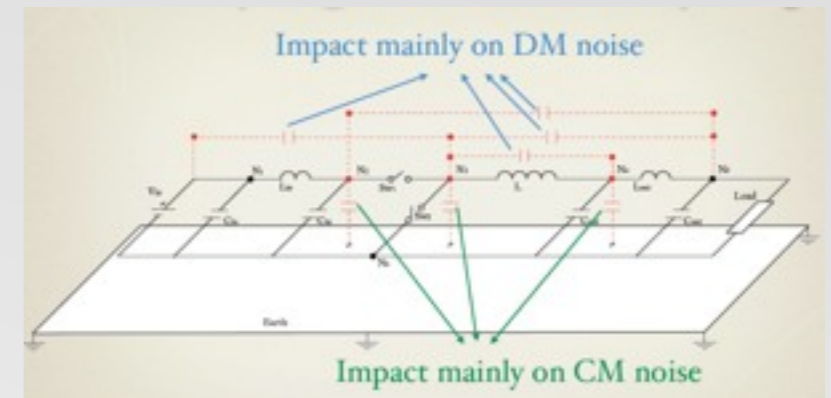
- Roadmap for EMC optimization of DCDCs
 - ❖ Critical stray capacitances identification.



C.Fuentes talk @ TWEPP

Optimization of full DCDC converter boards

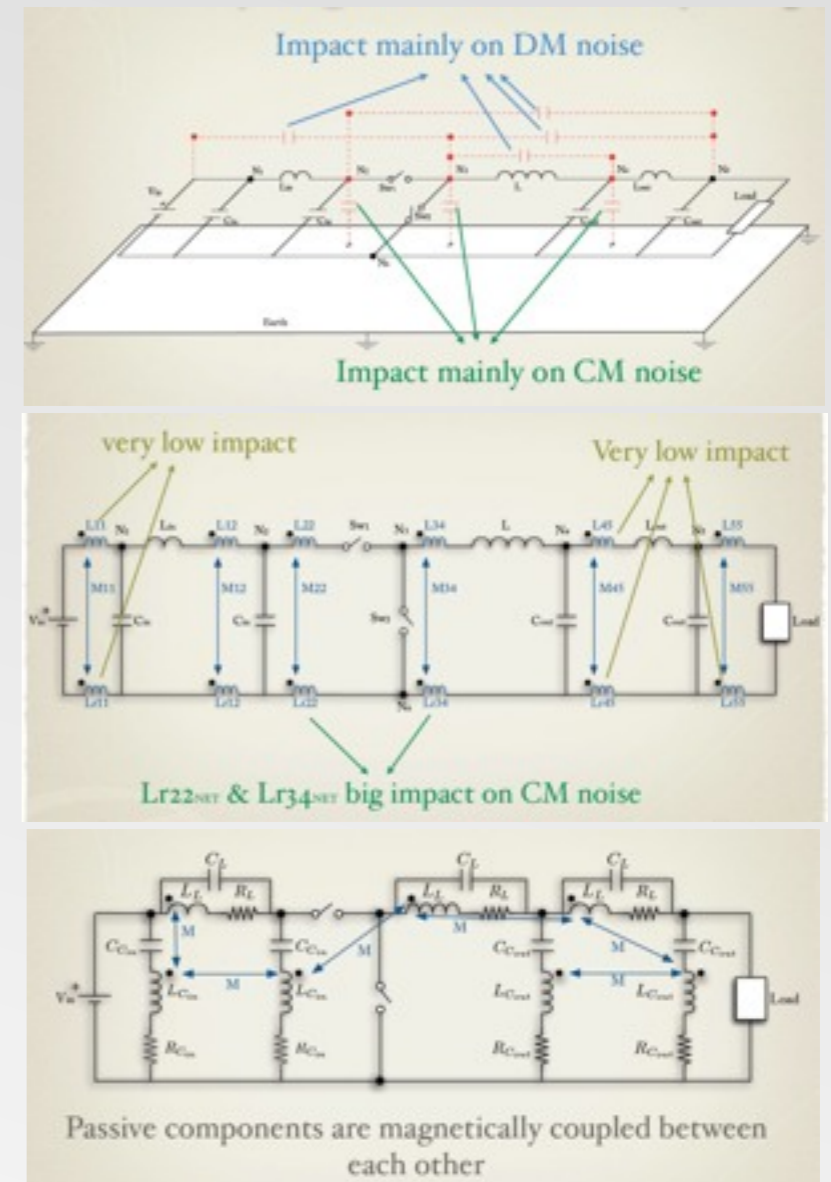
- Roadmap for EMC optimization of DCDCs
 - ❖ Critical stray capacitances identification.
 - ❖ Critical stray inductances identification.



C.Fuentes talk @ TWEPP

Optimization of full DCDC converter boards

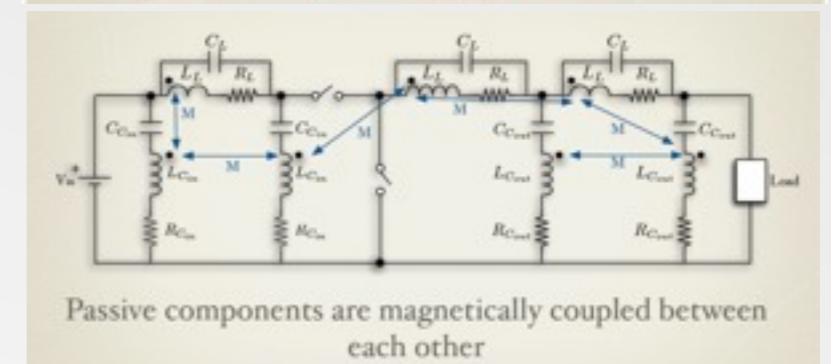
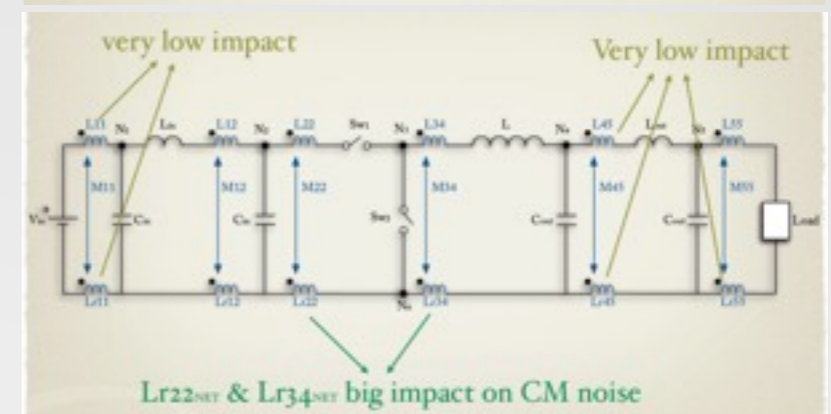
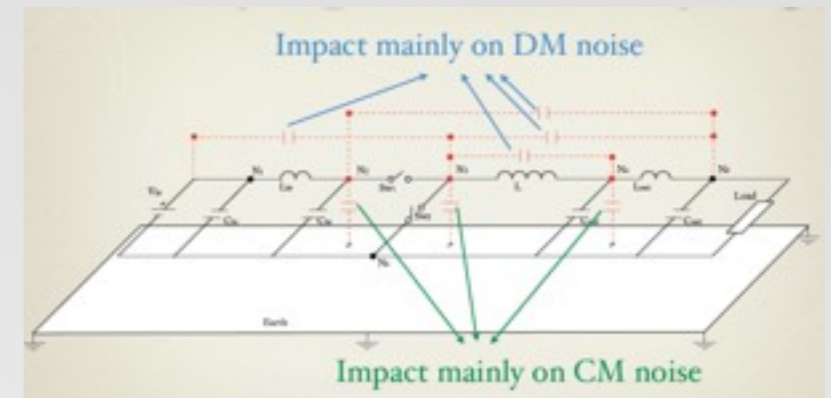
- Roadmap for EMC optimization of DCDCs
 - ❖ Critical stray capacitances identification.
 - ❖ Critical stray inductances identification.
 - ❖ On board parasitic magnetic couplings identification.



C.Fuentes talk @ TWEPP

Optimization of full DCDC converter boards

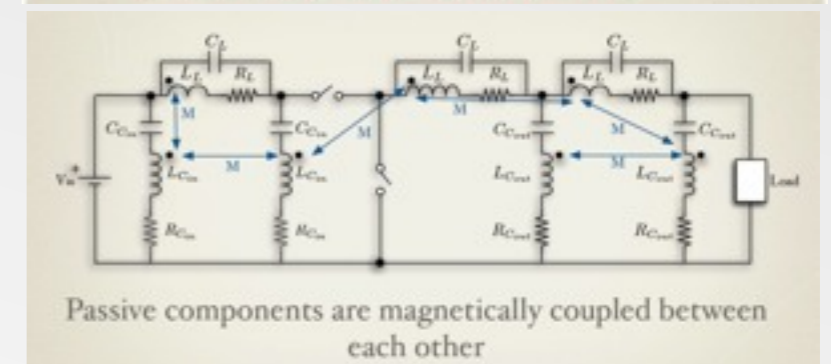
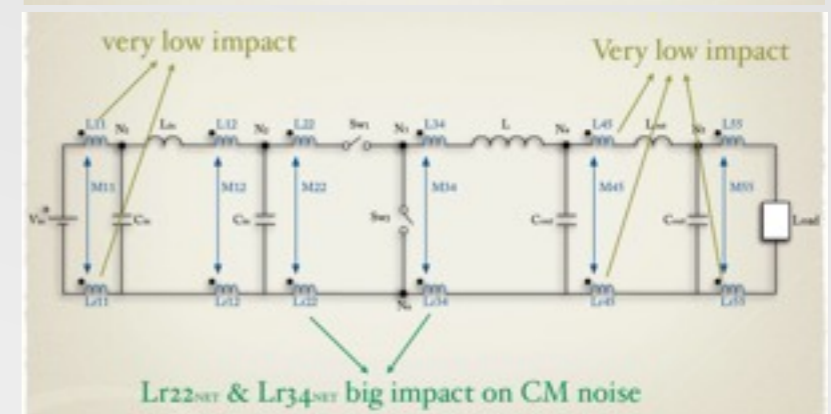
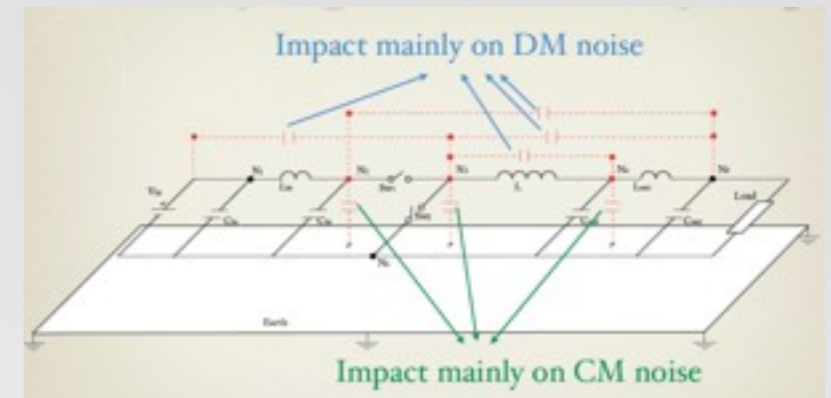
- Roadmap for EMC optimization of DCDCs
 - ❖ Critical stray capacitances identification.
 - ❖ Critical stray inductances identification.
 - ❖ On board parasitic magnetic couplings identification.
- Noise optimization of DCDCs :



C.Fuentes talk @ TWEPP

Optimization of full DCDC converter boards

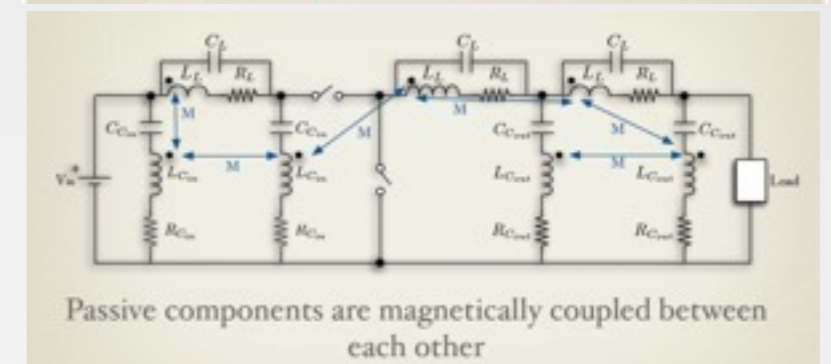
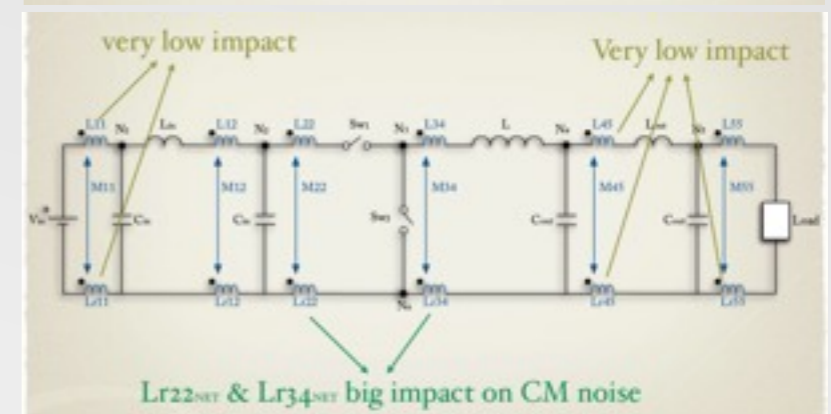
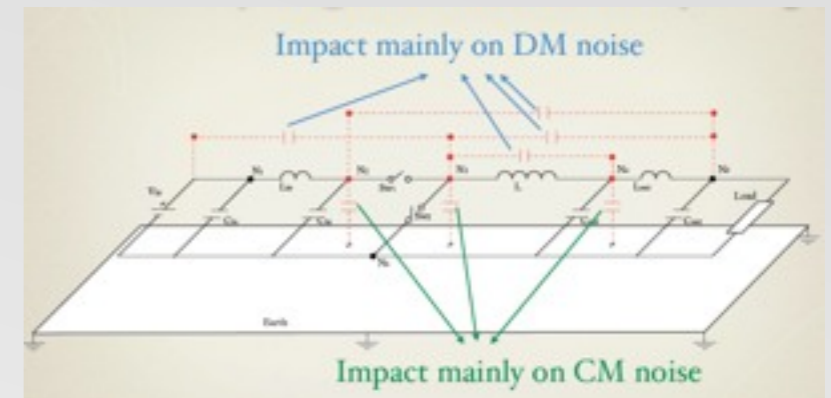
- Roadmap for EMC optimization of DCDCs
 - ❖ Critical stray capacitances identification.
 - ❖ Critical stray inductances identification.
 - ❖ On board parasitic magnetic couplings identification.
- Noise optimization of DCDCs :
 - ❖ Optimal placement of parts obtained through electromagnetic simulation of board layouts.



C.Fuentes talk @ TWEPP

Optimization of full DCDC converter boards

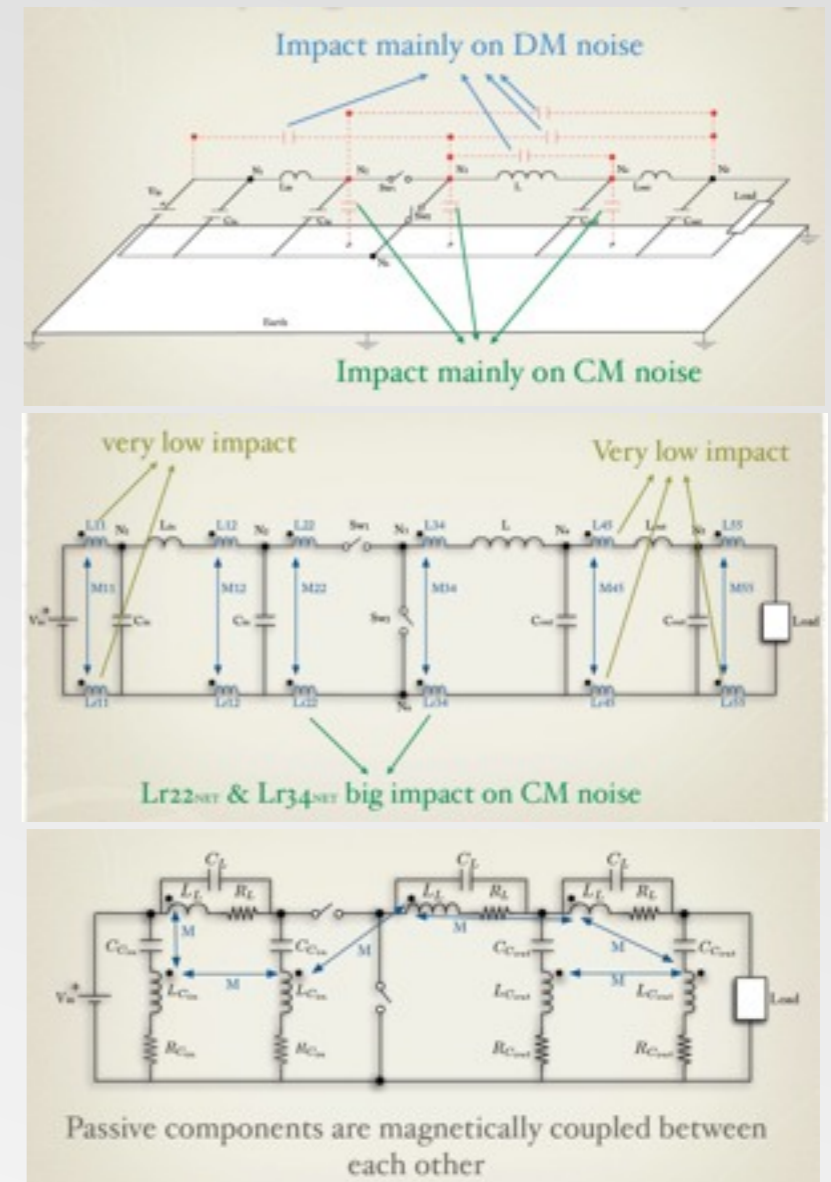
- Roadmap for EMC optimization of DCDCs
 - ❖ Critical stray capacitances identification.
 - ❖ Critical stray inductances identification.
 - ❖ On board parasitic magnetic couplings identification.
- Noise optimization of DCDCs :
 - ❖ Optimal placement of parts obtained through electromagnetic simulation of board layouts.
 - ❖ Optimal PCB layout structure that minimizes the critical stray capacitances and inductances.



C.Fuentes talk @ TWEPP

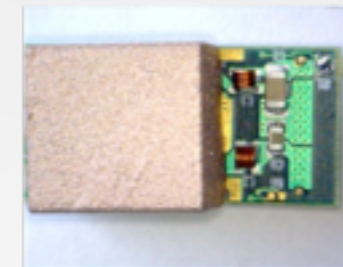
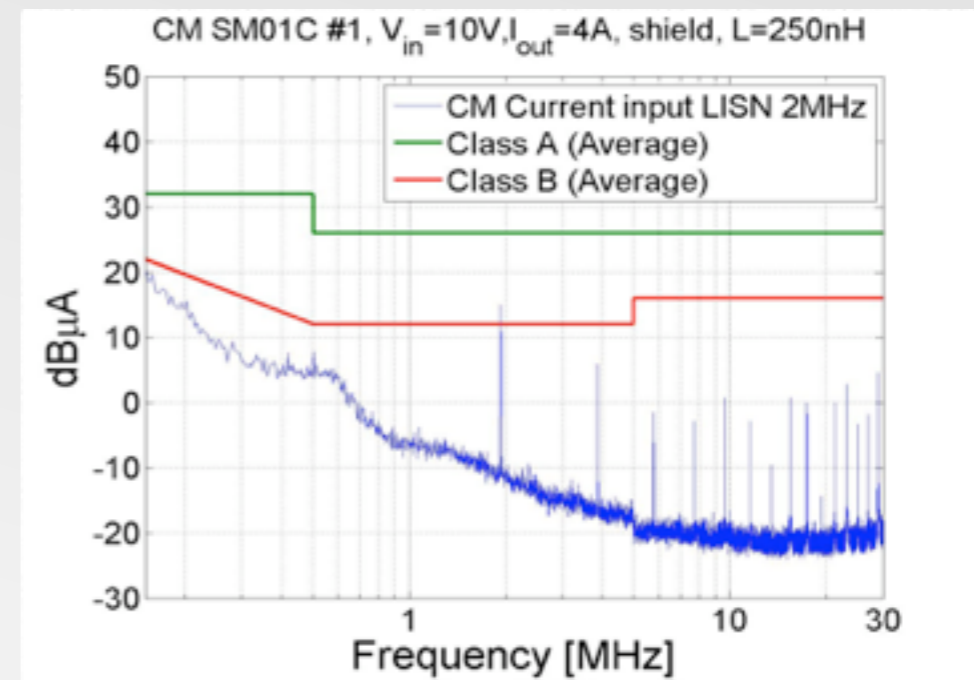
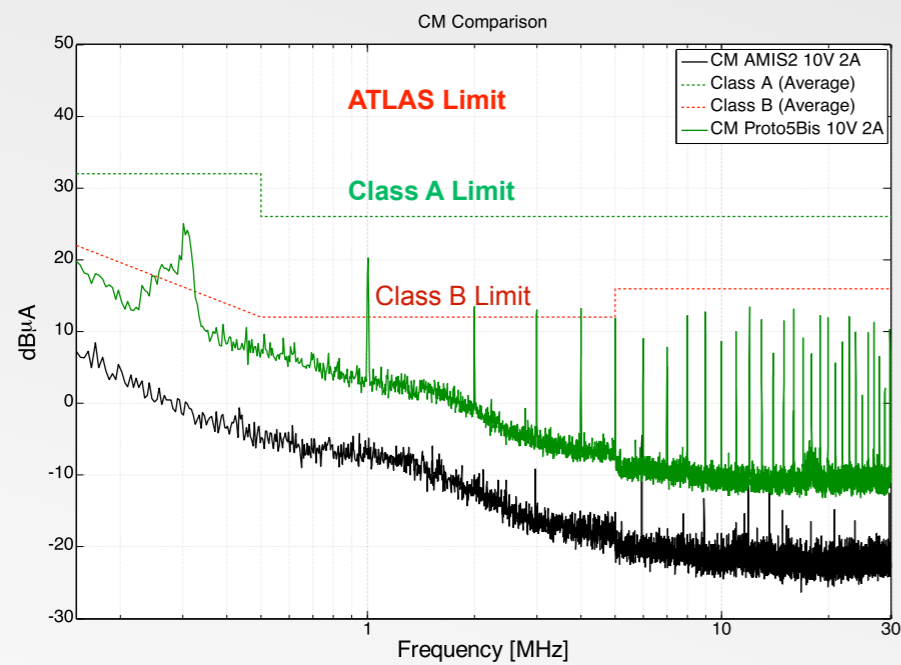
Optimization of full DCDC converter boards

- Roadmap for EMC optimization of DCDCs
 - ❖ Critical stray capacitances identification.
 - ❖ Critical stray inductances identification.
 - ❖ On board parasitic magnetic couplings identification.
- Noise optimization of DCDCs :
 - ❖ Optimal placement of parts obtained through electromagnetic simulation of board layouts.
 - ❖ Optimal PCB layout structure that minimizes the critical stray capacitances and inductances.
 - ❖ Addition of shield for segregation of noisy and quiet areas of PCB.



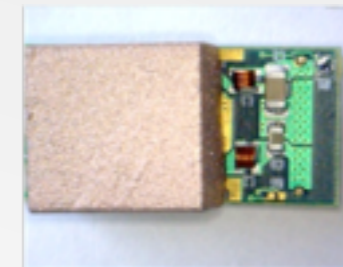
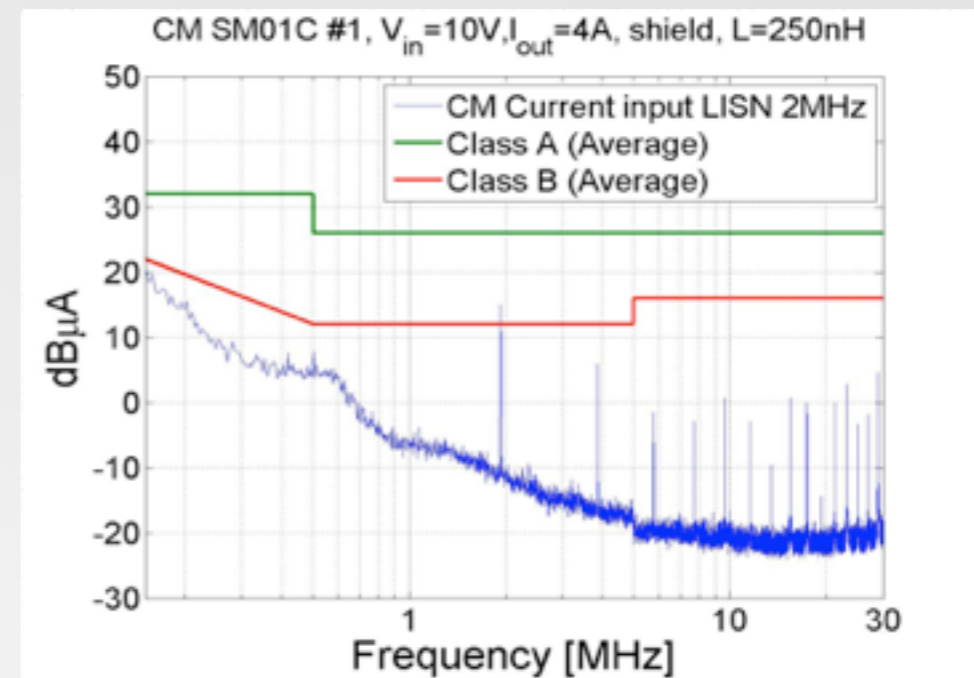
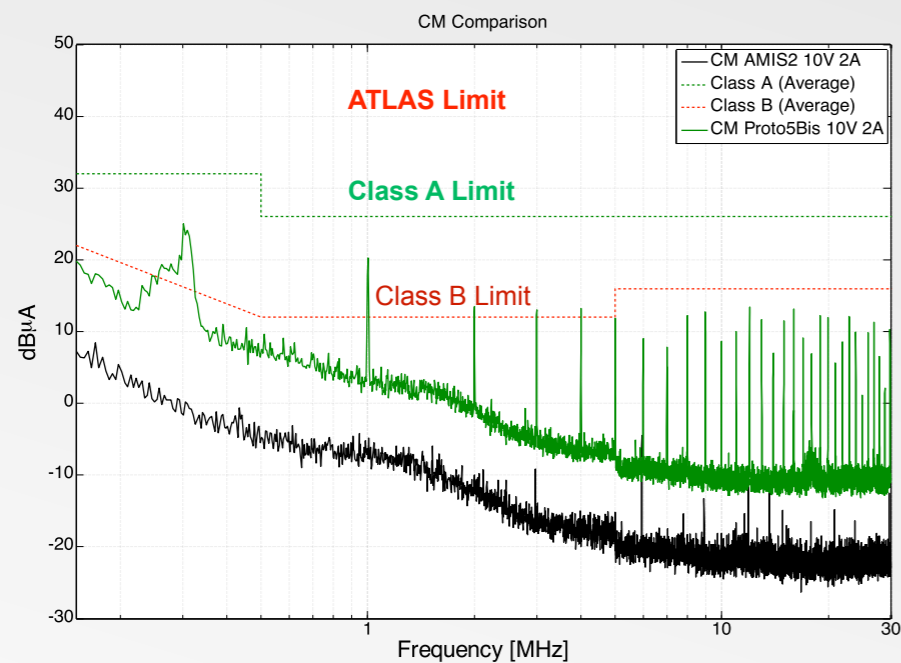
C.Fuentes talk @ TWEPP

Full converter boards



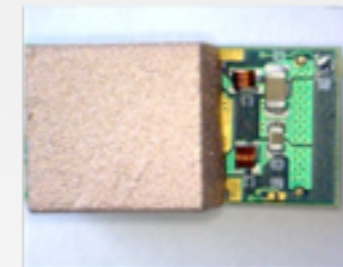
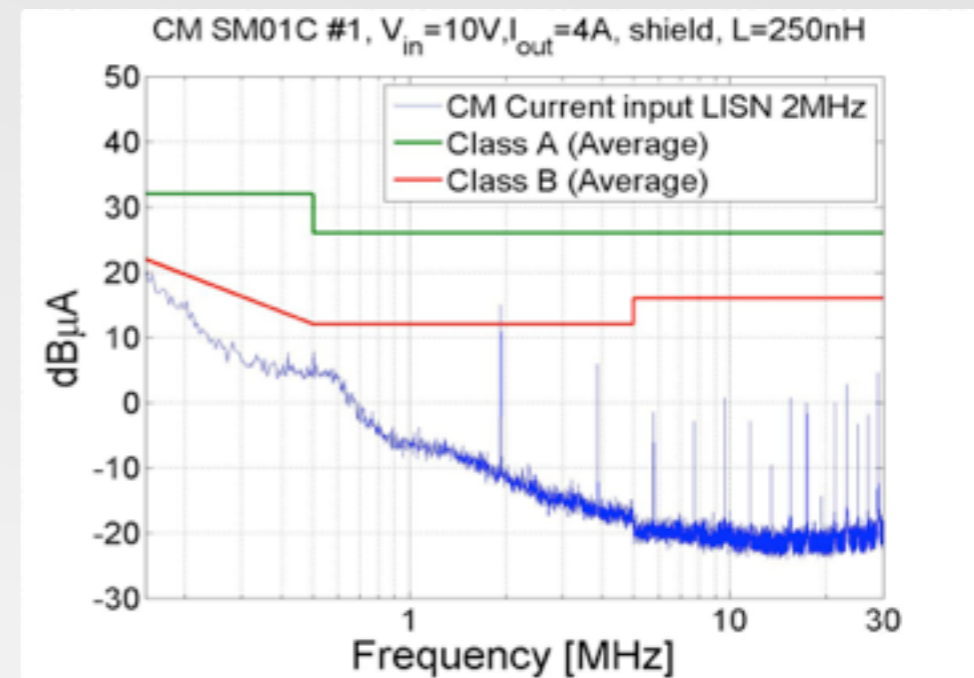
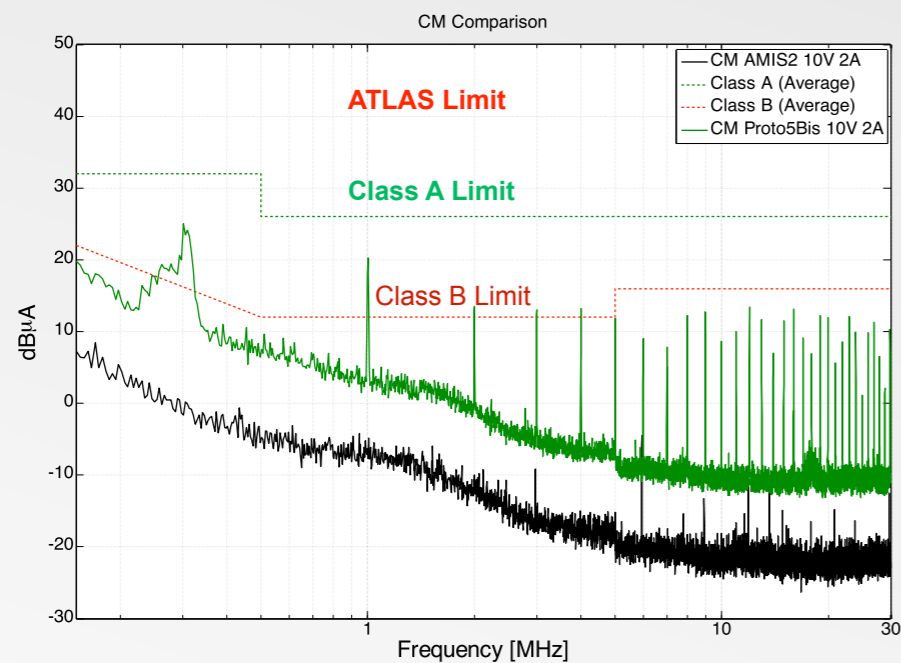
Full converter boards

- Using the AMIS2 ASIC



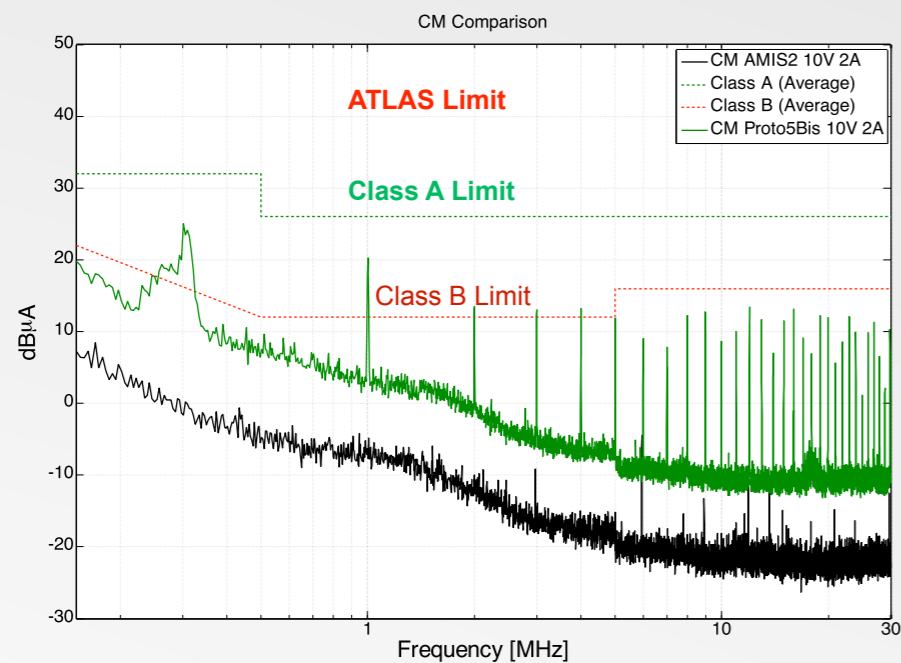
Full converter boards

- Using the AMIS2 ASIC
 - ❖ Optimization principles fully applied

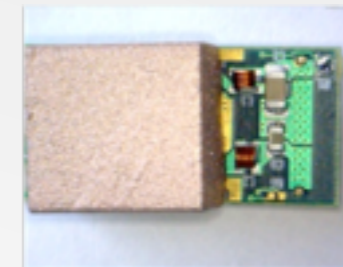
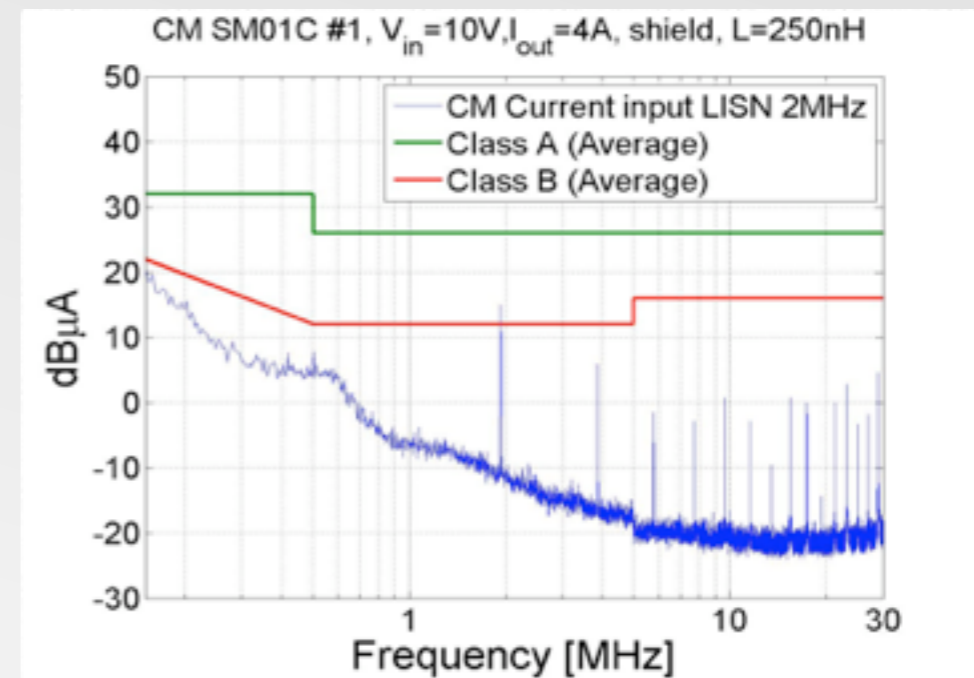


Full converter boards

- Using the AMIS2 ASIC
 - ❖ Optimization principles fully applied
 - ❖ Very compact design, need only for few external components

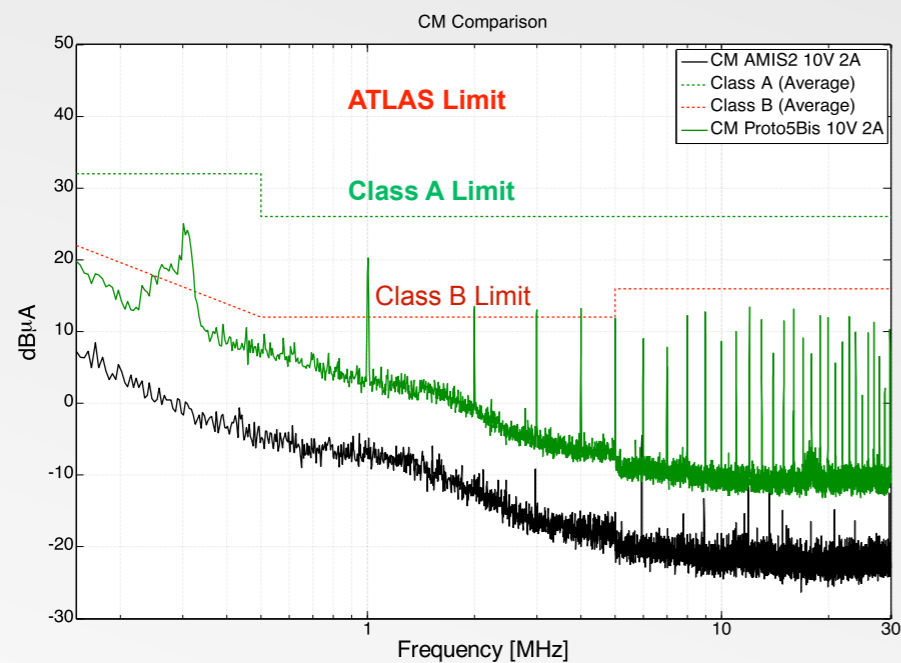


- Using a commercial DCDC circuit (LTC3605) - SM01C

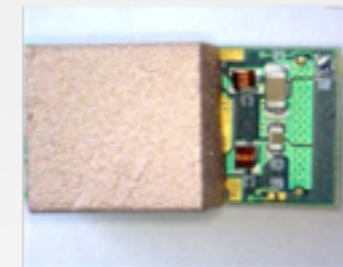
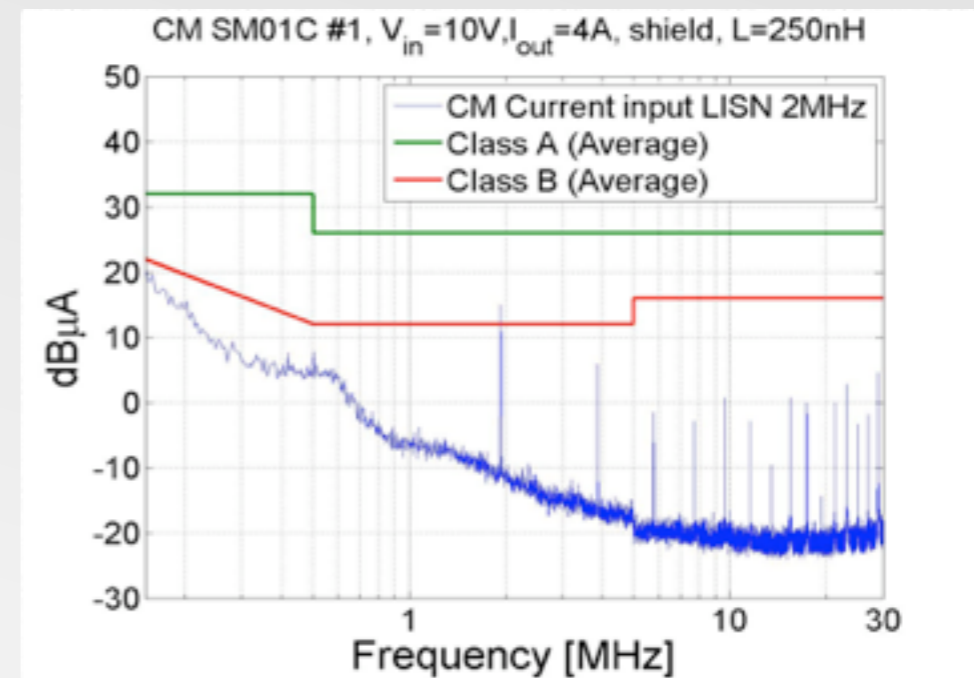


Full converter boards

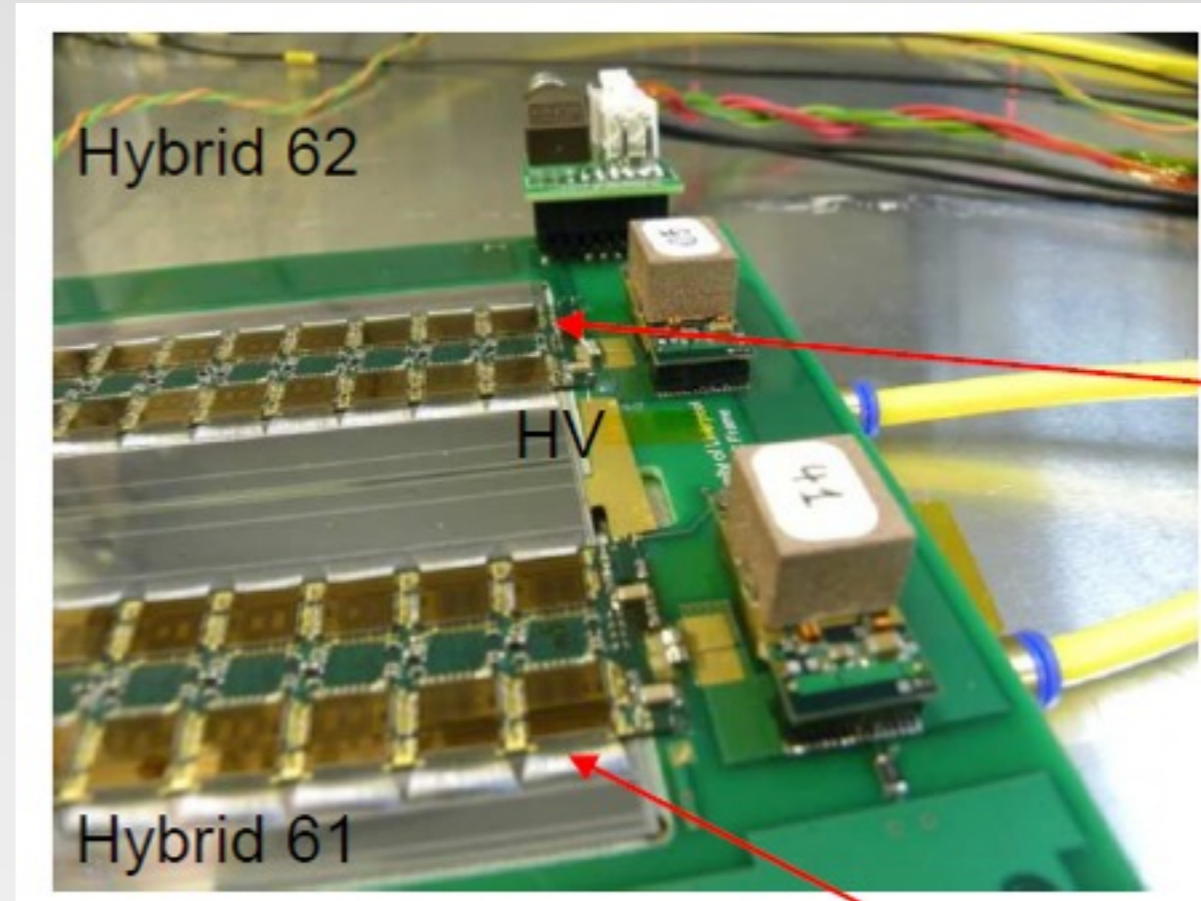
- Using the AMIS2 ASIC
 - ❖ Optimization principles fully applied
 - ❖ Very compact design, need only for few external components



- Using a commercial DCDC circuit (LTC3605) - SM01C
 - ❖ Designed to provide up to 5A to match requirements of ATLAS SCT prototype modules

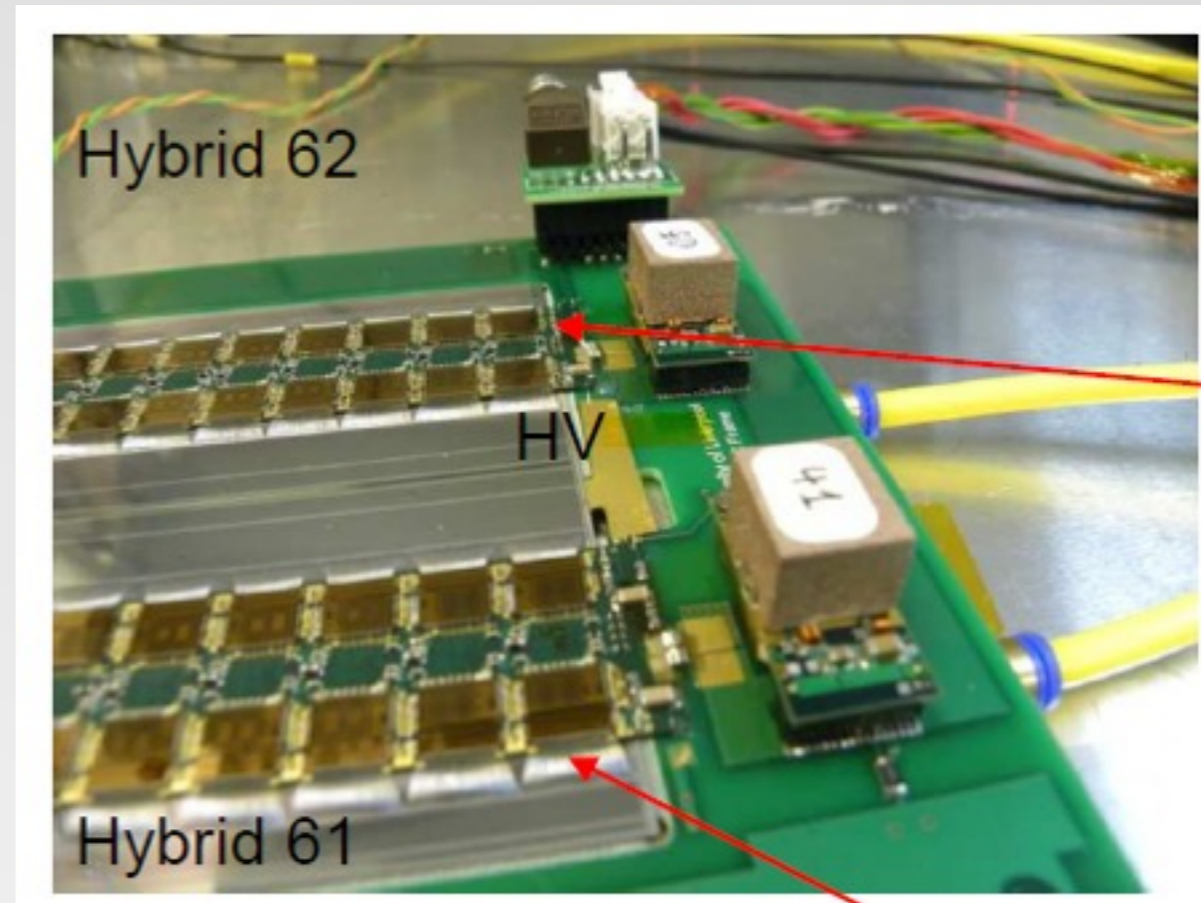


Measurements with ATLAS SCT prototype modules



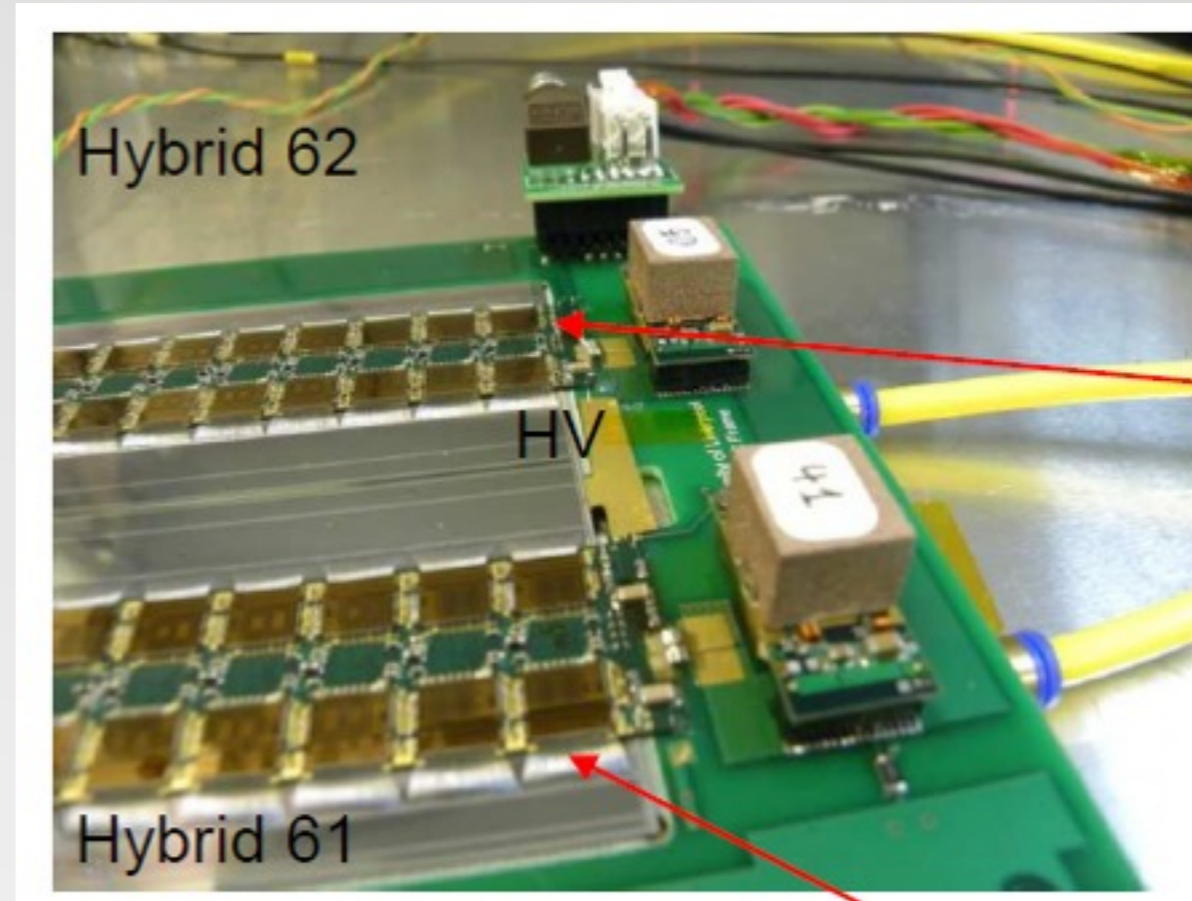
Measurements with ATLAS SCT prototype modules

- A stave module was powered with two SM01C converters and its performance was compared with the one obtained using a linear power supply (test done at Liverpool, then at CERN with UniGe module)



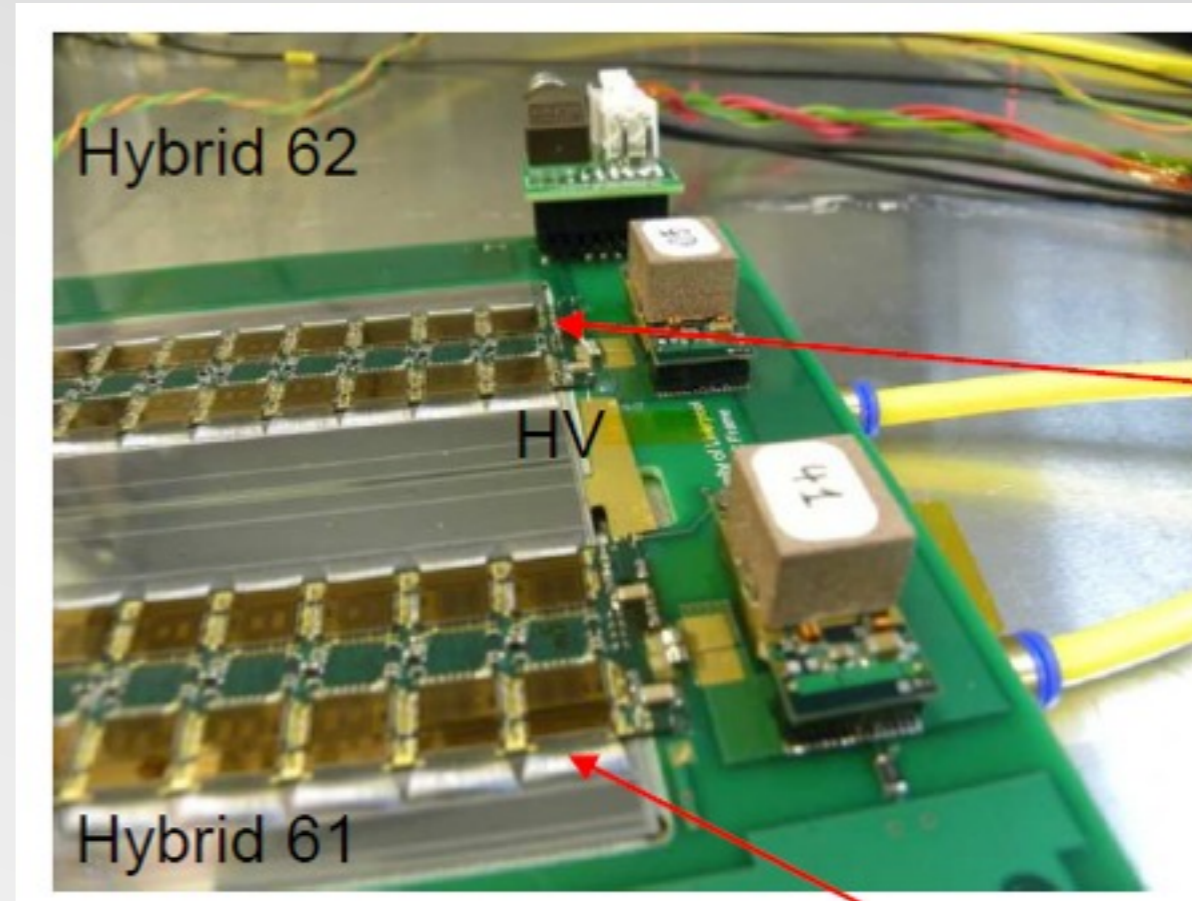
Measurements with ATLAS SCT prototype modules

- A stave module was powered with two SM01C converters and its performance was compared with the one obtained using a linear power supply (test done at Liverpool, then at CERN with UniGe module)
- A residual magnetic field emitted from the DCDC board fitted with plastic coated shield raises the noise of the front-end



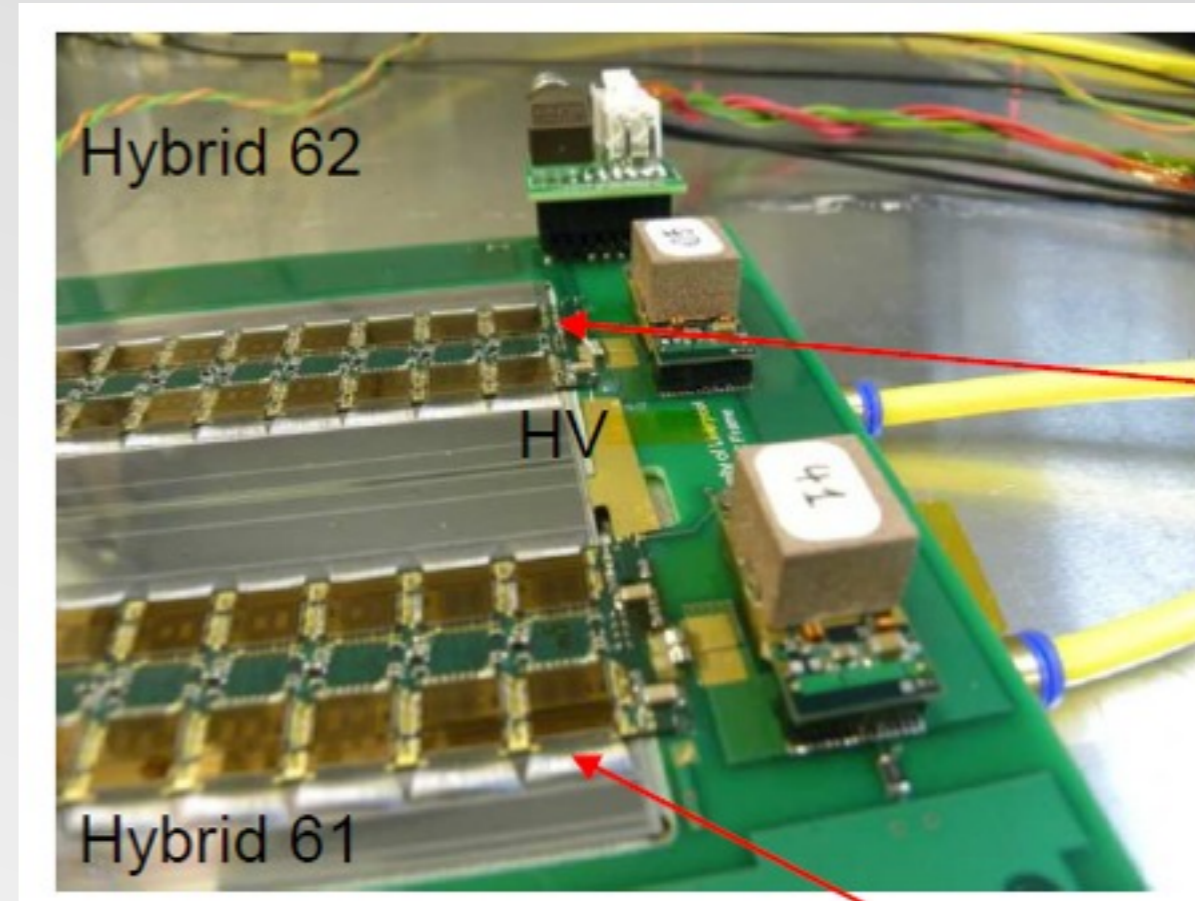
Measurements with ATLAS SCT prototype modules

- A stave module was powered with two SM01C converters and its performance was compared with the one obtained using a linear power supply (test done at Liverpool, then at CERN with UniGe module)
- A residual magnetic field emitted from the DCDC board fitted with plastic coated shield raises the noise of the front-end
- When using a copper foil shield instead, the reference noise levels are recovered



Measurements with ATLAS SCT prototype modules

- A stave module was powered with two SM01C converters and its performance was compared with the one obtained using a linear power supply (test done at Liverpool, then at CERN with UniGe module)
- A residual magnetic field emitted from the DCDC board fitted with plastic coated shield raises the noise of the front-end
- When using a copper foil shield instead, the reference noise levels are recovered
- The compatibility between SM01C and the ATLAS stave modules is now achieved, using copper foil shields



Shielding EM fields

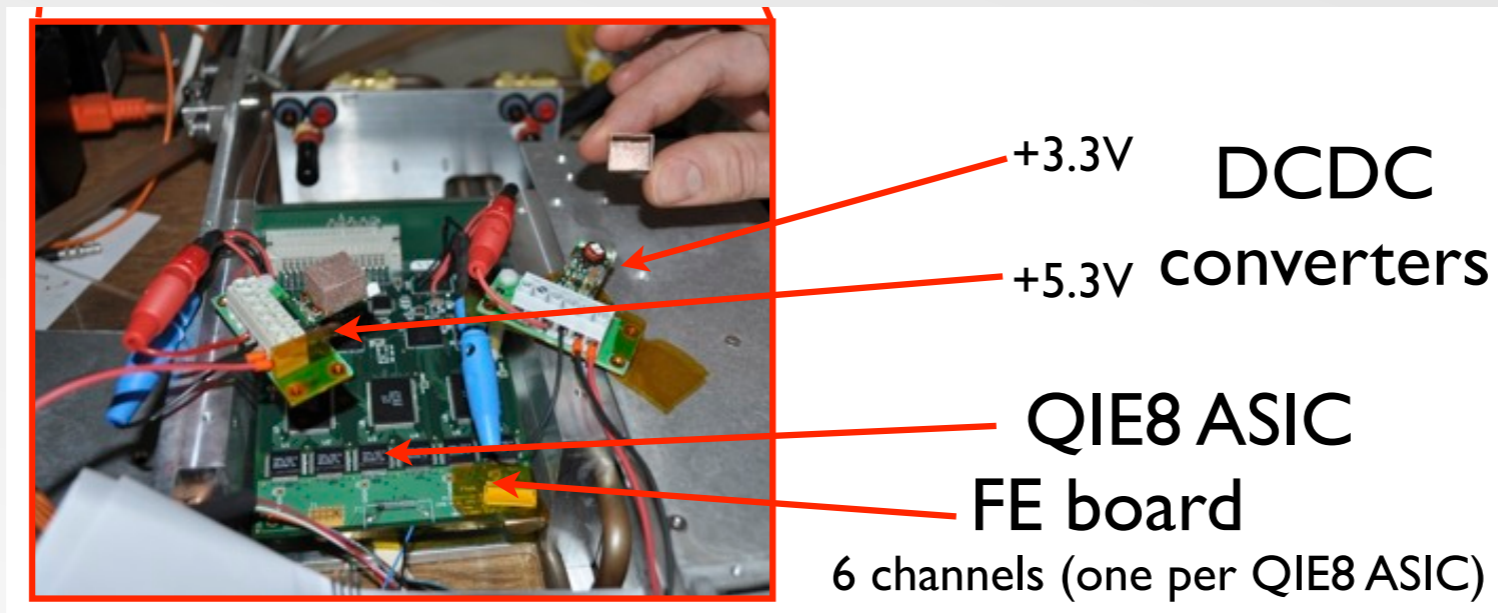
Shielding EM fields

- Measurements with ATLAS SCT modules evidence the need for optimizing the shield

Shielding EM fields

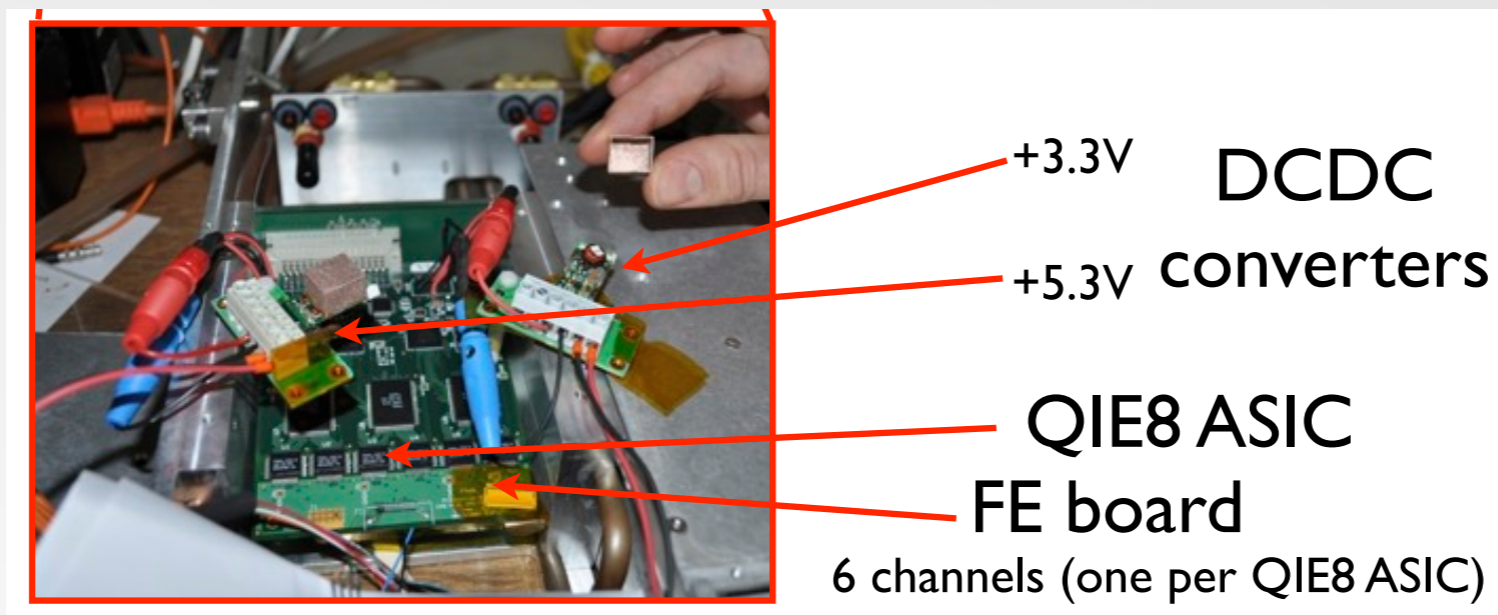
- Measurements with ATLAS SCT modules evidence the need for optimizing the shield
- 2 approaches have been followed to prototype manufacturable shields, both based on a coated plastic support. Metal (Cu) is either painted as a Cu-loaded varnish, or deposited (on-going work)
 - ❖ A dedicated test board has been developed to measure the effectiveness of all shields and define the optimum material and thickness
 - ❖ A simulation study will be performed and results compared to experimental benchmarks

Interest in using our DCDC converters



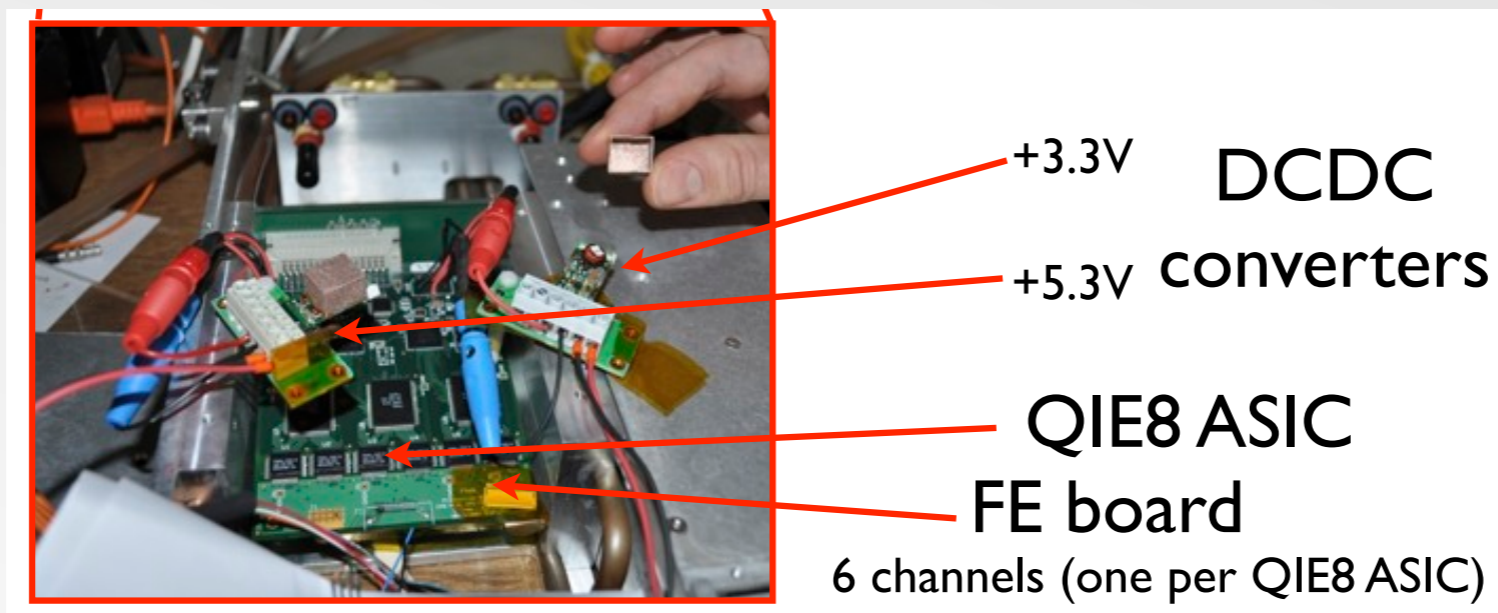
Interest in using our DCDC converters

- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)



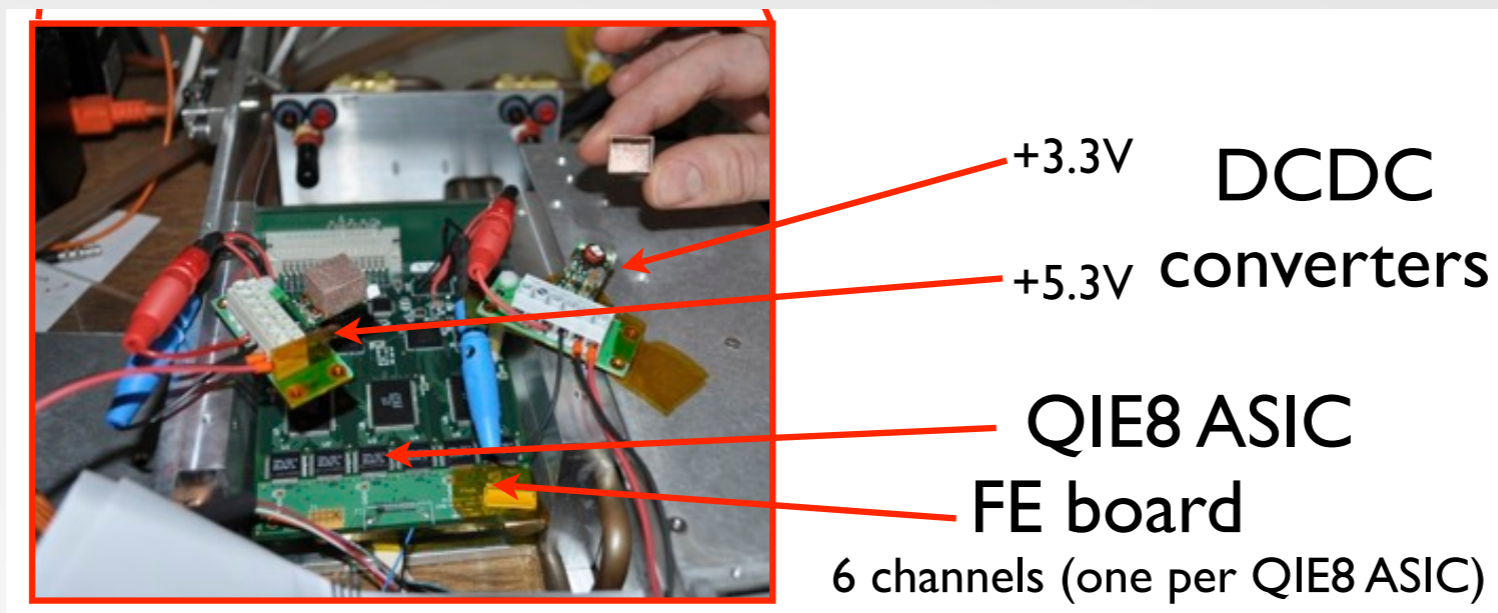
Interest in using our DCDC converters

- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)



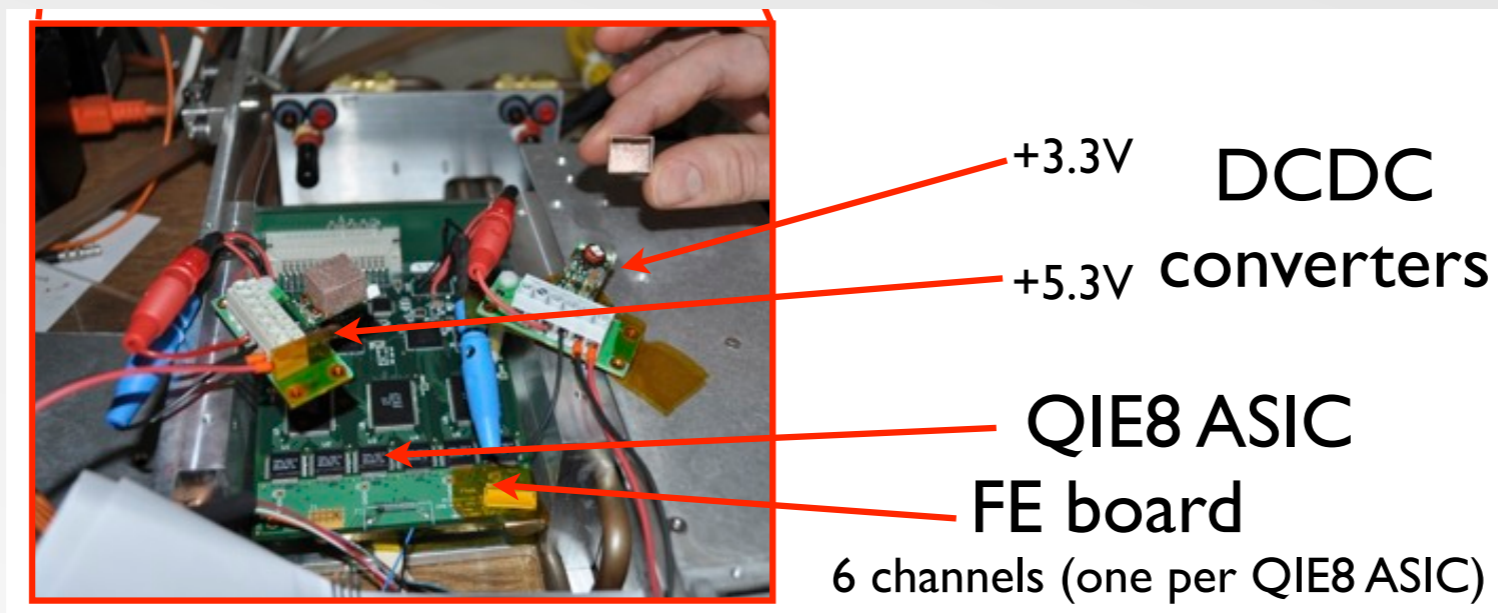
Interest in using our DCDC converters

- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)



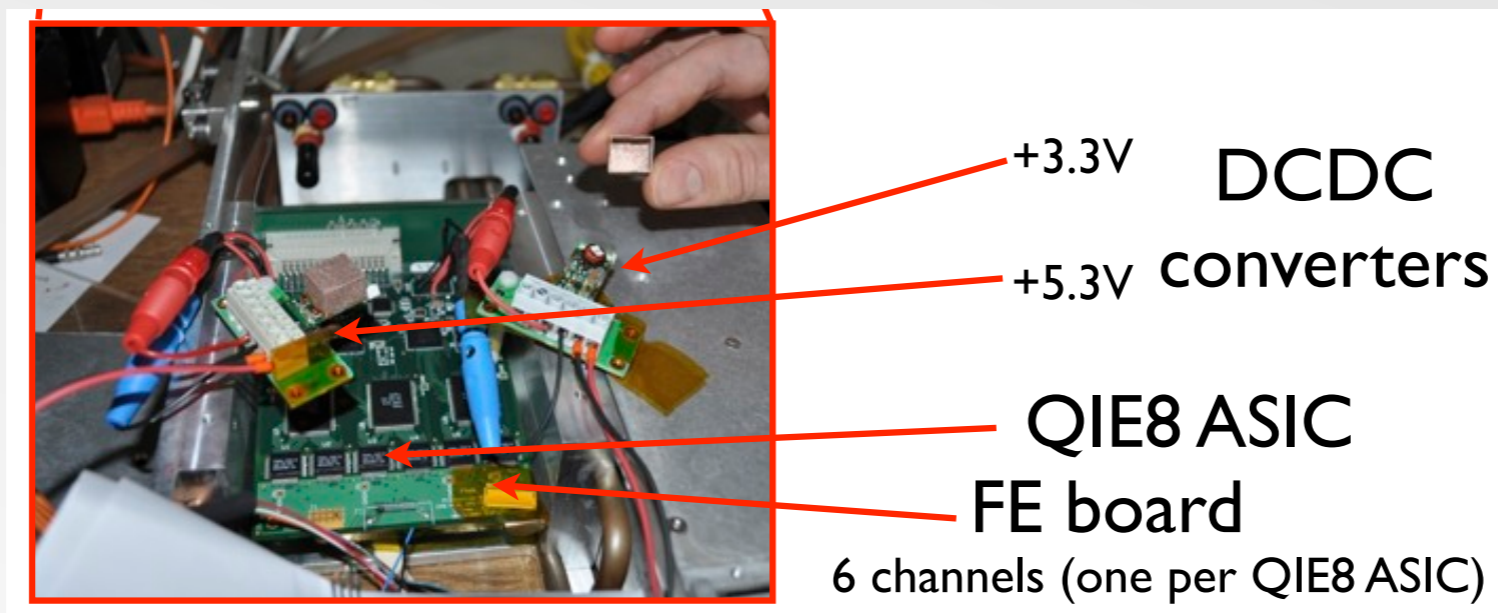
Interest in using our DCDC converters

- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)
- Phase1 upgrade of CMS HCAL (Fermilab, Maryland, Minnesota,). Preliminary system-level measurement done on FEE board by C.Fuentes and T.Grassi with very good results



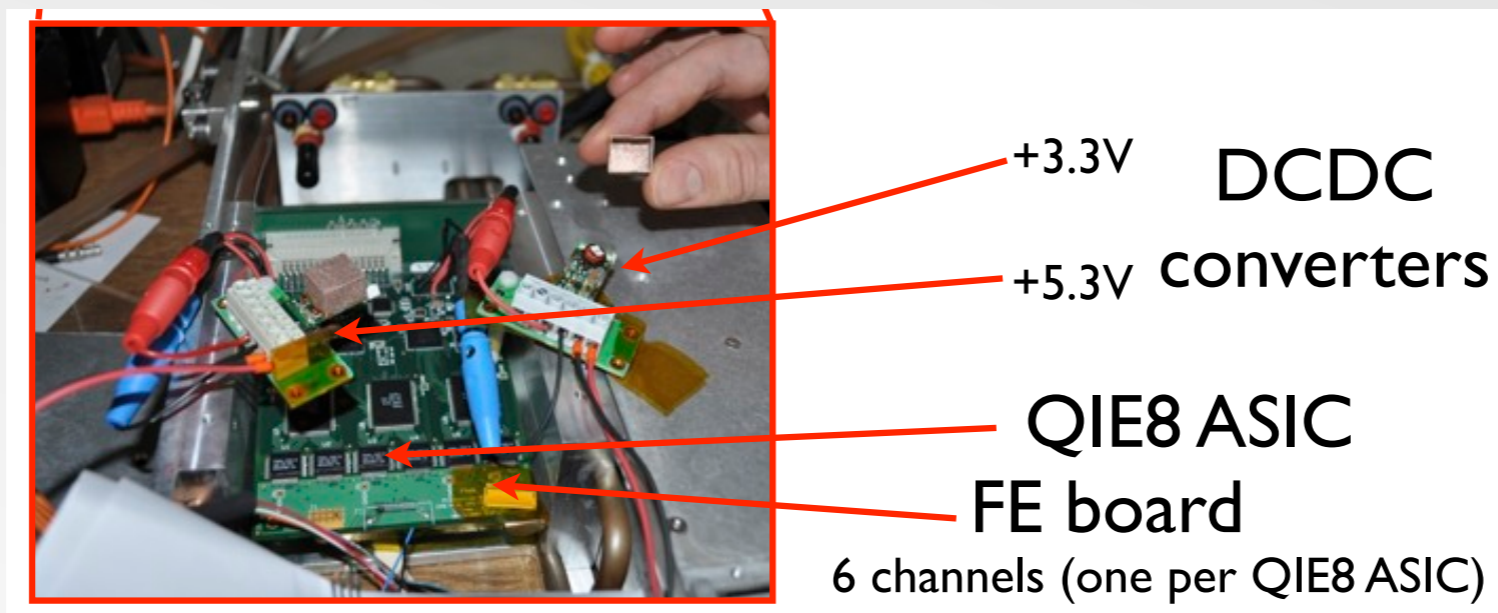
Interest in using our DCDC converters

- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)
- Phase1 upgrade of CMS HCAL (Fermilab, Maryland, Minnesota,). Preliminary system-level measurement done on FEE board by C.Fuentes and T.Grassi with very good results



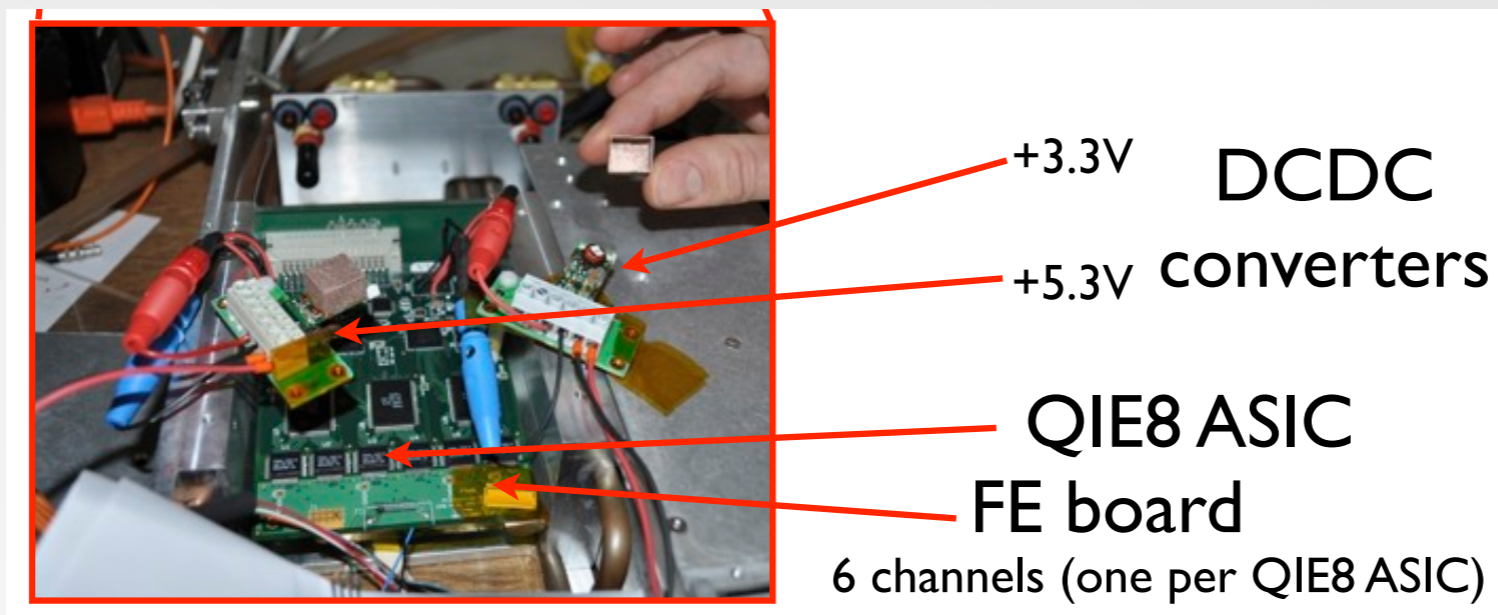
Interest in using our DCDC converters

- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)
- Phase1 upgrade of CMS HCAL (Fermilab, Maryland, Minnesota,). Preliminary system-level measurement done on FEE board by C.Fuentes and T.Grassi with very good results



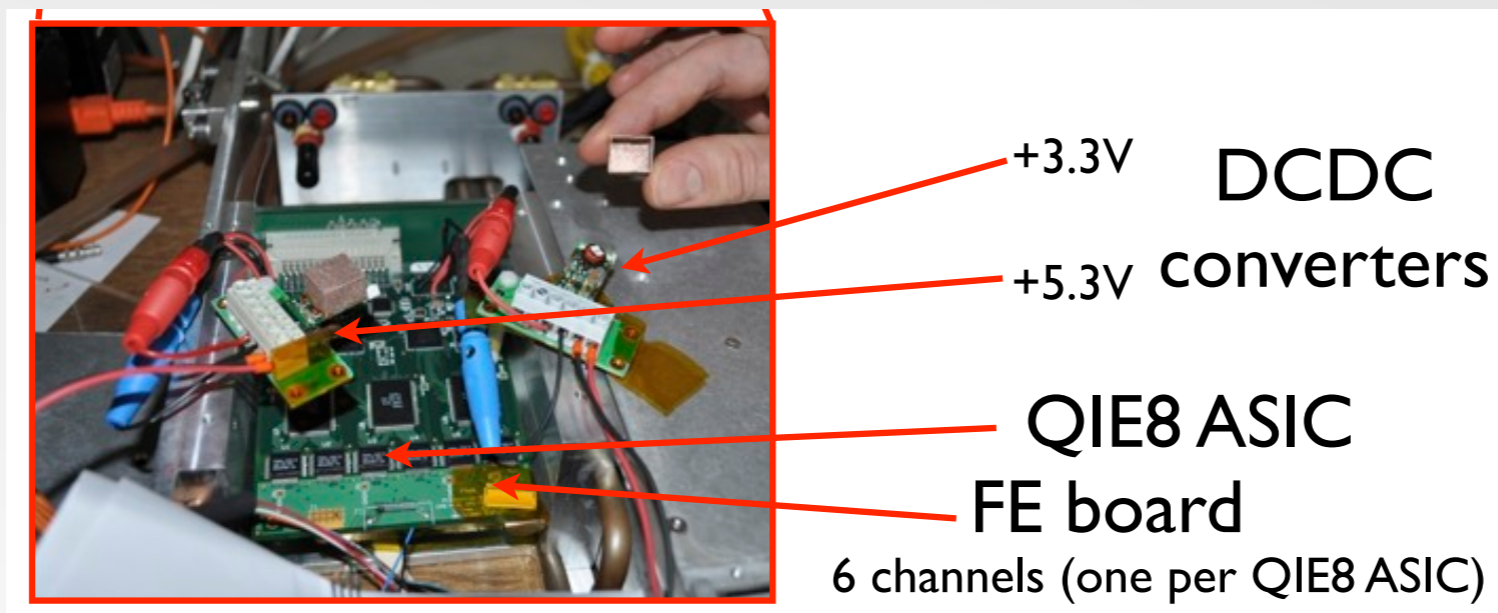
Interest in using our DCDC converters

- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)
- Phase1 upgrade of CMS HCAL (Fermilab, Maryland, Minnesota,). Preliminary system-level measurement done on FEE board by C.Fuentes and T.Grassi with very good results



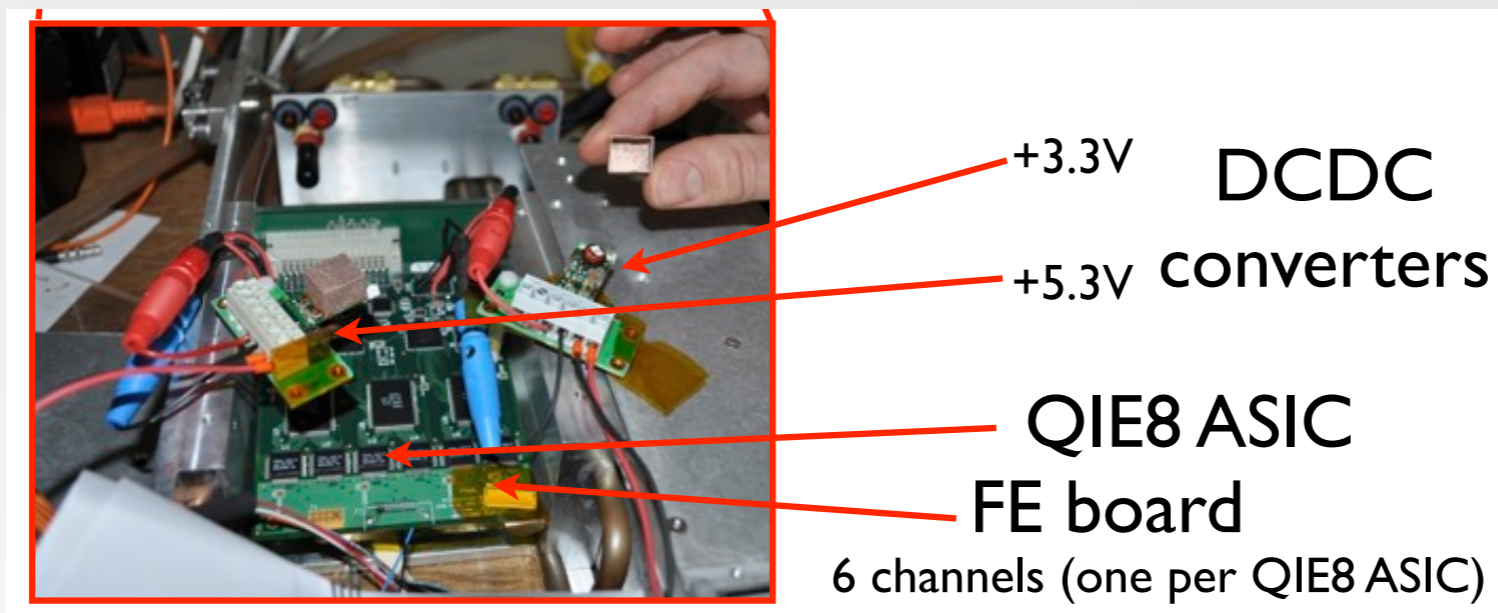
Interest in using our DCDC converters

- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)
- Phase1 upgrade of CMS HCAL (Fermilab, Maryland, Minnesota,). Preliminary system-level measurement done on FEE board by C.Fuentes and T.Grassi with very good results



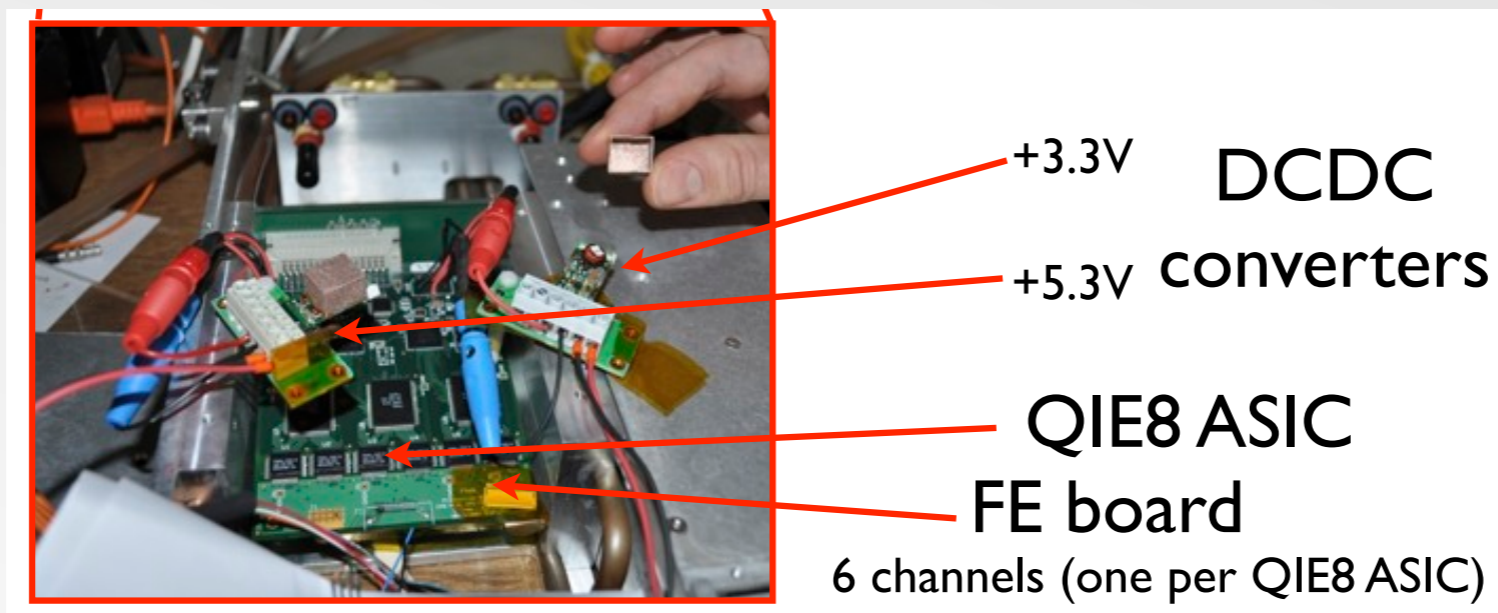
Interest in using our DCDC converters

- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)
- Phase1 upgrade of CMS HCAL (Fermilab, Maryland, Minnesota,). Preliminary system-level measurement done on FEE board by C.Fuentes and T.Grassi with very good results



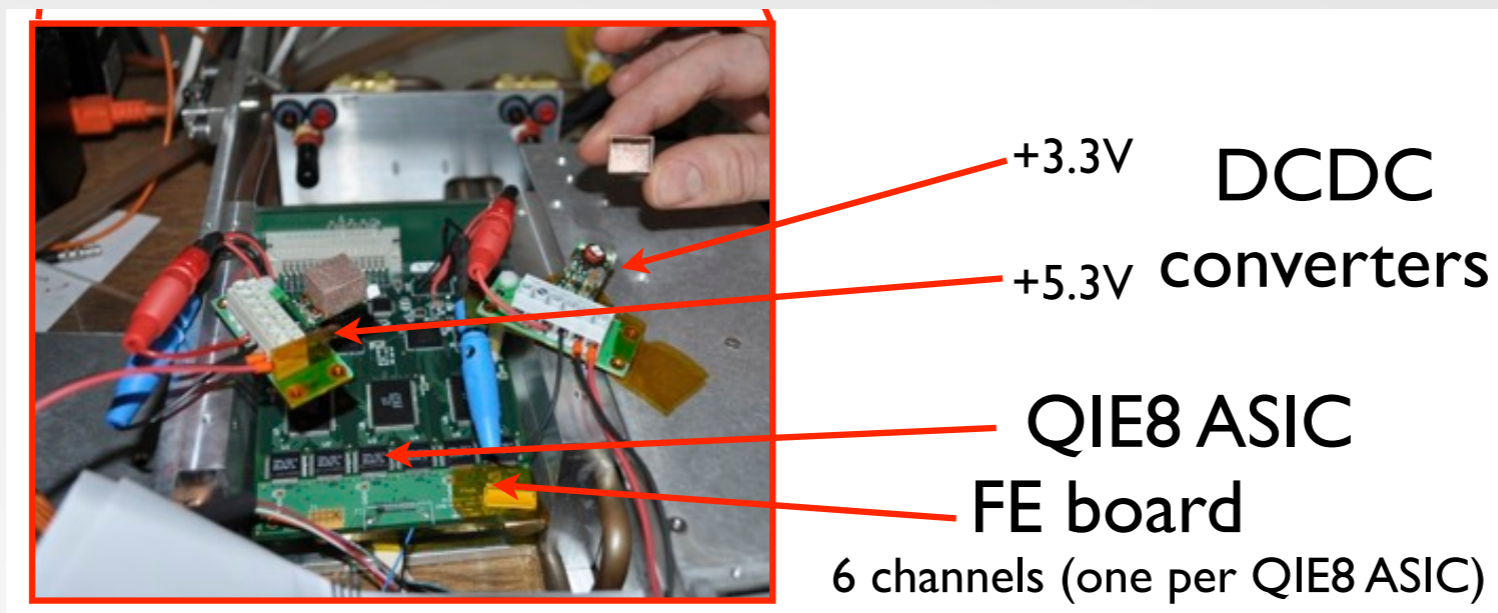
Interest in using our DCDC converters

- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)
- Phase1 upgrade of CMS HCAL (Fermilab, Maryland, Minnesota,). Preliminary system-level measurement done on FEE board by C.Fuentes and T.Grassi with very good results



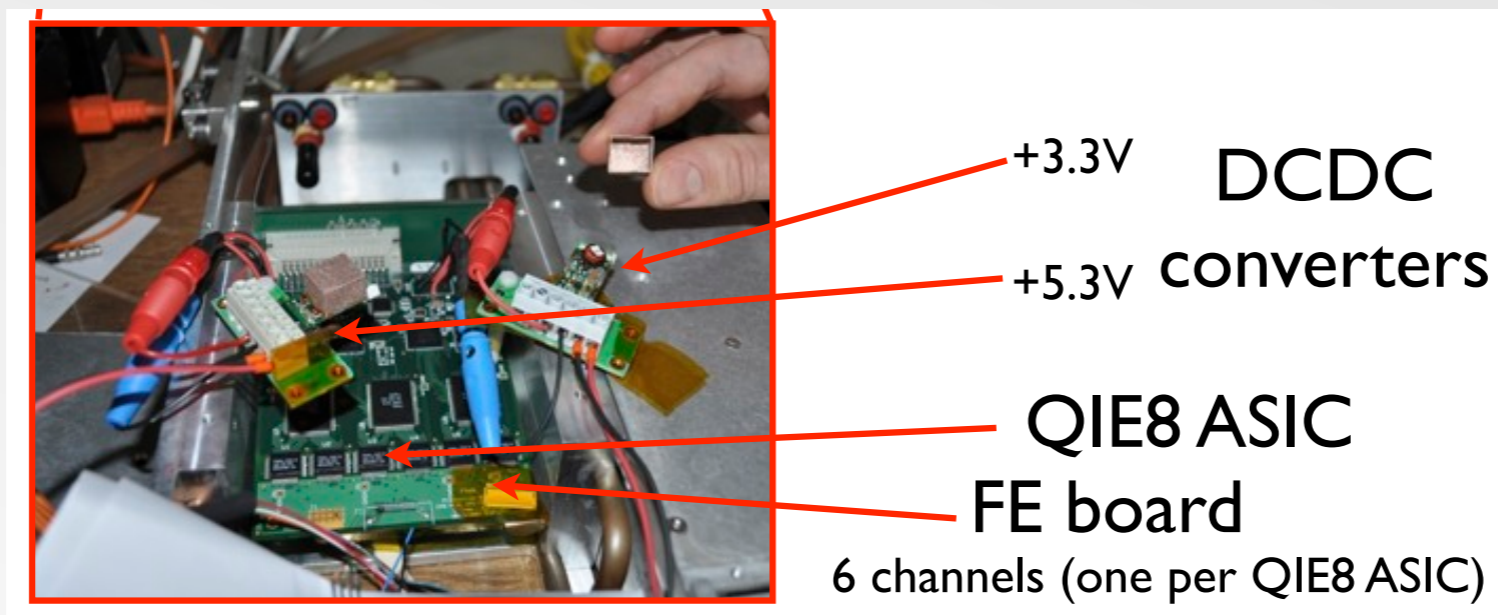
Interest in using our DCDC converters

- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)
- Phase1 upgrade of CMS HCAL (Fermilab, Maryland, Minnesota,). Preliminary system-level measurement done on FEE board by C.Fuentes and T.Grassi with very good results



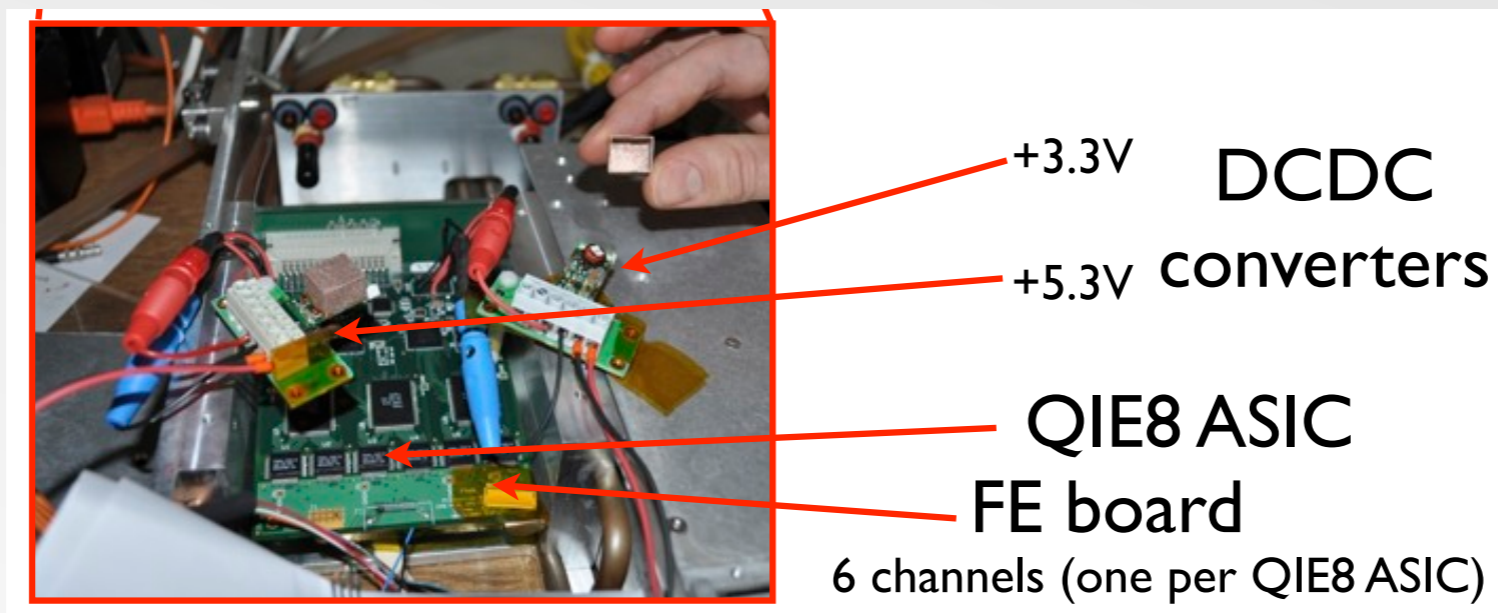
Interest in using our DCDC converters

- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)
- Phase1 upgrade of CMS HCAL (Fermilab, Maryland, Minnesota,). Preliminary system-level measurement done on FEE board by C.Fuentes and T.Grassi with very good results



Interest in using our DCDC converters

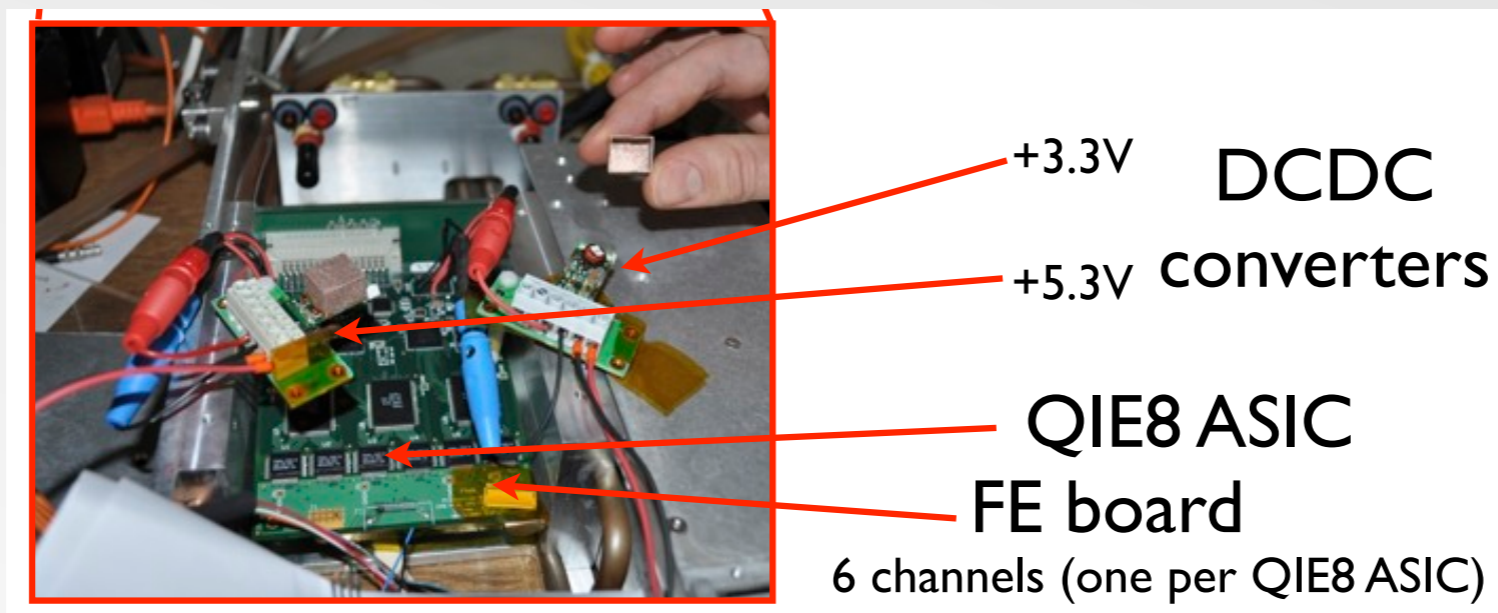
- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)
- Phase1 upgrade of CMS HCAL (Fermilab, Maryland, Minnesota,). Preliminary system-level measurement done on FEE board by C.Fuentes and T.Grassi with very good results



- Phase2 upgrade of ATLAS endcap tracker (Barcelona, P.Bernabeu)

Interest in using our DCDC converters

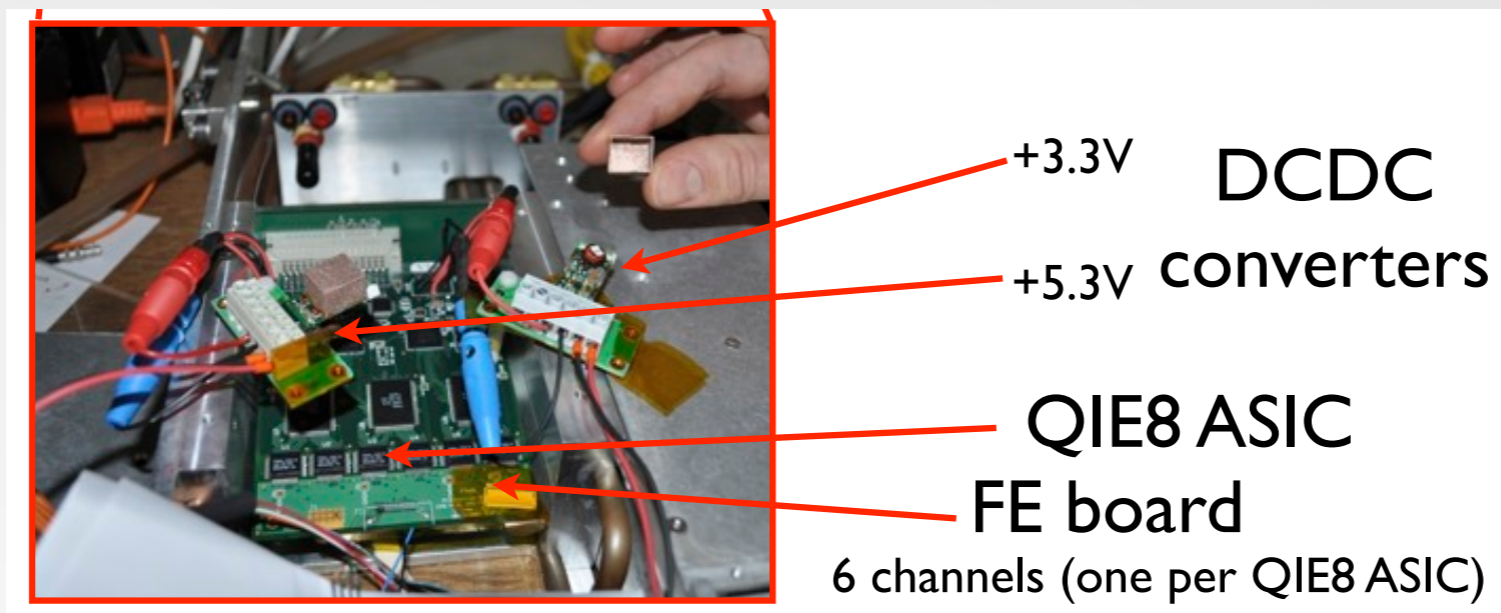
- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)
- Phase1 upgrade of CMS HCAL (Fermilab, Maryland, Minnesota,). Preliminary system-level measurement done on FEE board by C.Fuentes and T.Grassi with very good results



- Phase2 upgrade of ATLAS endcap tracker (Barcelona, P.Bernabeu)
- Phase2 upgrade of ATLAS TileCal (Argonne NatLab, Chicago, G.Drake)

Interest in using our DCDC converters

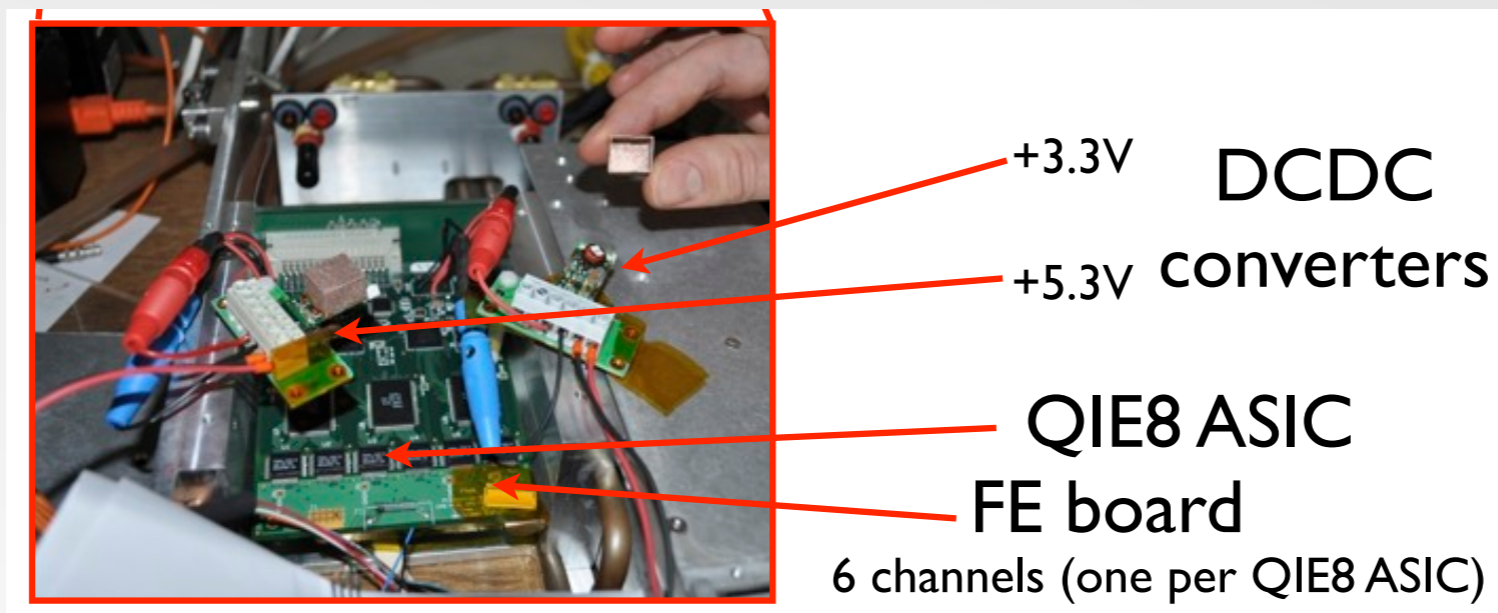
- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)
- Phase1 upgrade of CMS HCAL (Fermilab, Maryland, Minnesota,). Preliminary system-level measurement done on FEE board by C.Fuentes and T.Grassi with very good results



- Phase2 upgrade of ATLAS endcap tracker (Barcelona, P.Bernabeu)
- Phase2 upgrade of ATLAS TileCal (Argonne NatLab, Chicago, G.Drake)
- Phase1/2 upgrade of ATLAS LAr calorimeter (BNL, J.Kierstead)

Interest in using our DCDC converters

- Phase1 upgrade of CMS pixels (RWTH Aachen, PSI, Fermilab, ...)
- Phase2 upgrade of CMS tracker (no prototype module available yet)
- Phase2 upgrade of ATLAS barrel tracker (both supermodule and stave concepts. Contacts and work mainly with Liverpool and UniGe)
- Phase1 upgrade of CMS HCAL (Fermilab, Maryland, Minnesota,). Preliminary system-level measurement done on FEE board by C.Fuentes and T.Grassi with very good results



- Phase2 upgrade of ATLAS endcap tracker (Barcelona, P.Bernabeu)
- Phase2 upgrade of ATLAS TileCal (Argonne NatLab, Chicago, G.Drake)
- Phase1/2 upgrade of ATLAS LAr calorimeter (BNL, J.Kierstead)
- Phase2 upgrade of LHCb calorimeter (Barcelona, D.Gascon)

Summary

- ASIC
 - ❖ Technology
 - * On-semi 0.35um technology fully validated. This is baseline for Phase1 developments
 - * IHP 0.25um technology still under evaluation, in collaboration with IHP. SEB test in April should tell if this technology is quickly usable for our development
 - ❖ Design
 - * 2 prototypes in production in On-Semi 0.35um. AMIS4 contains full protection features and is very close to a final design (to be confirmed by measurements...)
- Full converter boards
 - ❖ Low-noise board design
 - * Know-how acquired and confirmed by results
 - * Low-noise and compact prototypes available for both ASIC and commercial DCDC
 - ❖ Special components
 - * Inductor design chosen, transferred to industry and in production
 - * Shield requirements being studied, and prototypes produced
 - ❖ Integration in detector systems
 - * Measurements on different systems confirm that power can be provided by DCDC converters without impacting the noise performance