



## A Super-TFC for a Super-LHCb (II)

1. S-TFC on xTCA – Mapping TFC on Marseille hardware
  2. ECS+TFC relay in FE Interface
  3. Protocol and commands for FE/BE control (Discussion topic)
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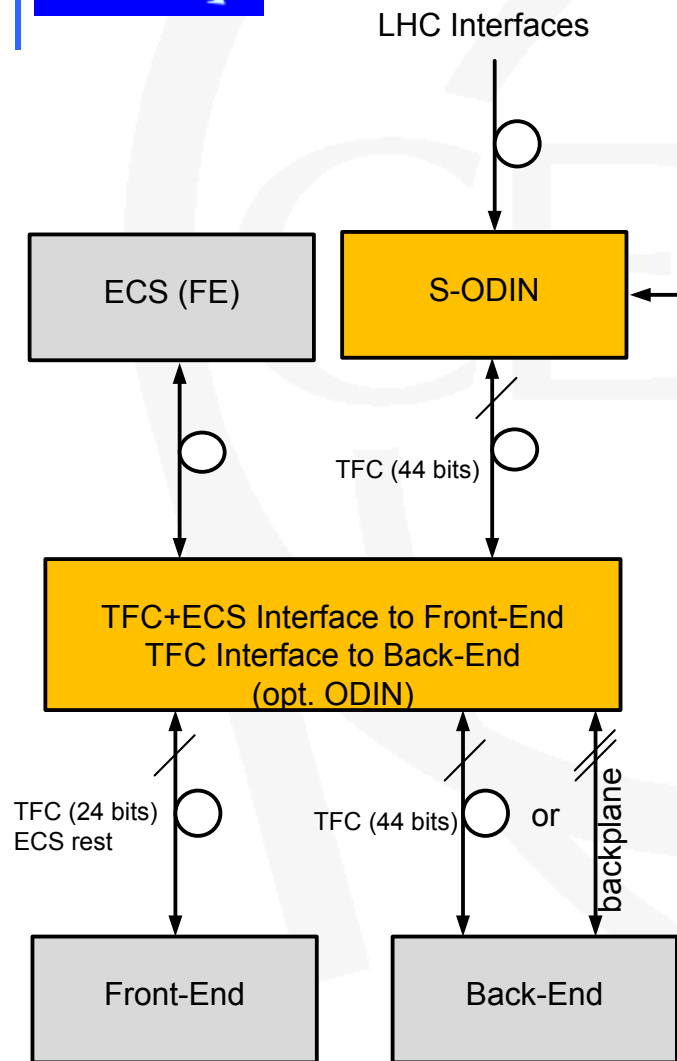
Jean-Pierre Cachemiche

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# What do we need?

Simplest strip-down view as starting-point:



## Conclusion:

### 1. Single General Purpose board

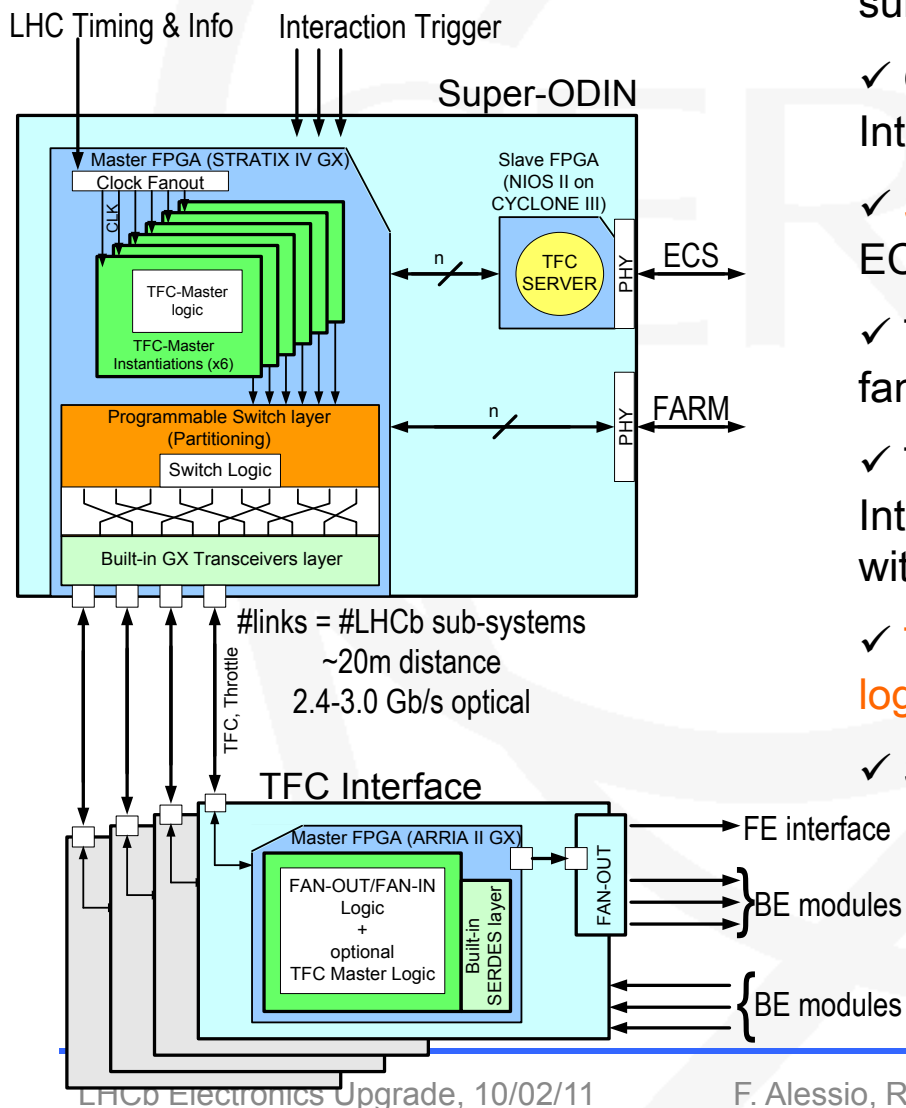
- ✓ ECS interface, local intelligence and com-fabric
- ✓ Fitted with several mezzanine slots
- ✓ The all-desired form-factor (BP "2b or !2b")

### 2. Mezzanines

- ✓ GBT mezzanine (standard)
- ✓ DAQ mezzanine (standard)
- ✓ Our *special* (clock, LHC interfaces, TTC, etc)



# S-TFC concept reminder



✓ S-ODIN has **separate instantiations** in FPGA per sub-detector. Like different ODINs.

✓ Only **one instantiation drives LHCb** and receives Interaction Triggers.

✓ **Switching** is done **in FPGA**. Programmable via ECS and only need enough outputs (24?).

✓ TFC Interface fans out TFC information to BE, fans in THROTTLE information from BE.

✓ TFC Interface splits TFC information to FE Interface. FE Interface relays TFC and merges it with ECS and sends it to FE. → **Could be merged**

✓ **TFC Interface can be loaded with single S-ODIN logic** to run sub-detector standalone or in lab

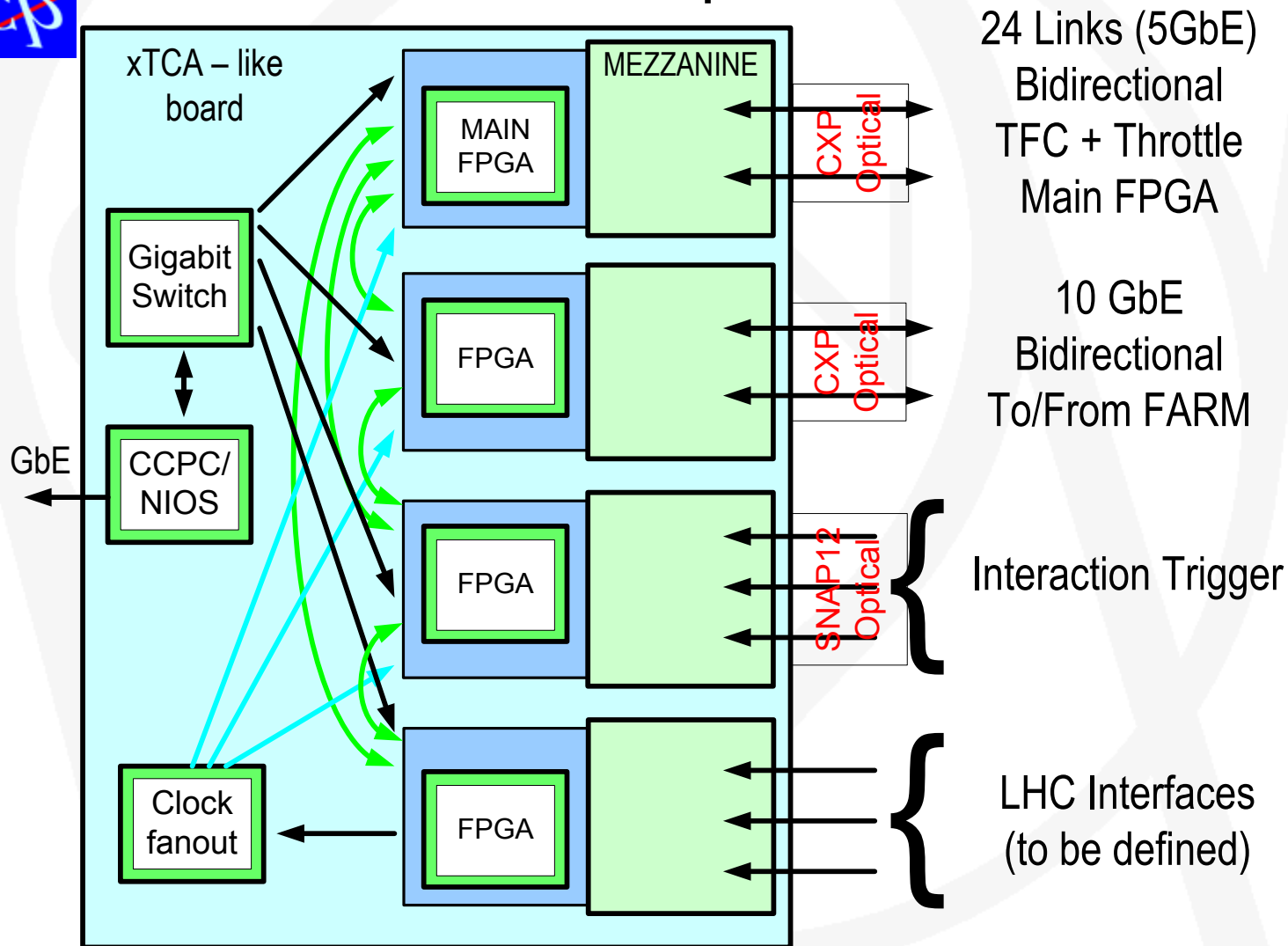
✓ Support for old TTC system

✓ **CCPC or NIOS?**

✓ **Fibres or backplane?**

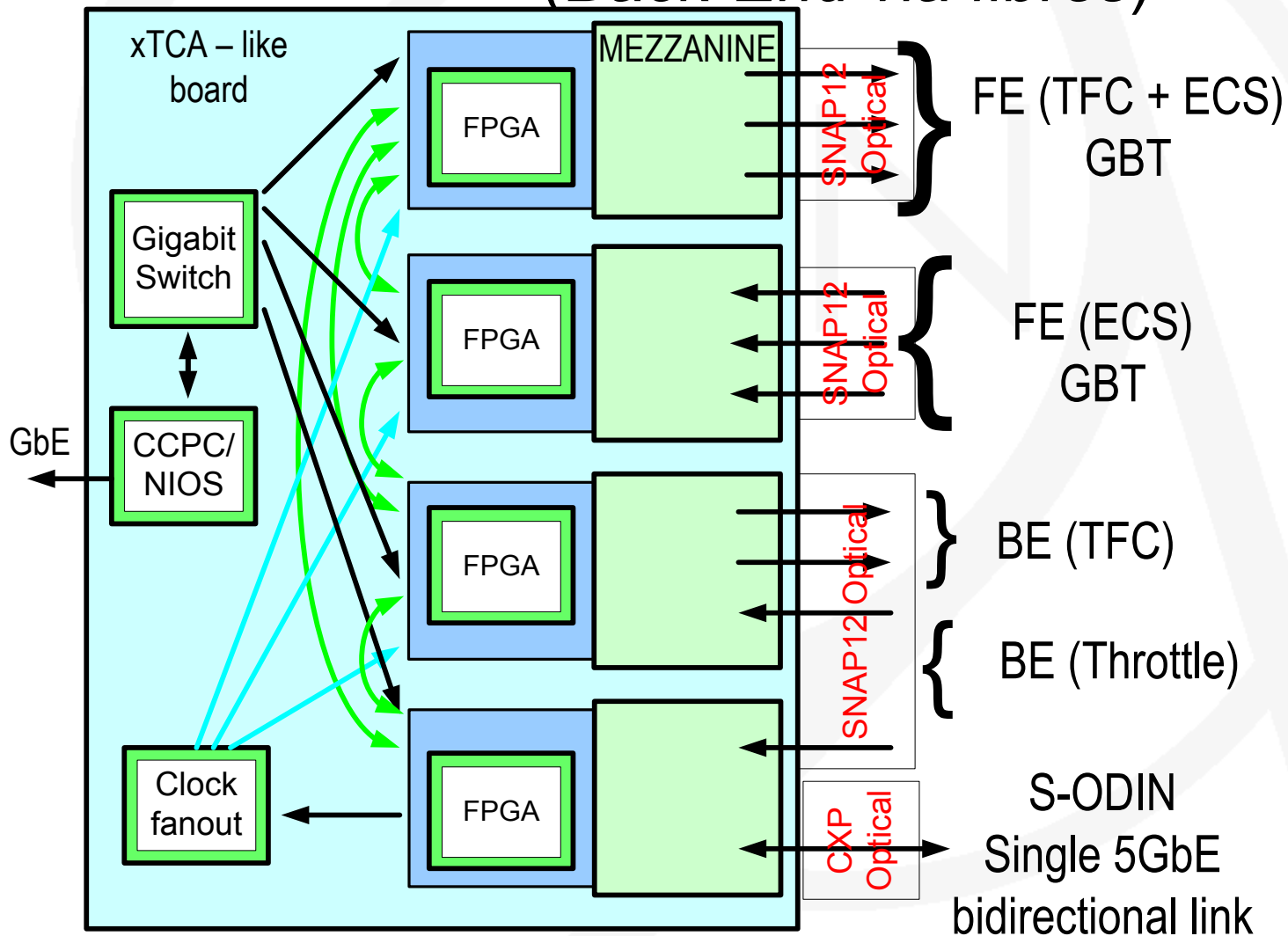
No absolute requirement from TFC specs, just preferences.

# S-ODIN Implementation

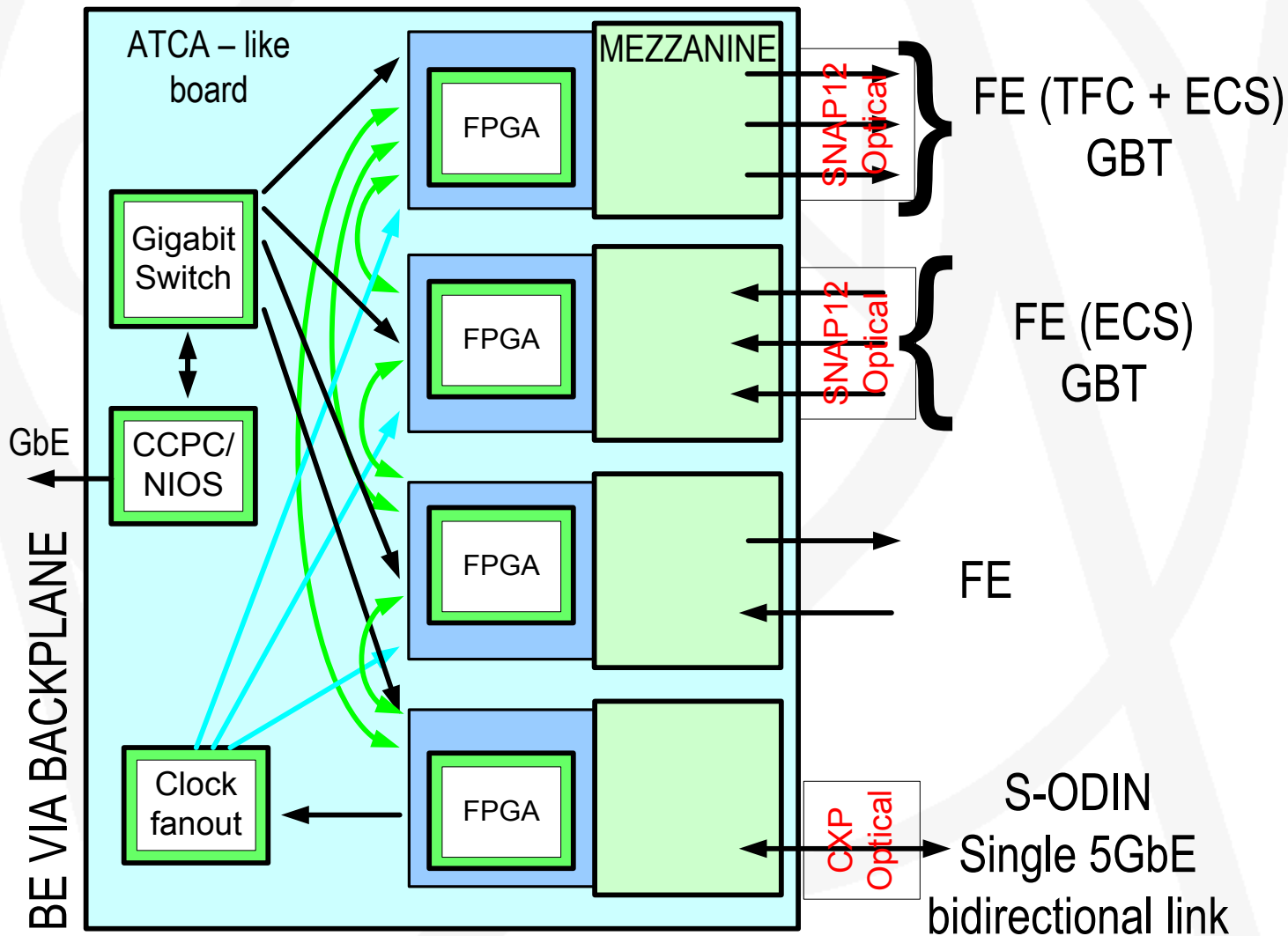


Fibre ribbon break-outs needed

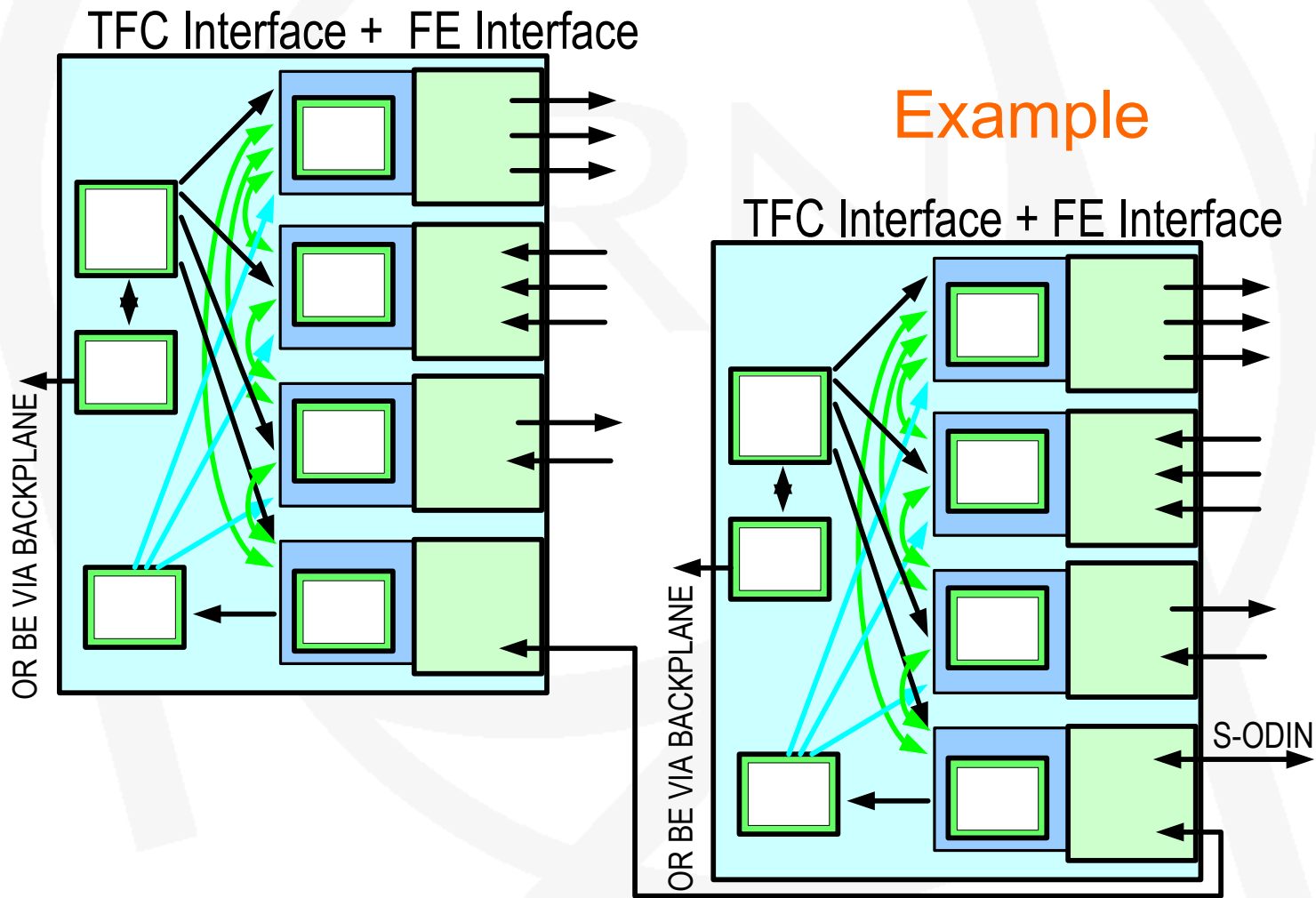
# TFC Interface **AND** FE Interface (*Back-End via fibres*)



# Alternative TFC Interface AND FE Interface (BE via backplane)



# Cascading option, if needed





# TFC fits well on xTCA and Marseille hardware

TFC development work at CERN apart from hardware testing and high level control

- ✓ All FPGA code (TFC logic including trigger, link protocols, board control)
- ✓ Special mezzanine(s) (Clock reception, LHC Interfaces, TTC, etc)
- ✓ Relay logic for TFC+FE Interface including optional ODIN logic for stand-alone activities

## Challenges:

- ✓ TFC+FE interfaces with optional ODIN need to be ready and produced in quantities before any SD test setup! → Strain on Marseille
  - ✓ Validation of clock phase control and reproducibility of latency, jitter

## Considerations

In ATCA Dual Star technology, boards in Hub1 and Hub2 talks to all the boards in the crate

→ TFC Interface as Hub1 board

S-ODIN located near the LHC interfaces (clock, machine timing and control information).

→ bidirectional fibres connections to TFC Interface

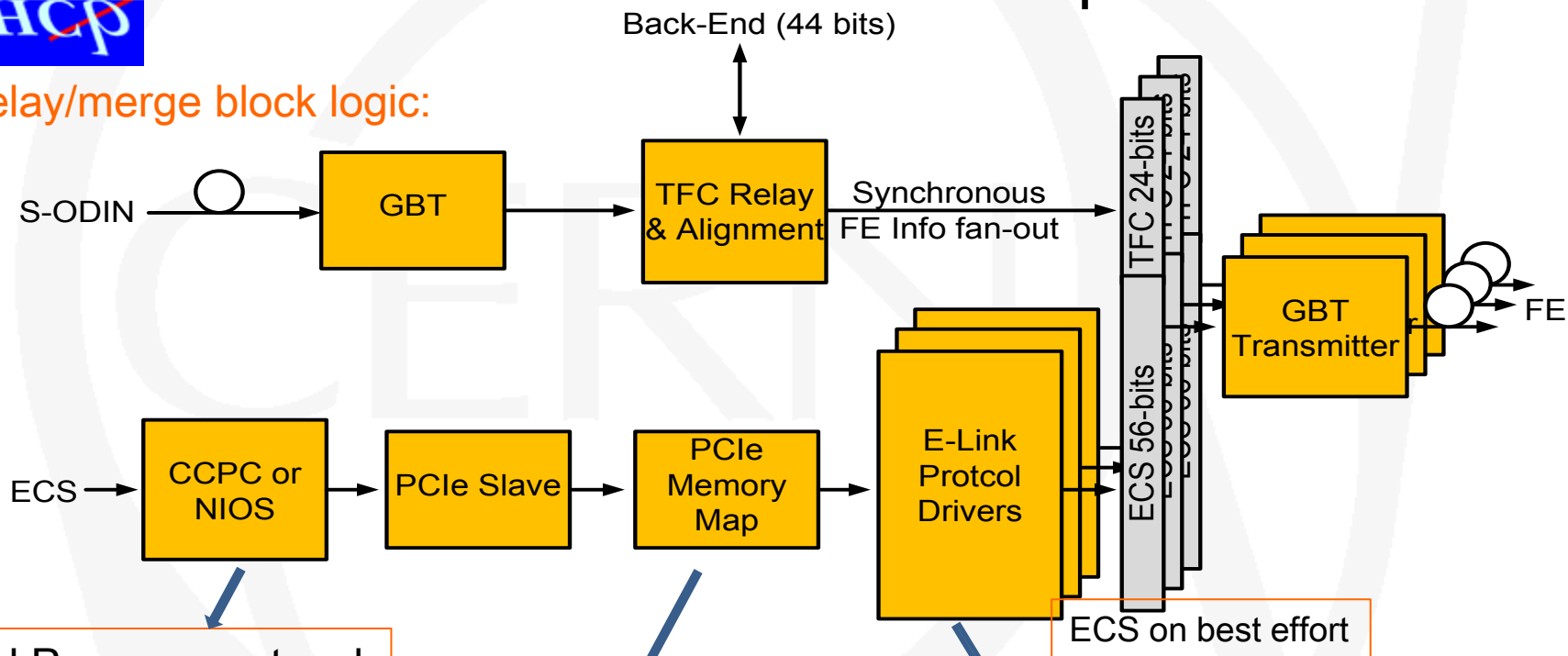
If no backplane, BE connection via TFC Interface must be done via fibres

→ how many receivers/transmitter per mezzanine/ how many mezzanines?



# TFC+FE Interface Proposal

Relay/merge block logic:



General Purpose protocol through DIM server “a la TFC” on Ethernet(→PCIe)

‘Memory Map’ with internal address scheme for GBT addressing, E-link addressing and bus type

‘Protocol drivers’ build GBT-SCA packets with addressing scheme and bus type for SCA user busses:

- I2C, JTAG, Single-wire, parallel-port, JTAG, Memory, Temperature sensing, ADC
- *Can it be defined what we will use?*



# TFC Front-End control command proposal

## ✓ Control functions for Front-End

- Bunch ID for synchronization check with internal counter
- Bunch Counter Reset
- Event Counter Reset
  - Reset of counter for accepted crossings = crossings for which header+data was sent
  - Reset of counter of truncated events
  - And all other event related counters (TFC command counters, etc!)
- Header Only → Force FE to transmit only header and no data
- Calibration pulsing (How many types do we need?)
- Non-zero suppressed readout of current crossing
  - Following  $n$  crossing will receive “Header Only” → Header only transmission
- Bunch Crossing Type Veto based on crossing scheme from LHC
  - Send header only for empty crossings and most single beam crossings
- Front-End electronics reset
  - During the time of the reset (common duration) Front-End receives “Header Only” command and should transmit header only
- Any other needs? → Reserve bits

✓ All TFC commands (individual signal) require local configurable delay



# Front-End TFC Word format

TFC Word to FE: 24 bits inside GBT frame @ 40 MHz = ~1 Gb/s

Encoding	23 .. 12	11 .. 9	8 .. 5	4	3	2	1	0
TFC Info	BID(11..0)	Reserve	Calib Type(3..0)	BX Veto	NZS	Header Only	FE reset	BID reset



# TFC Back-End control command proposal

## ✓ Control functions for Back-End

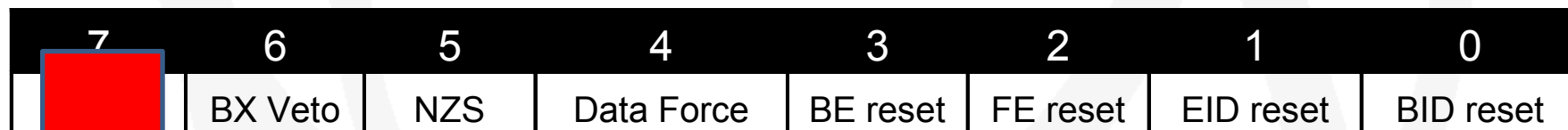
- Same as Front-End
  - Bunch ID for synchronization check with internal counter and data from FE
  - Bunch Counter Reset
  - Event Counter Reset (reset of same counters as FE + all event related counters)
  - Header Only → Force FE to transmit only header and no data (Informative)
  - Calibration pulsing (informative)
  - Non-zero suppressed readout of current crossing (Informative)
  - Bunch Crossing Type Veto (Informative)
  - Front-End electronics reset (Expect only header from FE)
- Back-End Reset (Header Only from FE during reset)
- Trigger
  - Reject data (Header still sent to farm or not?)
  - Attention: In TFC word, the trigger (& MEP destination) is not associated to the transmitted BunchID and the rest of the TFC word
  - S-ODIN pipes the asynchronous local trigger information for the *maximum latency possible for BE* (How much buffering is available in BE, number of events?)
  - *Realignment of all data for BE is done in TFC+FE interface via pipeline logic*
- Trigger Type to define type of event, processing type, destination type etc
- Multi-Event Packet Destination
  - Transmitted when MEP should be closed and transmitted
- Any other needs? → Reserve bits



# TFC Back-End Word Format

**TFC Word to BE:** 44 bits (60 with Reed-Salomon encoder) @ 40 MHz = 1.76 (2.4) Gb/s

Encoding	43 .. 32	31 .. 16	15 .. 12	11 .. 8
TFC Info	BID(11..0)	MEP Dest(15..0)	Trigger Type(3..0)	Calib Type(3..0)



Constant latency after S-ODIN

- ✓ **THROTTLE Information from BE:** 1 bit per board connected to TFC Interface. Full set of bits sent to S-ODIN by TFC+FE Interface.



# Backup

CERN

# Extra slide - GBT-SCA Packet

