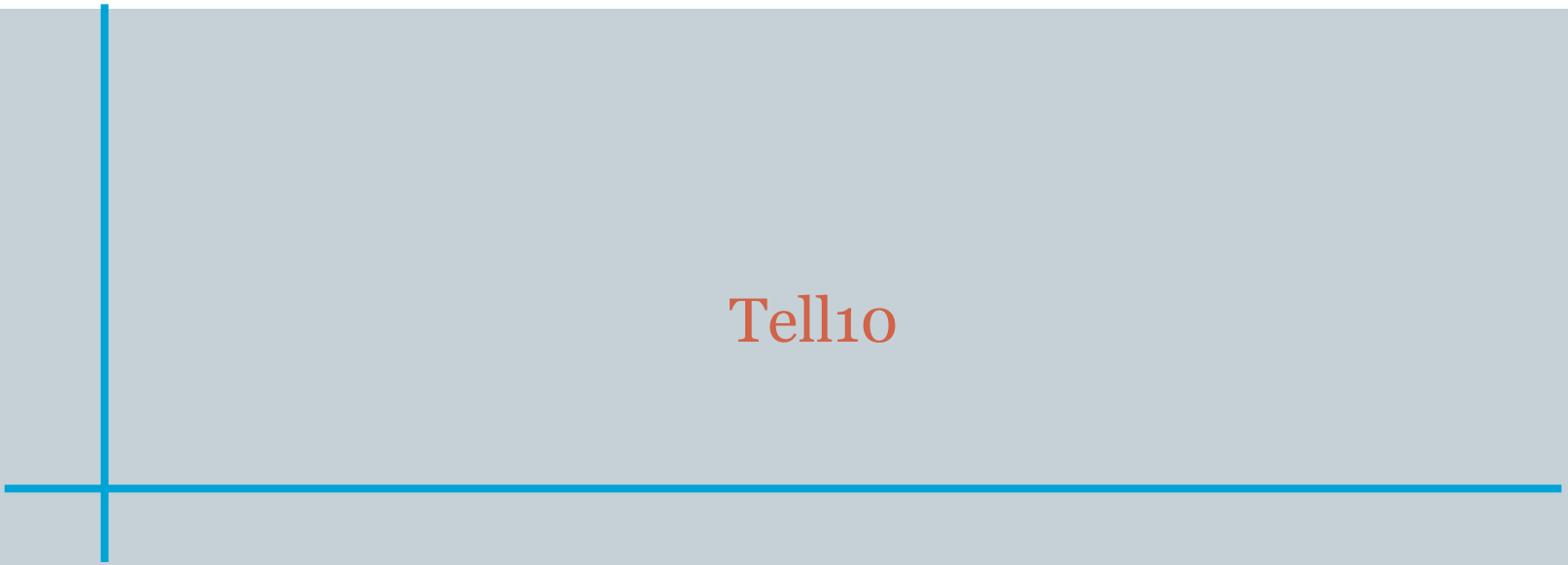
Guido Haefeli, Lausanne *Electronics upgrade meeting 10.February 2011*

Tell10



Overview

- Motivation for the development of a “second” Tell10(40)
- Description of the Tell10
- Status of the development

- Velo data processing evaluation
- Restriction to be considered

Motivation for the development of a "second" Tell10(40)

What can motivate the development of a concurrent (to the Marseille group development) Tell readout board?

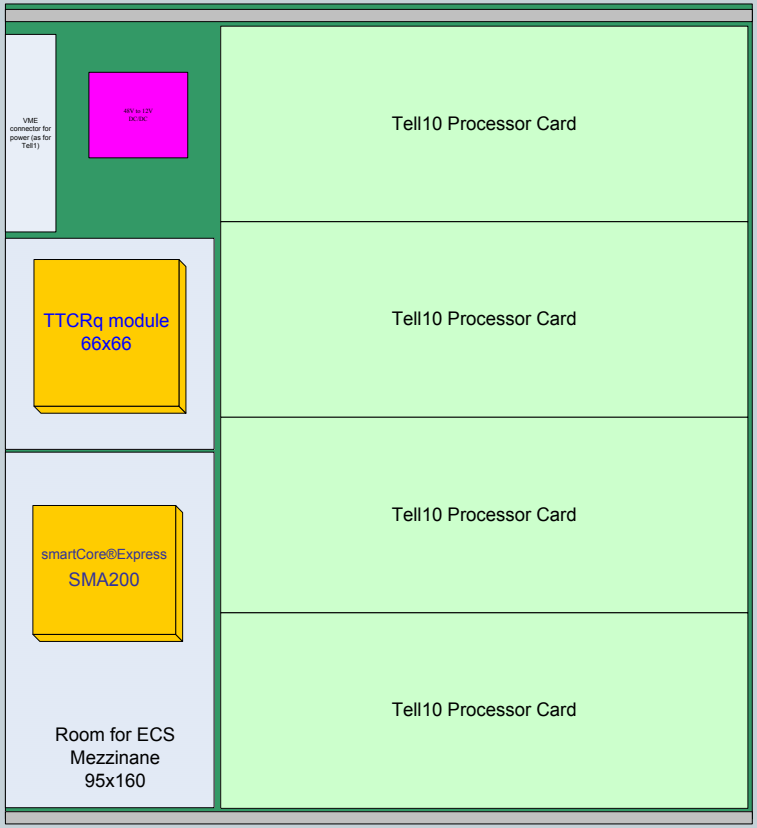
- The financial contribution by the SNF (founding agency) for a "self-made" (EPFL made) DAQ is certainly much more likely than the financial contribution to DAQ system made by foreign institutes. Note that the SNF has paid 65% of the Tell1 boards + Tell1 reproduction due to the manufacturing defects.
- Founding for the development of the Tell10 has been obtained.
- A team of 3 people are dedicated working on the project.
- Experience with the data processing and DAQ board development from Tell1 is existing.
- Chinese collaboration will be maintained and possibly extended.

Description of the Tell10

- The Tell10 development is understood has the first generation prototype towards a 40MHz readout board.
- Tell10 can be used with the current detector data and allows to use the current detector infrastructure to be used as a data source. TTC system is maintained.
- The Tell10 Processing Card can acquire 24 optical links and send the data non-zero suppressed to the DAQ, 30GBit/s input → 40 Gbit/s Ethernet output.
- The board is compatible with the current Tell1 crates.
- DAQ interface is 10G Ethernet over copper!

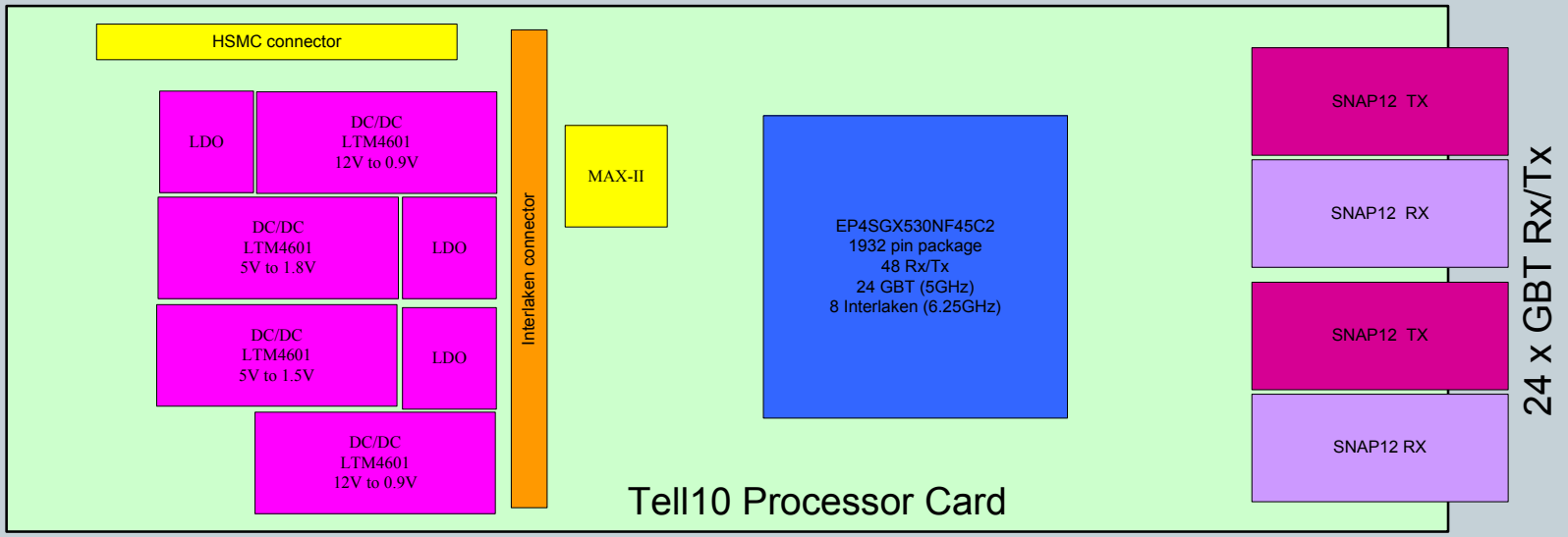
Tell10 motherboard

- 4 slots of processor mezzanine cards
- ECS interface with CCPC and GlueCard based on PCIe (Brazilian group is working on this)
- TTCRq for used with LHCb data in Tell1 mode
- Power connector and DCDC



Tell10 Processor Card

- Largest Altera Stratix 4 FPGA (design made foreseen to be upgraded to Stratix 5, 6 what ever it will be at the required time).
- 24 bidirectional GBT links
- 2 x SODIMM with 100 Gbit/s total bandwidth
- Interface connector to 10GBE NIC card



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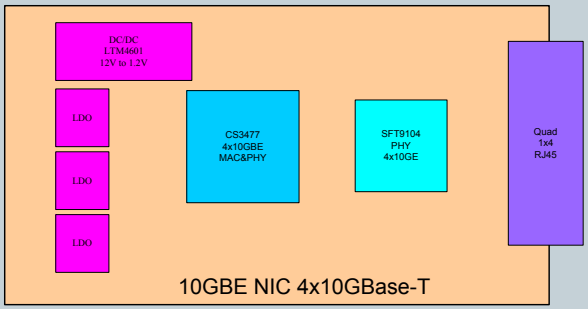
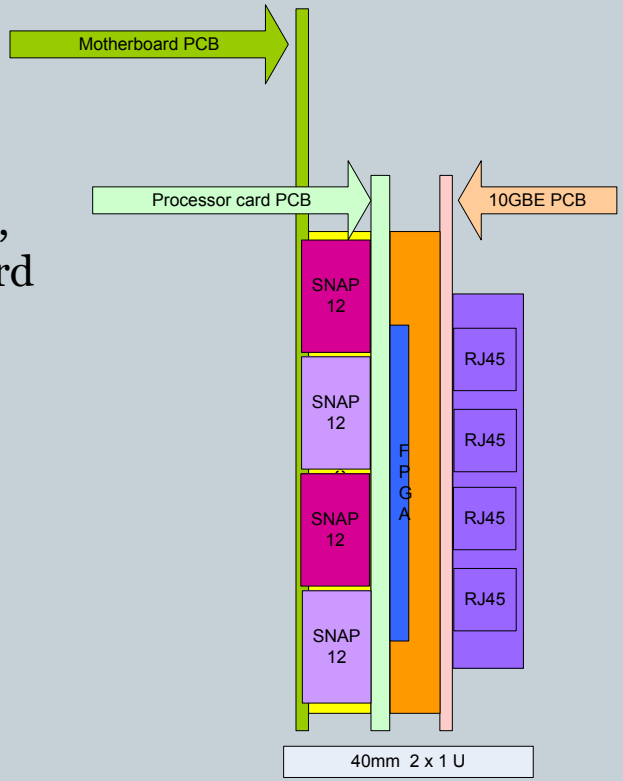
- Double width board (10/crate)
- The fact that the board is double width is not a loss of space, the power consumption is estimated to 120W/Processor Card and 500W per module. This requires 5kW of power per crate!





Status

- Schematics for motherboard, processor board and 10GE board are nearly ready for layout (2 more weeks required)
- Layout will be done by Cern central workshop.
- Prototypes are expected to be available in 3 month time.
- VHDL development is under way, this is the largest part of the hardware development.
  - Xavier Gremaud has been working for 6 month now to develop the code for a Velo pixel data processing (see his talk)
  - Control interface implemented (Weibin Pan)
  - Interlaken core for MAC interface implemented
  - DDR3 SDRAM core interface implemented

- To be done in the near future
- Implementation of a complete simulation test bed
  - Reduce time for simulation (build simulation models for SDRAM controllers)
  - Reduce time for Place and Route, use optimized incremental design flow
  - Implementing GBT for Stratix 4