Tell40: Status of development

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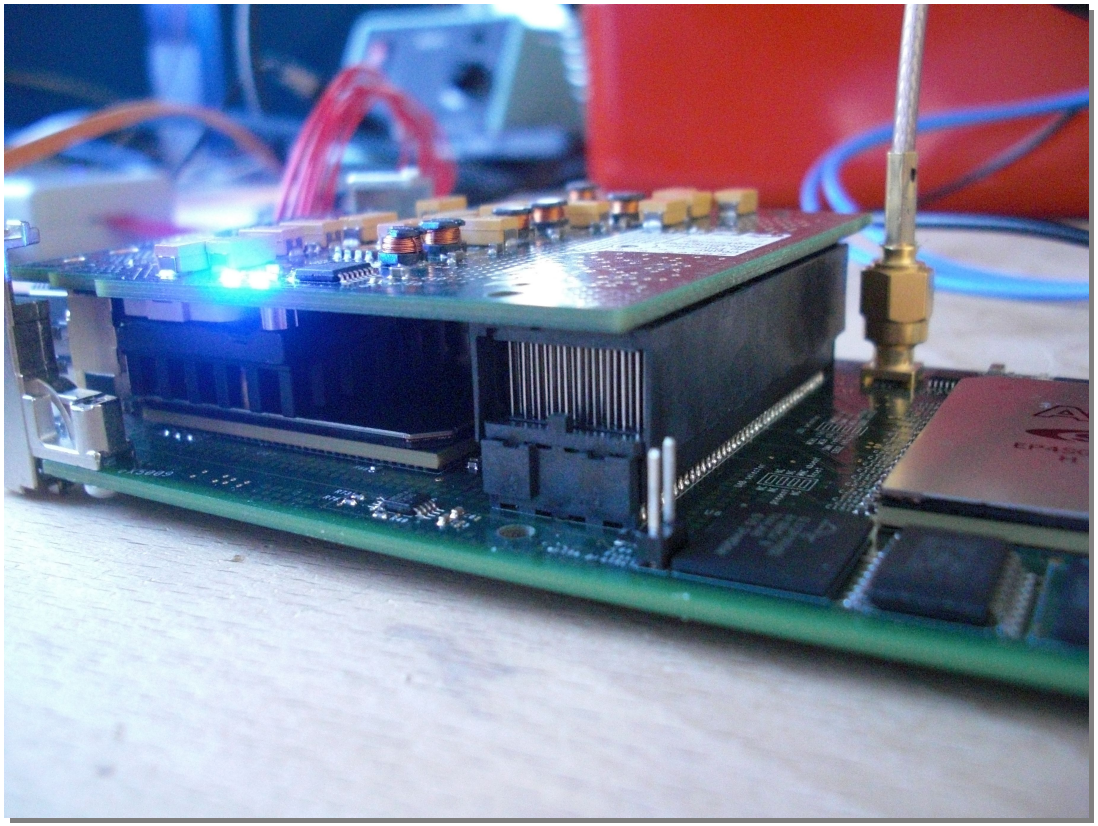
Outline

- Current status of AMC Stratix 4
- 10 Gbits/s design
- Clock phase issues
- AMC Stratix 5
- ATCA40 board
- Schedule
- Test benches + Firmware development

Current status of AMC board

- Serial links fully tested on mezzanine at 4.8 Gbits/s and 8 Gbits/s
- Protocol GBT OK
- 64 Mb Dynamic RAM access OK
- Gigabit Ethernet interface OK
- Embedded NIOS core implemented
- Simple socket server implemented on NIOS core



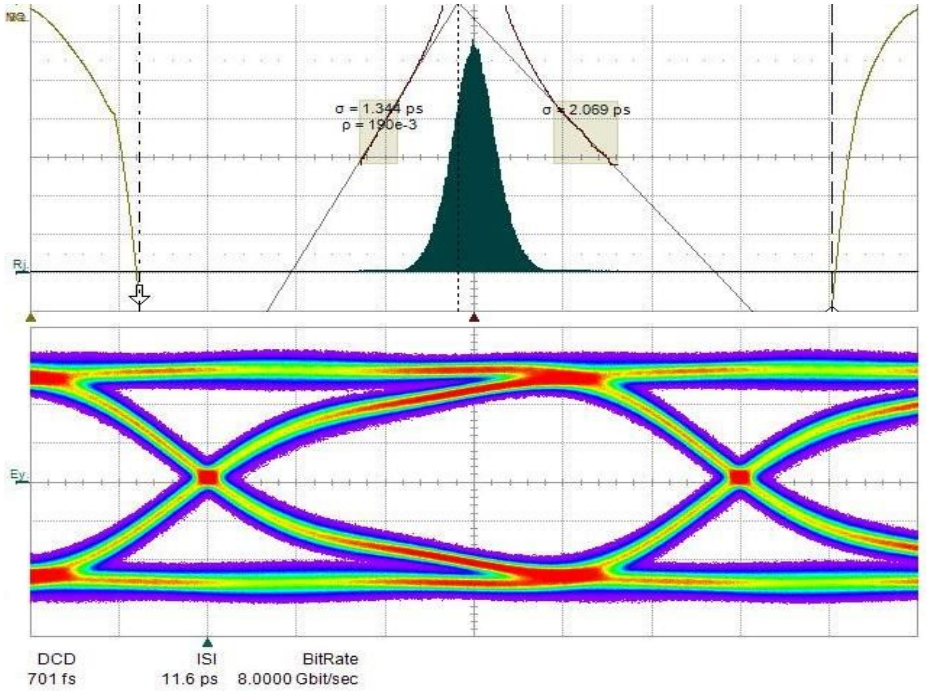
10 Gbits/s design

Can we design securely at 10 Gbits/s with current routing rules, via types and connectors ?

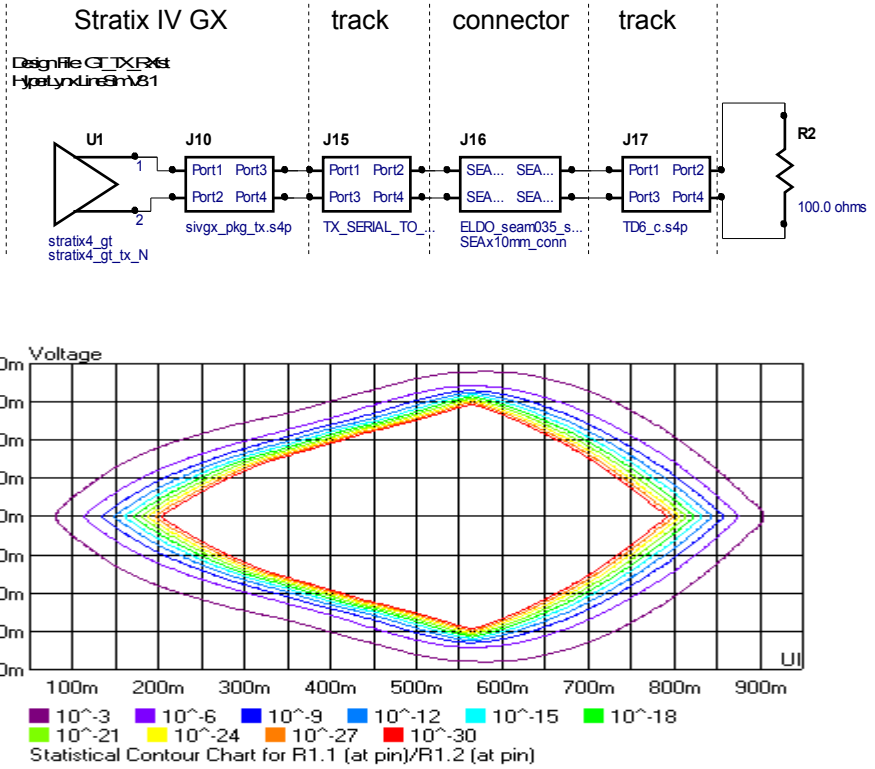
- Eye diagram measurements at 8 Gbits/s as reference
- Simulations and coherence check between measures and simulations
- Optimization of pre-emphasis and equalization filters
- Simulations at 10 Gbits/s and validation of design
- Refinement of simulations:
  - TDR measurements to obtain more acurate model of full data path
  - Extraction of S-parameters

Comparison between simulations and measurements at 8 Gbits/s

- One way simulation between FPGA and optical device



Measurement

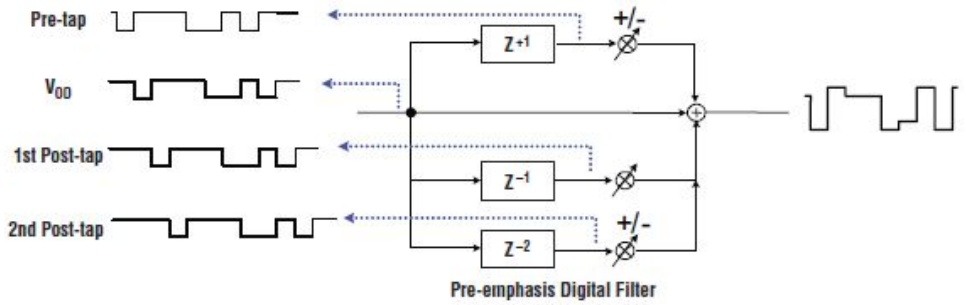


Simulation

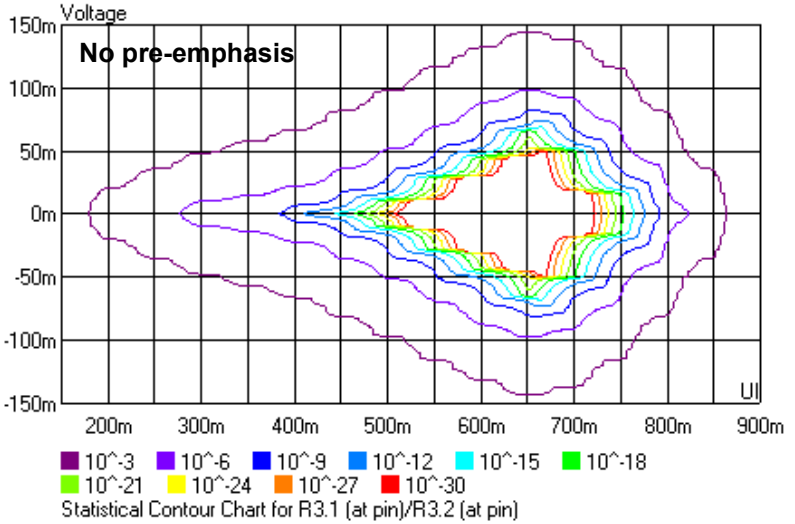
- Measured opening at 10^{-16} : 0.78 UI
  Simulated opening at 10^{-16} : 0.67 UI

  - ➔ Simulation more pessimistic but approximations in the connector model

Simulation and preemphasis at 10 Gbits/s

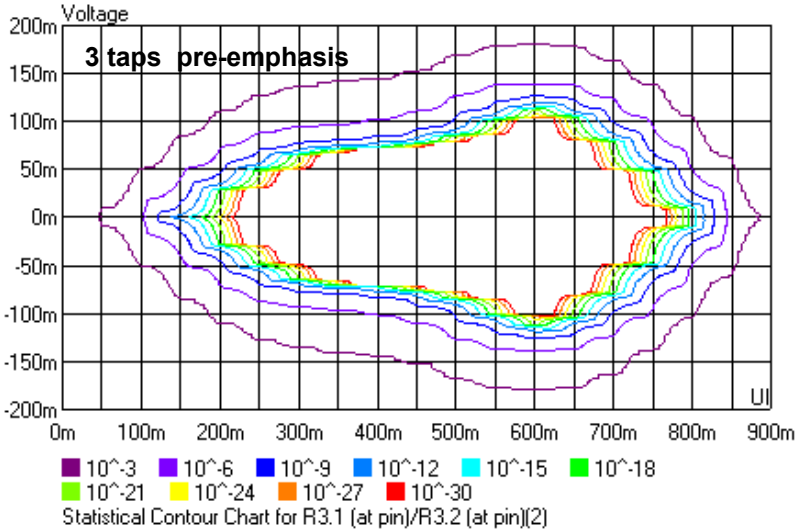


Preemphasis principle



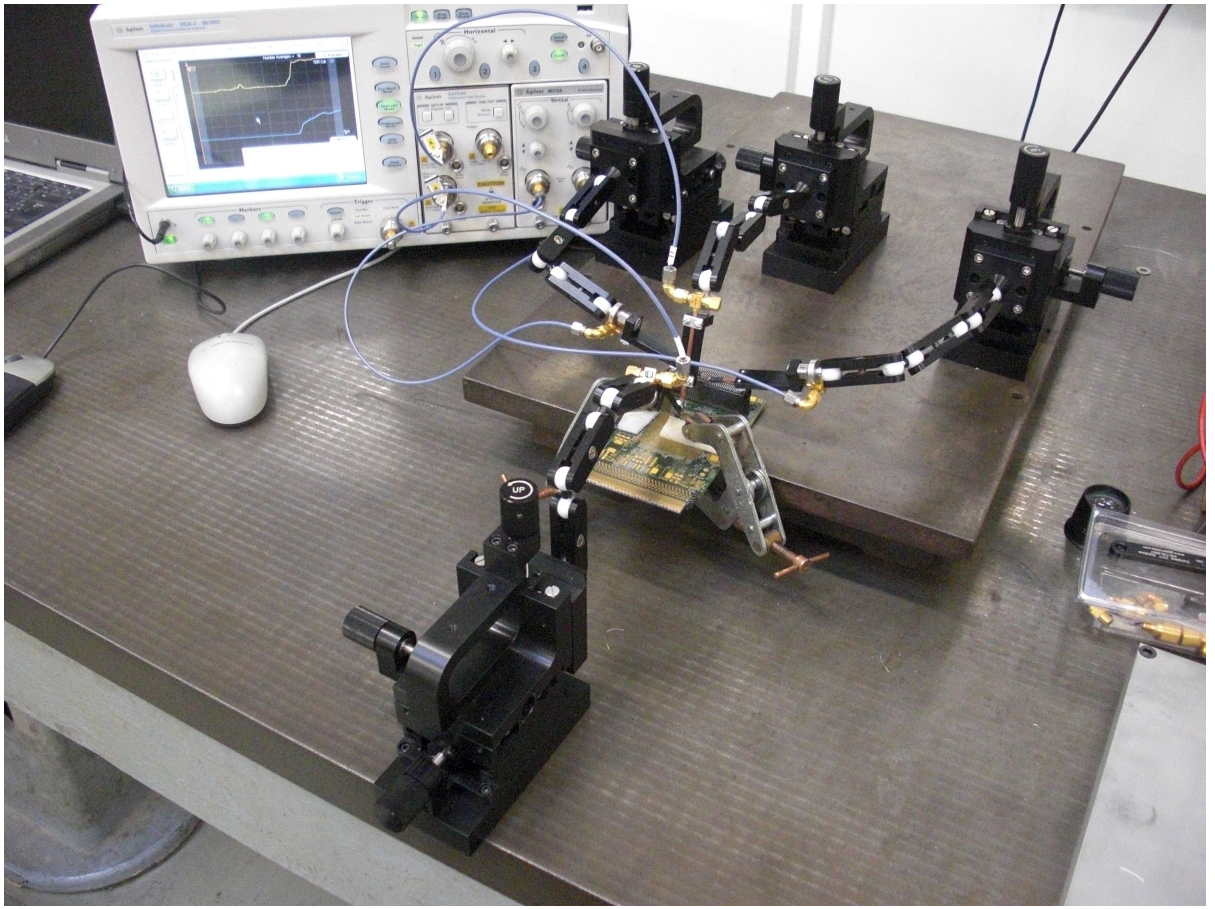
- Without preemplasis
  Simulated opening at 10^{-16} : 0.31 UI
- With preemphasis
  Simulated opening at 10^{-16} : 0.63 UI
  (was 0.67 UI at 8 Gbits/s without error)
  - Preemphasis cancels the eye closure
  - Still some margin on the receiver side with equalization (cannot be simulated)

➡ **Mezzanine concept at 10 Gbits/s OK**



Refining results

- Requires a better model for connector and tracks
- Can be extracted by measurements of characteristics by Time Domain Reflection



Measurement setup

Clock phase

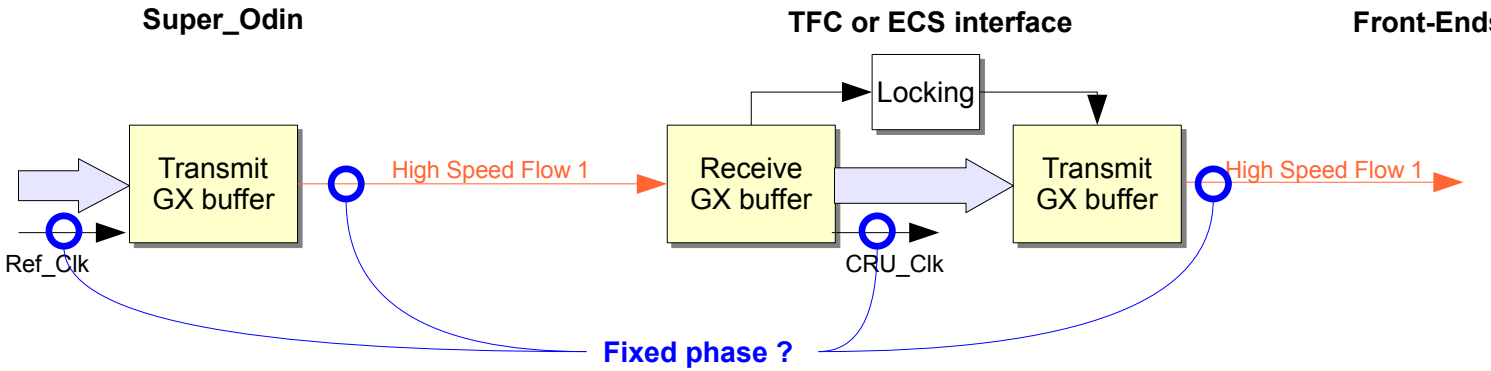
Two problems

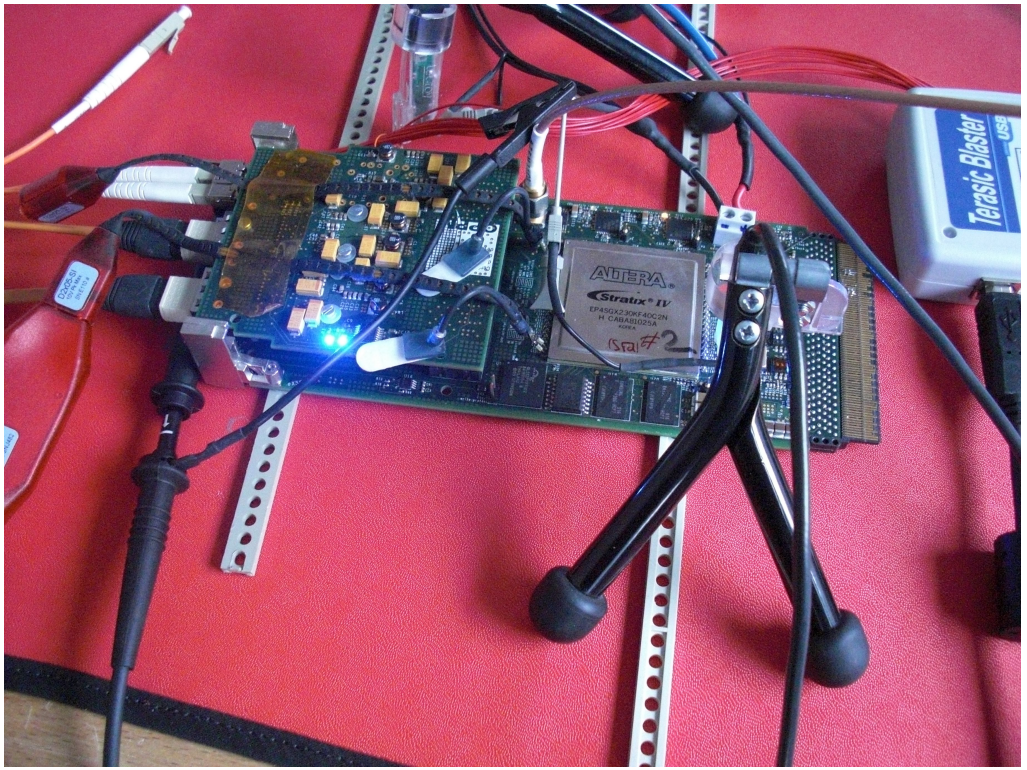
- **Does the phase of a high speed serial flow changes after several power on and off** ? (condition for the GBT to extract a clock with fixed phase)
  - Depends of PLL behaviour
- Optionally, can we extract a TFC clock from a high speed serial link with:
  - a **sufficient precision**
  - a **fixed phase**
  - or propagate the serial flow with a constant phase?
    - Possible use : link between Super_Odin and BE or FE

Approach:

- Use the current design to simulate a clock/serialisation/deserialization/re-serialization
- Check timing consistency after power down and up

Clock stability measurements





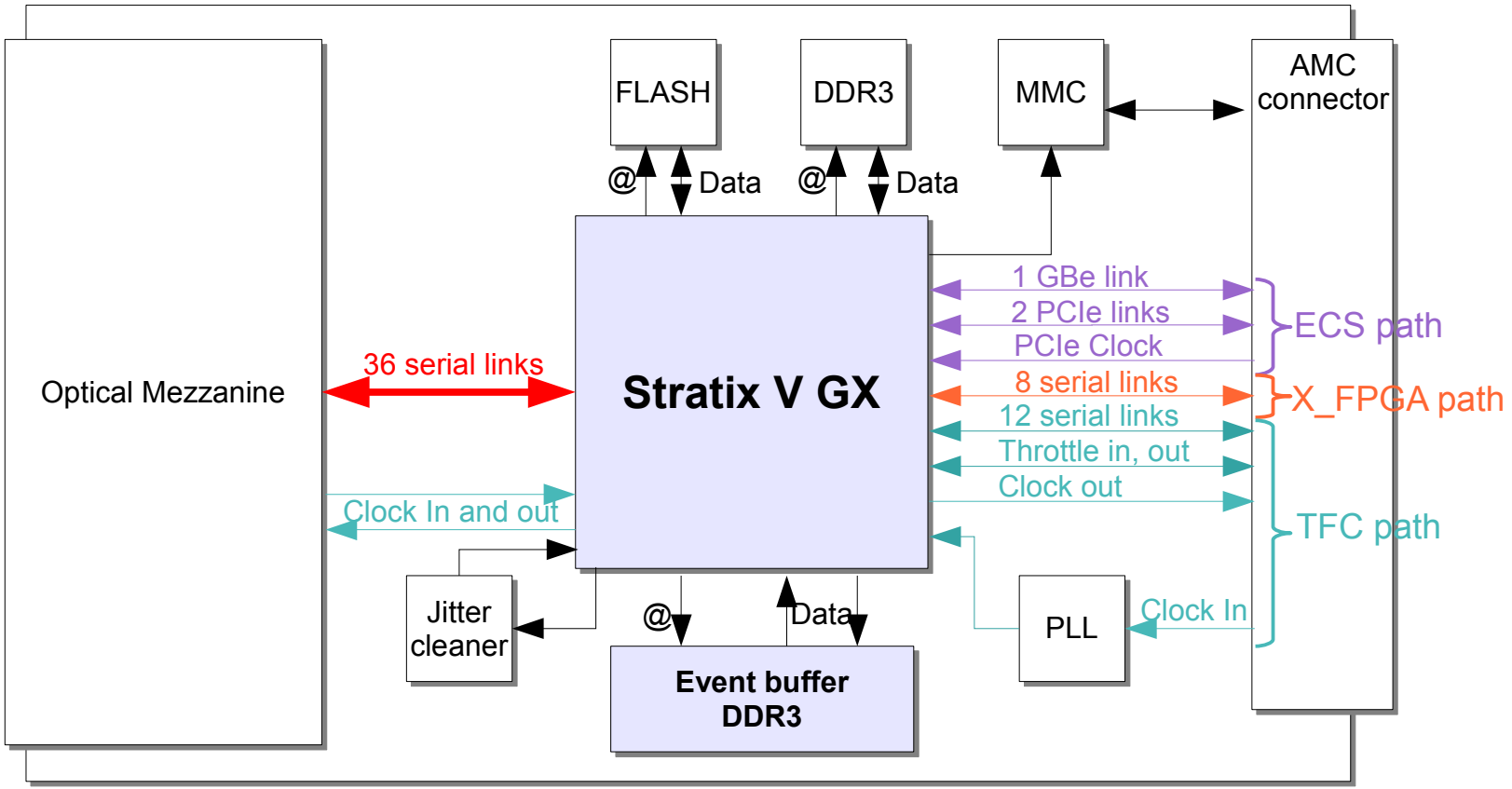
- Current setup can test this
- Special mechanism present in Stratix IV GX allowing to lock serial flows
  - under study
  - help of Richard and Federico welcome

Generic building set for TELL40, TRIG40, ECS40, Super_ODIN

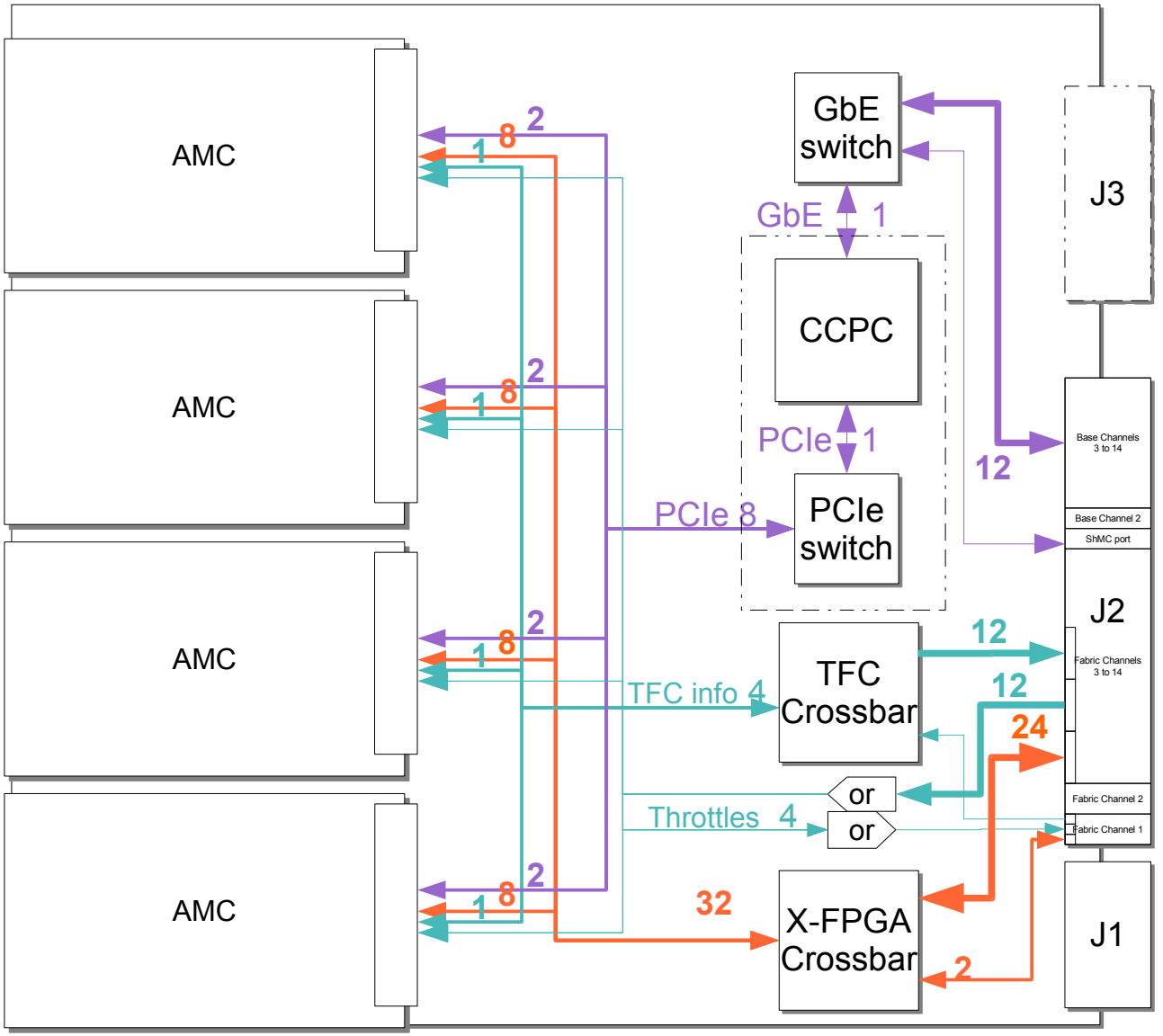
10 Gbits/s AMC board with Stratix V

- One FPGA instead of two at the same cost and same number of cells
- Let room to add **external RAM for an event buffer**
- **Up to 66 serial links**,
  - All at 10 Gbits/s: no placement constraints
  - Allows more links toward AMC connector
  - **36 links to mezzanine** instead of 32: full use of 3 SNAP12
  - Allows **more concentrating power** :
    - With 2 Stratix IV GT 12 links concatenated on one 10 GbE link
    - With 1 Stratix V GX 24 links concatenated on one 10 GbE link
- Ready for a future GBT at 10 Gbits/s if any

Generic AMC board

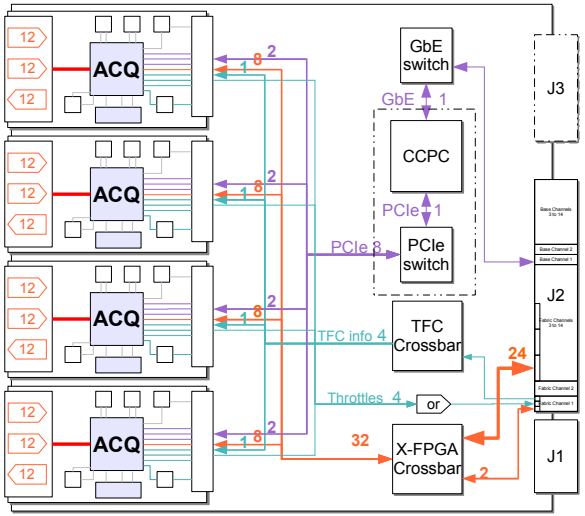


Generic ATCA board

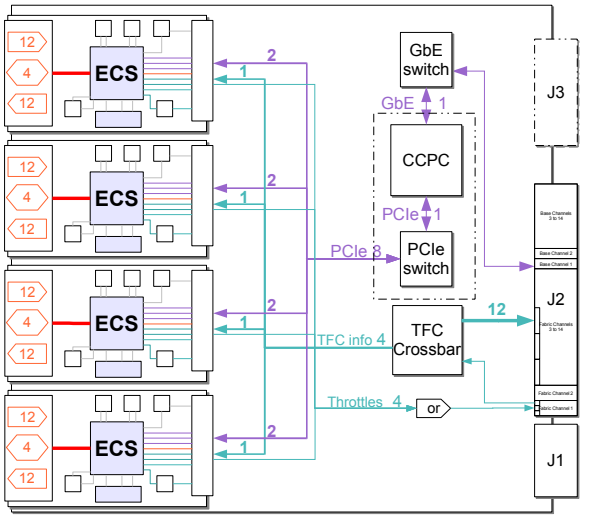


ATCA + AMC → 5 Configurations

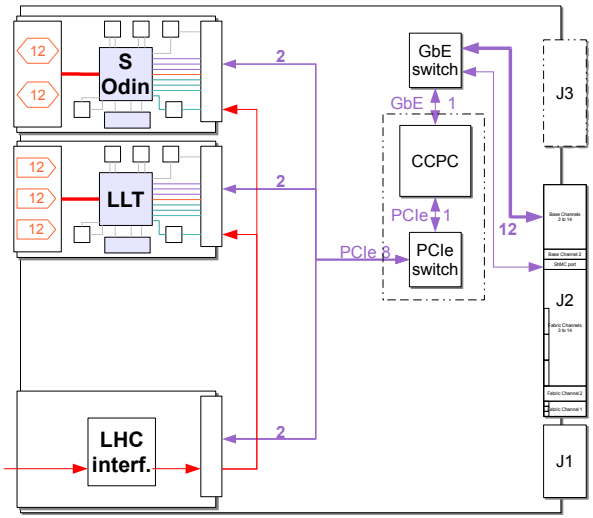
TELL40
or
TRG40



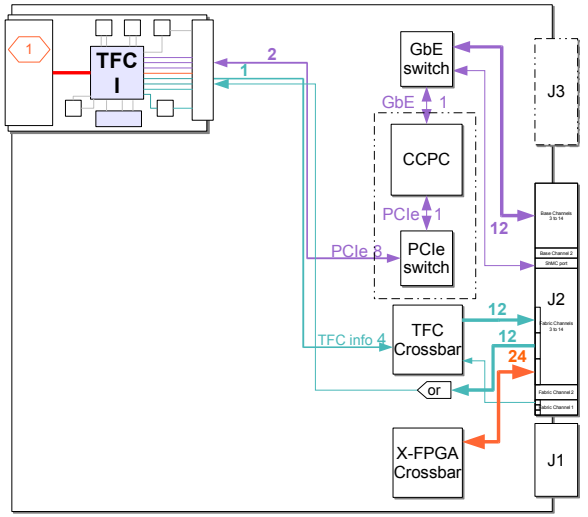
ECS40



Super_ODIN

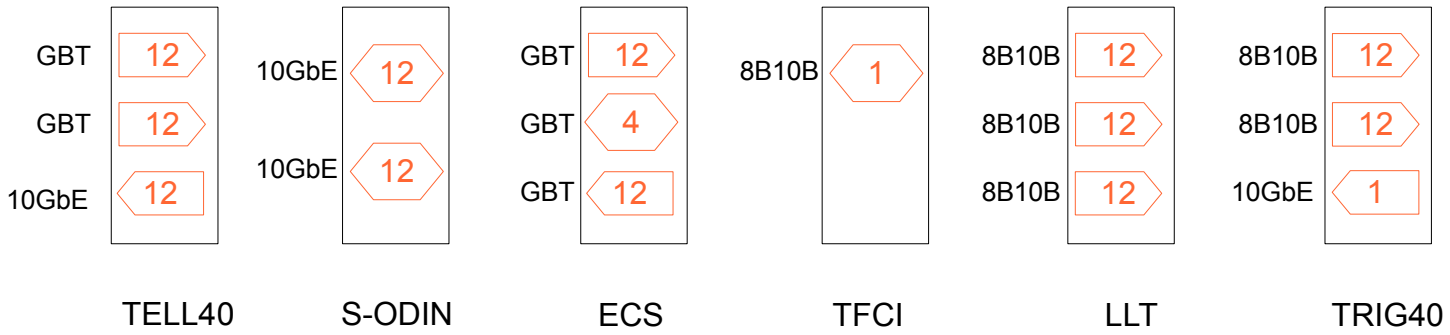


TFC_Interface

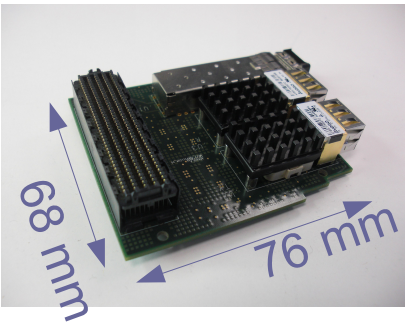


Few objects to develop

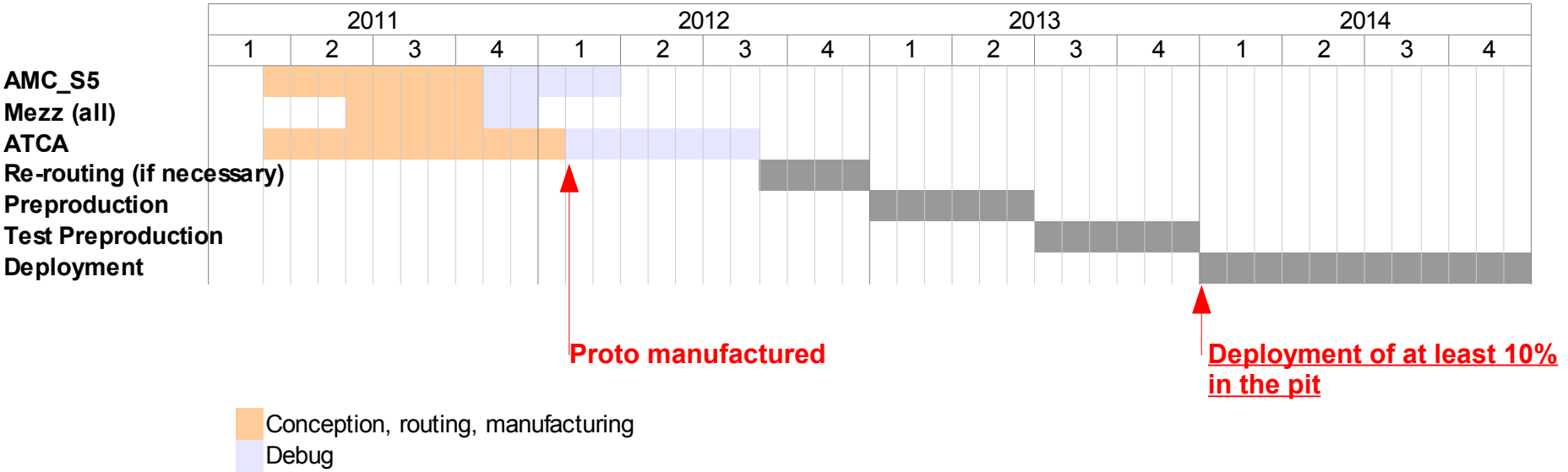
- **1 Generic ATCA board**
- **1 Generic AMC board**
- **1 AMC board** to interface with LHC timing and control
- **6 types of mezzanine boards**, maybe less ..



- Easy to design a mezzanine board.



Schedule


2011
2012
2013
2014
1 2 3 4 1 2 3 4 1 2 3 4 1 2 3 4
AMC_S5
Mezz (all)
ATCA
Re-routing (if necessary)
Preproduction
Test Preproduction
Deployment
Proto manufactured
Deployment of at least 10% in the pit
Conception, routing, manufacturing
Debug

Test benches
Firmware development

Needs

- Different firmwares have to be developped in each context (TELL40, ECS40, Super_ODIN, TFC_Interface, TRIG40, ...)
- It requires:
  - Common test benches, available early
  - Common control environment
  - Early availability of hardware

Very early test setup

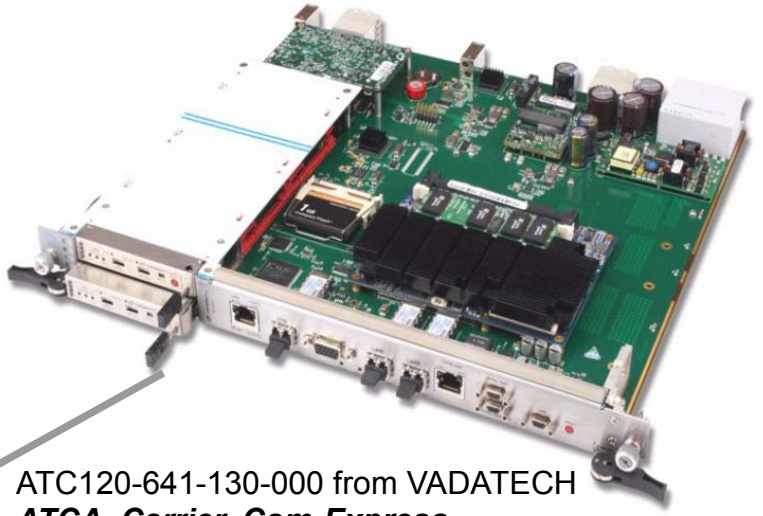
Duplication of current AMC Stratix 4 GX

- 2 already available for early bird developers
  - Single Stratix IV FPFA
  - 6 optical links in at 4.8 Gbits/s
  - 6 optical links out at 4.8 Gbits/s
  - 1 biduirectional 8 Gbit/s link
- Stand alone mode:
  - single 12V power suplly
  - Control by NIOS core through JTAG link

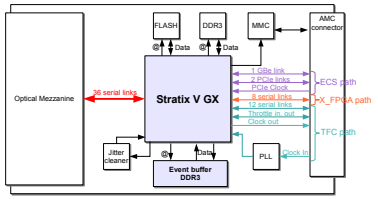
Basic test setup

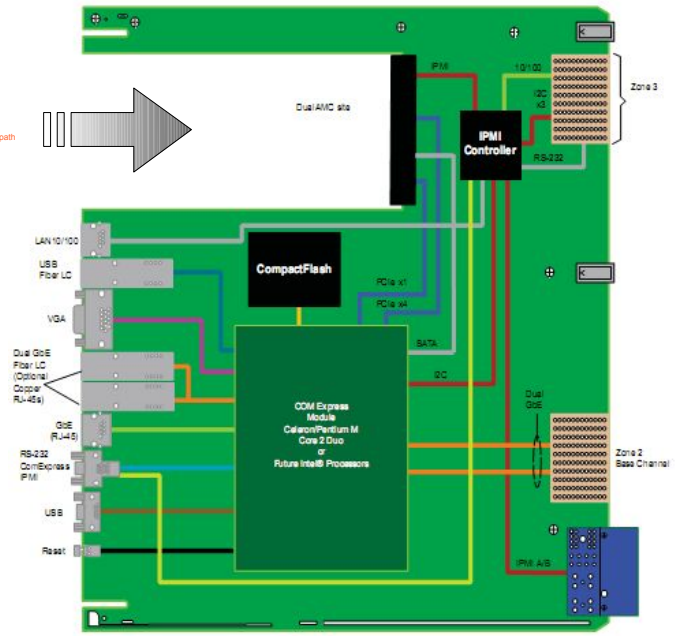
Simple and compact setup

- Available end 2011



ATC120-641-130-000 from VADATECH
ATCA, Carrier, Com-Express,
Core i-7 @Ghz COM Express Module,
4GByte System DDR3 SDRAM Memory, 1 Gbyte CompactFlash,
Node board, Copper front panel GbE interface





Centellis 2000 from Emerson
AdvancedTCA Platform
2 slots + ShManager

- ATC120 board replaced by final ATCA board available beginning 2012, same test crate

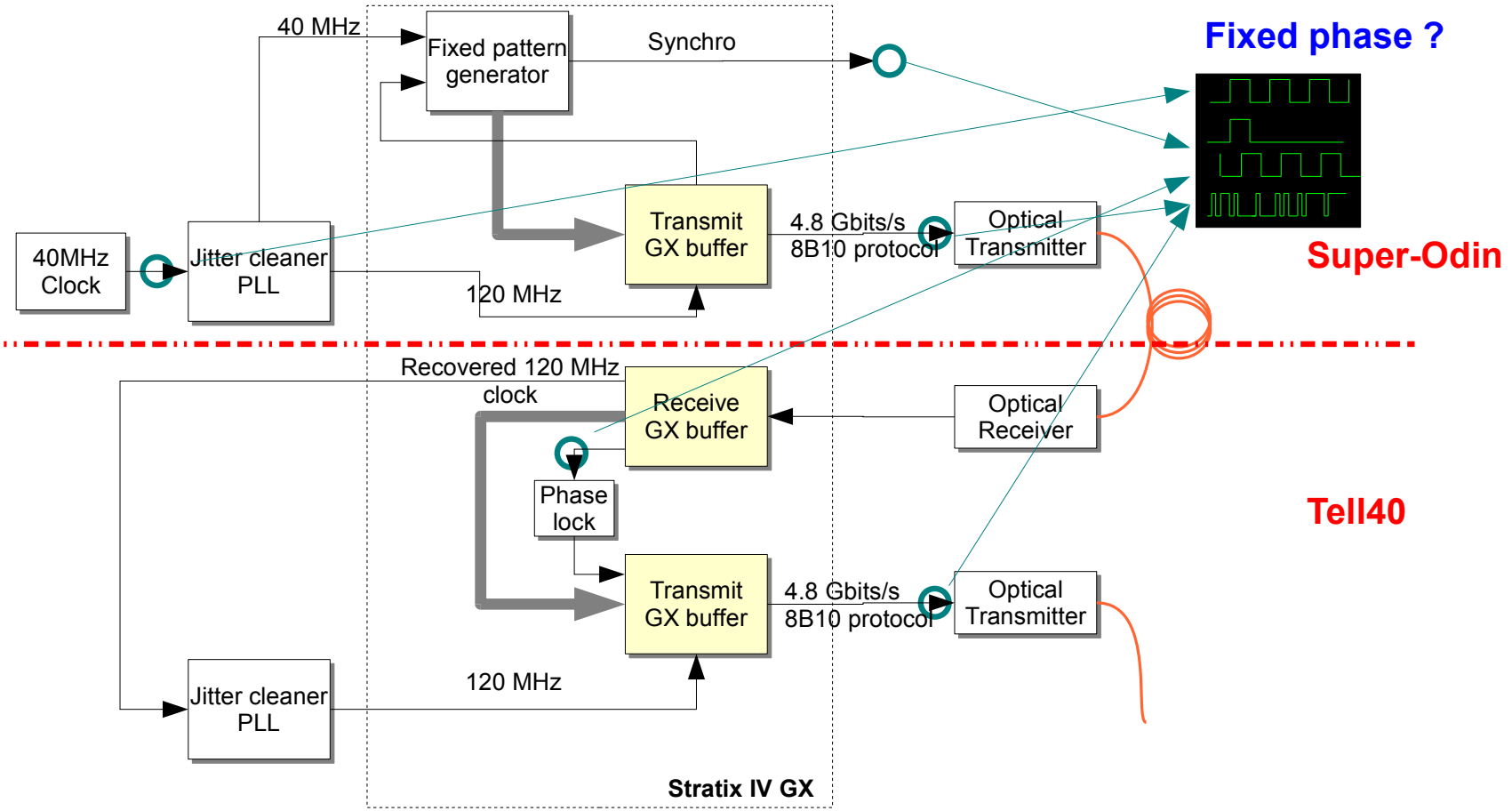
Summary

- All the elementary blocks tested and ready to be re-implemented in a Tell40 prototype 0
- Mezzanine concept at 10 Gbits/s is feasible
- Propagation of clock mixed with data between Super-Odin and TFC interfaces has to be checked
  - Measurements ongoing
  - Fallback solution : dedicated link (TTCrx-like)
- Flexible concept:
  - Generic ATCA board + generic AMC board + customized mezzanines addresses all of the needs (TELL40, ECS40, TRIG40, Super_ODIN, etc …)
- Common organization for firmwares development is mandatory
- Test setup available now with existing boards
- Full prototype available begining 2012
- Deployment of at least 10% at pit possible end 2013

Backup

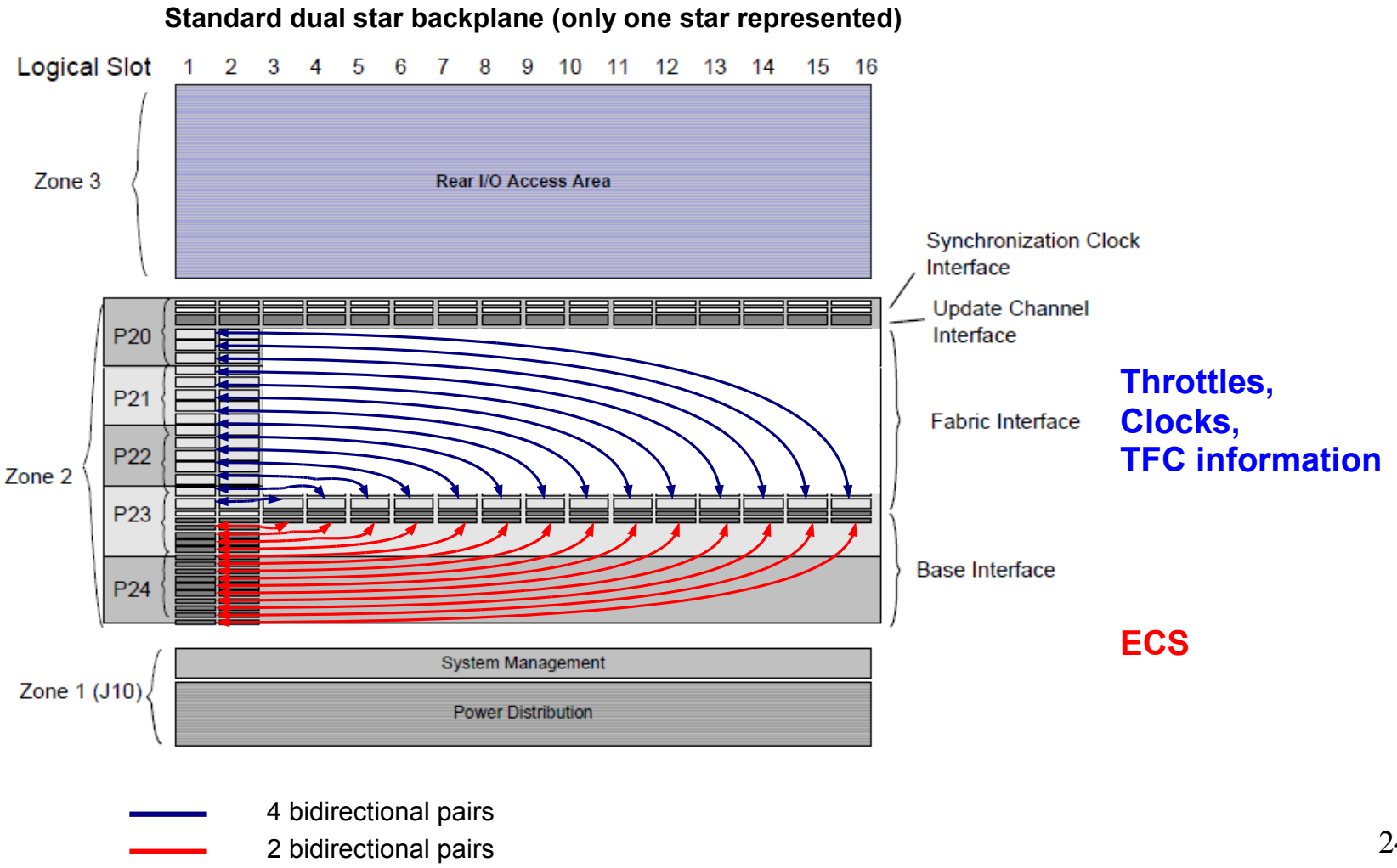
Clock stability setup

Ongoing work

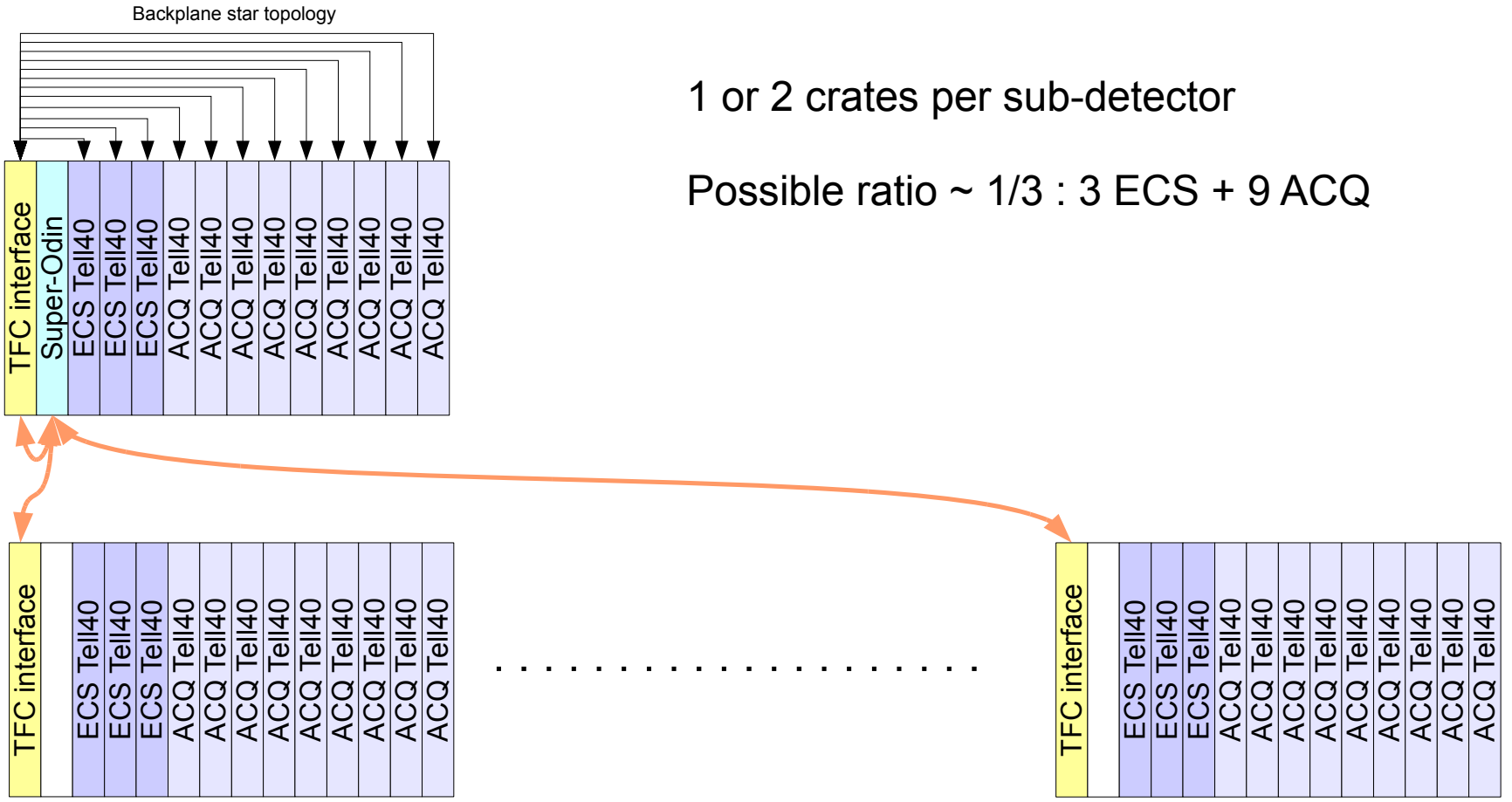


Connectivity between boards

Relies on powerful connectivity coming with the ATCA standard



Exemple of clustered architecture



1 or 2 crates per sub-detector

Possible ratio ~ 1/3 : 3 ECS + 9 ACQ