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TELL40 DATA PROCESSING

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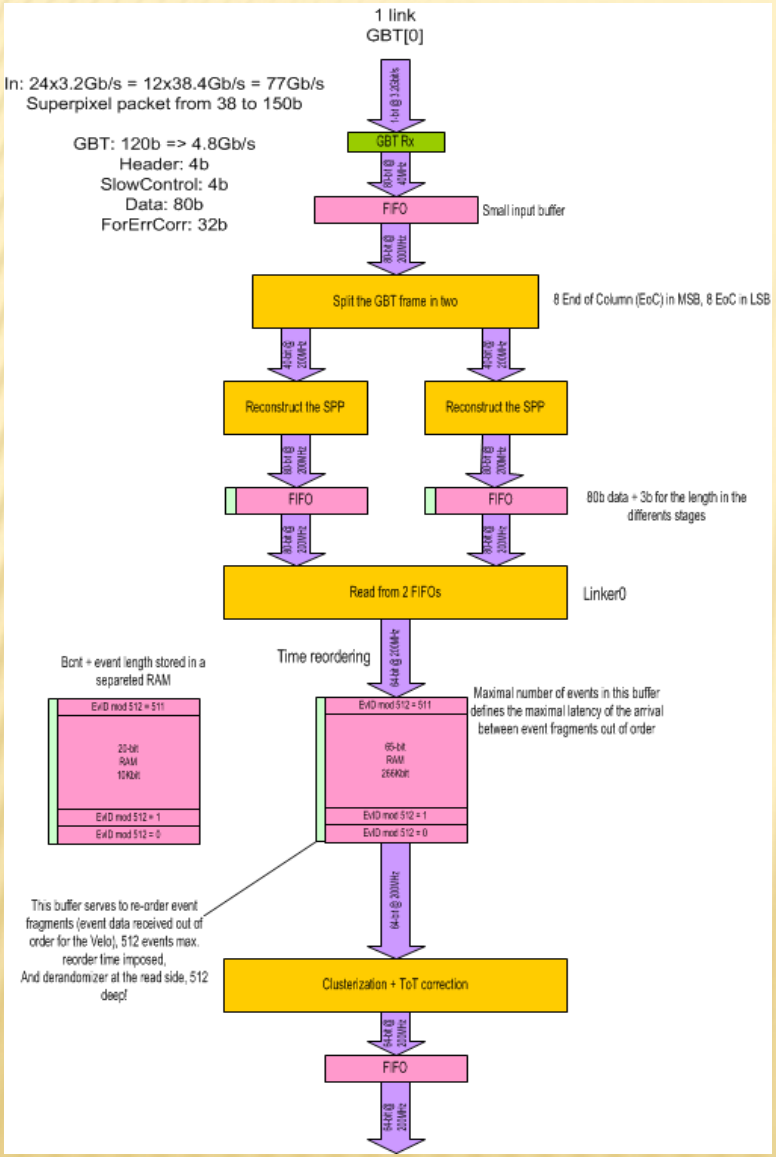
- Data flow
- Padder limitation
- Processing frequency
- Resource utilization
- Conclusion

DATA FLOW



Split the GBT data in 2x40b

Data from two column processors

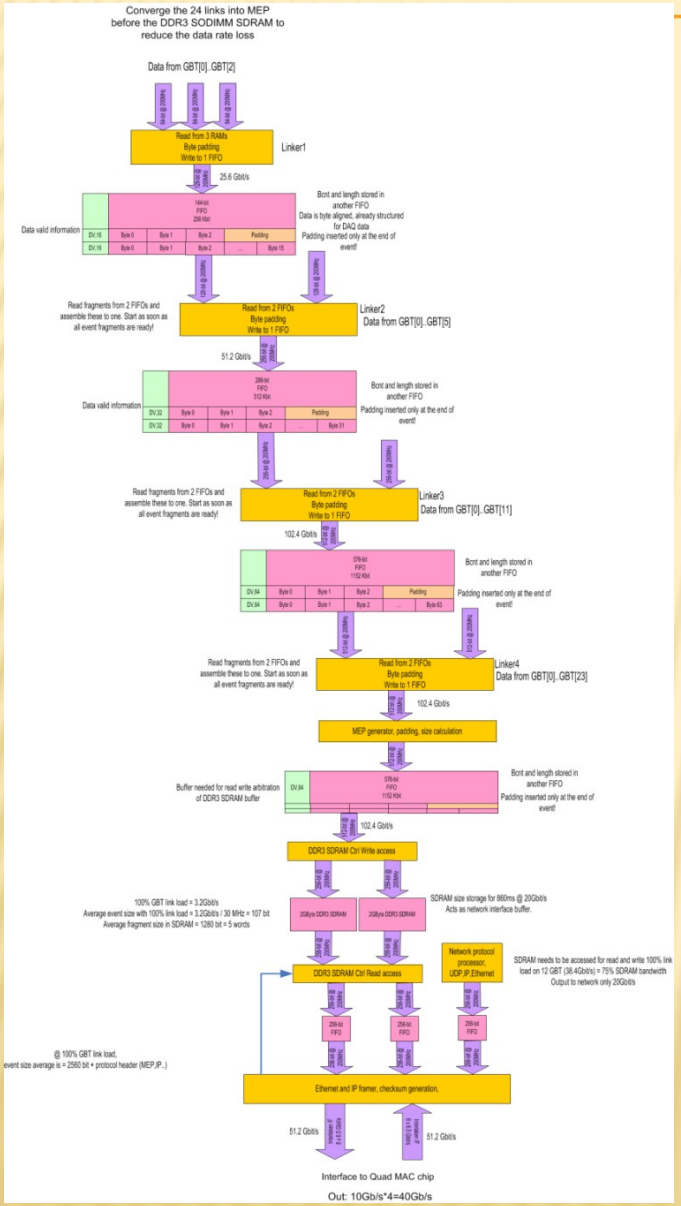
Reconstruct the Super Pixel Packet (SPP) 80b wide

Linker 0, assemble data from 2 SPP data stream

Time Reordering

Clusterization + ToT correction (subtraction) (maybe lookup table based calibration)

DATA FLOW



Linker 1, assemble data from 3 GBT, 64b->128b

Linker 2, assemble data from 2x3 GBT, 128b->256b

Linker 3, assemble data from 2x2x3 GBT, 256b->512b

Linker 4, assemble data from 2x2x2x3 GBT, 512b

MEP assembly (note : average event is only 2..4 512-bit word long)

External memory 2x256b

Ethernet framer 512b

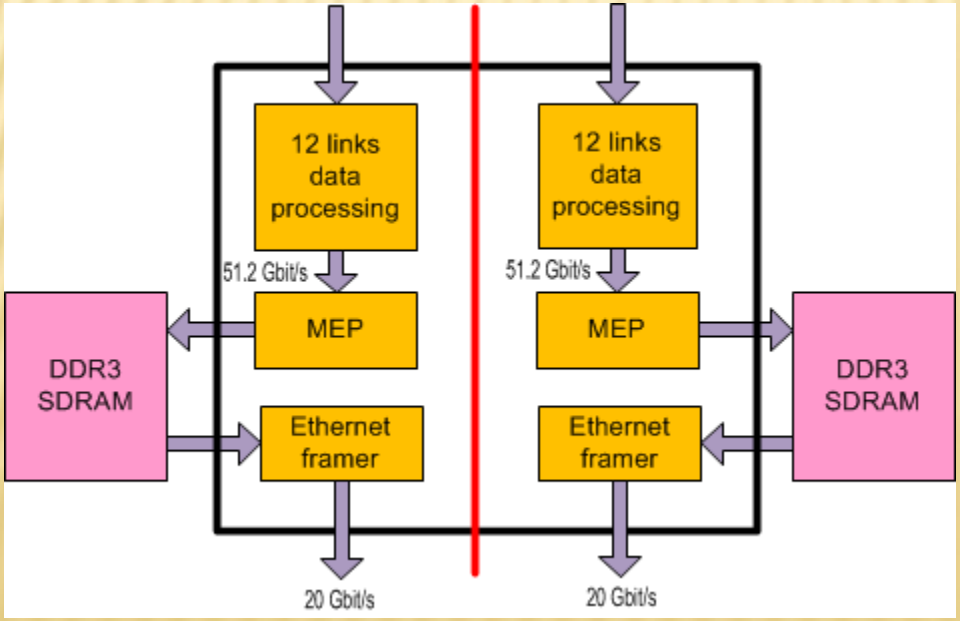
PADDER LIMITATION

- TELL40 use very wide bus (512b), that require large shift registers for padding.
- We need to use 16b and 32b padding for wide buses instead of 8b padding.
- Less resource, better timing but small increase of data size. Note that the event sizes are small and padding is important.

Padding stage	Bytes aligned	Data in width	Data out width
1	1	64b	128b
2	2	128b	256b
3	4	256b	512b
4	4	512b	512b

MEP STREAM

- It's possible to split the data processing design in two to run 2 independent 256b MEP stream.
- It allow to place and route the design more freely in the FPGA, especially with the I/O, to obtain better timings.
- It also remove the stage4 (linker4 + padder4, 512b width), small logic reduction



This results in two data sources per chip seen by the DAQ. One board gives therefore 8 sources.

PROCESSING FREQUENCY

- The design will be slower than foreseen.
- Maximum 200MHz on fastest Stratix IV seems to be the limit!
- At first sight, the limitation come from:

Part	Max frequency
Data processing only (12 links) Until one input of the linker4	250MHz
Data processing only (24 links) Until the output FIFO after the DDR3 SDRAM	230MHz
Full TELL40 VeLo design 1x512b MEP stream	200MHz (May be increased?) Core slack: +0.3 Input slack: +0.172 Output slack: +0.007

Clusterization not yet implemented

RESOURCE UTILIZATION

- The data processing require a lot of resource. For the VeLo, at the moment, we use 47% of the ALUT and 75% of large memory blocks.
- Current FPGA : EP4SGX530 (largest Altera Stratix IV device).

	Logic (ALUT)	Total memory bits	M144k blocks
Data processing	198'397 (47%)	7'484'850 (36%)	48 (75%)
FPGA	424'960	21'233'664	64

CONCLUSIONS

- The real challenge of the data processing is not to spend more than 25ns per event! Pipelining is required everywhere!
- Byte padding can't be done everywhere, small data loss.
- The data processing alone use half of the logic of the FPGA.