Radiation Hard DC-DC Converters Developed at CERN

C.Fuentes[1,3] ,F.Faccio[1], S.Michelis[1,2], G.Blanchot[1], B.Allongue[1]

CERN, PH dept, ESE group, Geneva, Switzerland [1]
EPFL, Lausanne, Switzerland [2]
UTFSM, Valparaiso, Chile [3]

Outline

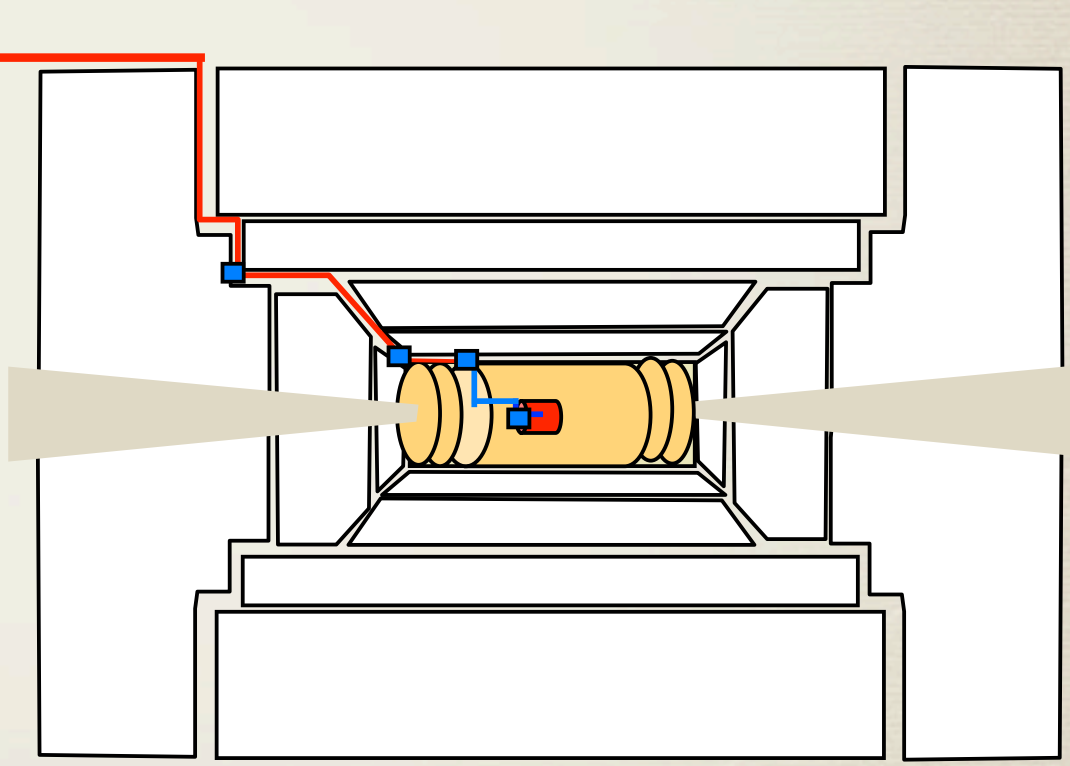
- Motivation and project goal.
- Buck converter topology.
- ASIC developments.
- DC-DC Plug-in modules.
    - Coil development.
    - Shield development.
- System tests.
- Stability and dynamic properties.
- Conclusions.

Motivation

Typical power distribution in LHC trackers:

- DC power supplies located 100 m far from detectors. (No on-detector conversion):

  -Low-voltage (2.5 -5V) required by electronics provided directly from remote back-end PS.



- Large losses in the cables.
- Cooling requirements increase mass as well.
- Cables get thinner when approaching the collision point (strict material budget).

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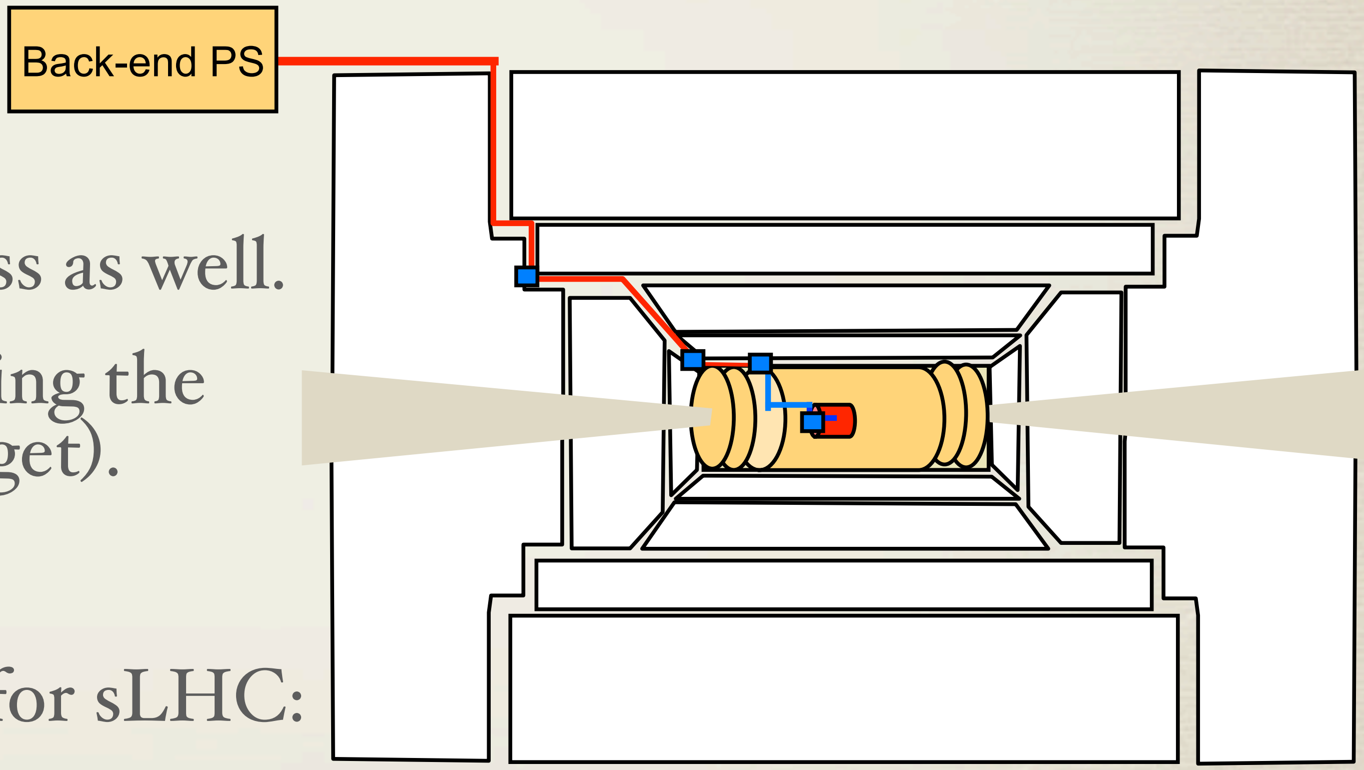

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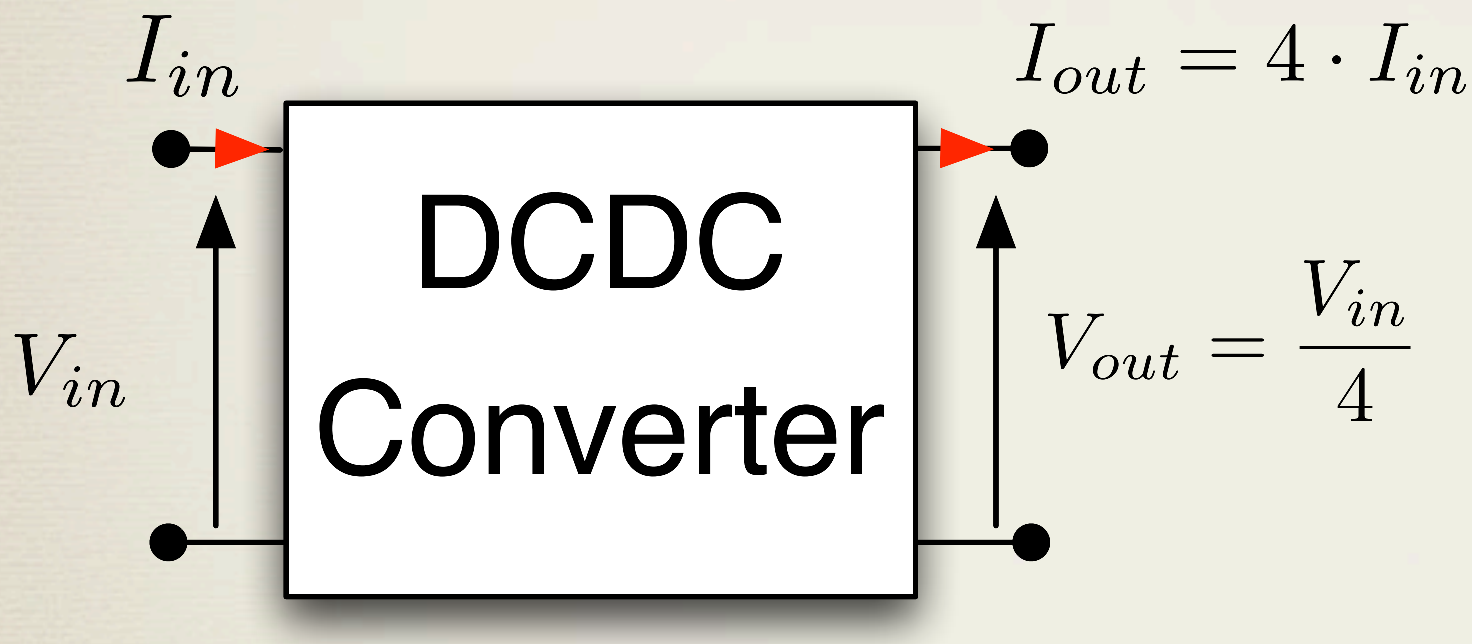
sLHC upgrade:

Actual powering scheme can **not** use for sLHC:

- Current increased x 6, cable losses x 36.
- No room for more or thicker cables.
- Material budget must be decreased.

Project goal

$$V_{in} \cdot I_{in} = V_{out} \cdot I_{out}$$



Challenges:

- Radiation tolerance.
- Magnetic field tolerance.
- Material budget and size.
- Electromagnetic noise.

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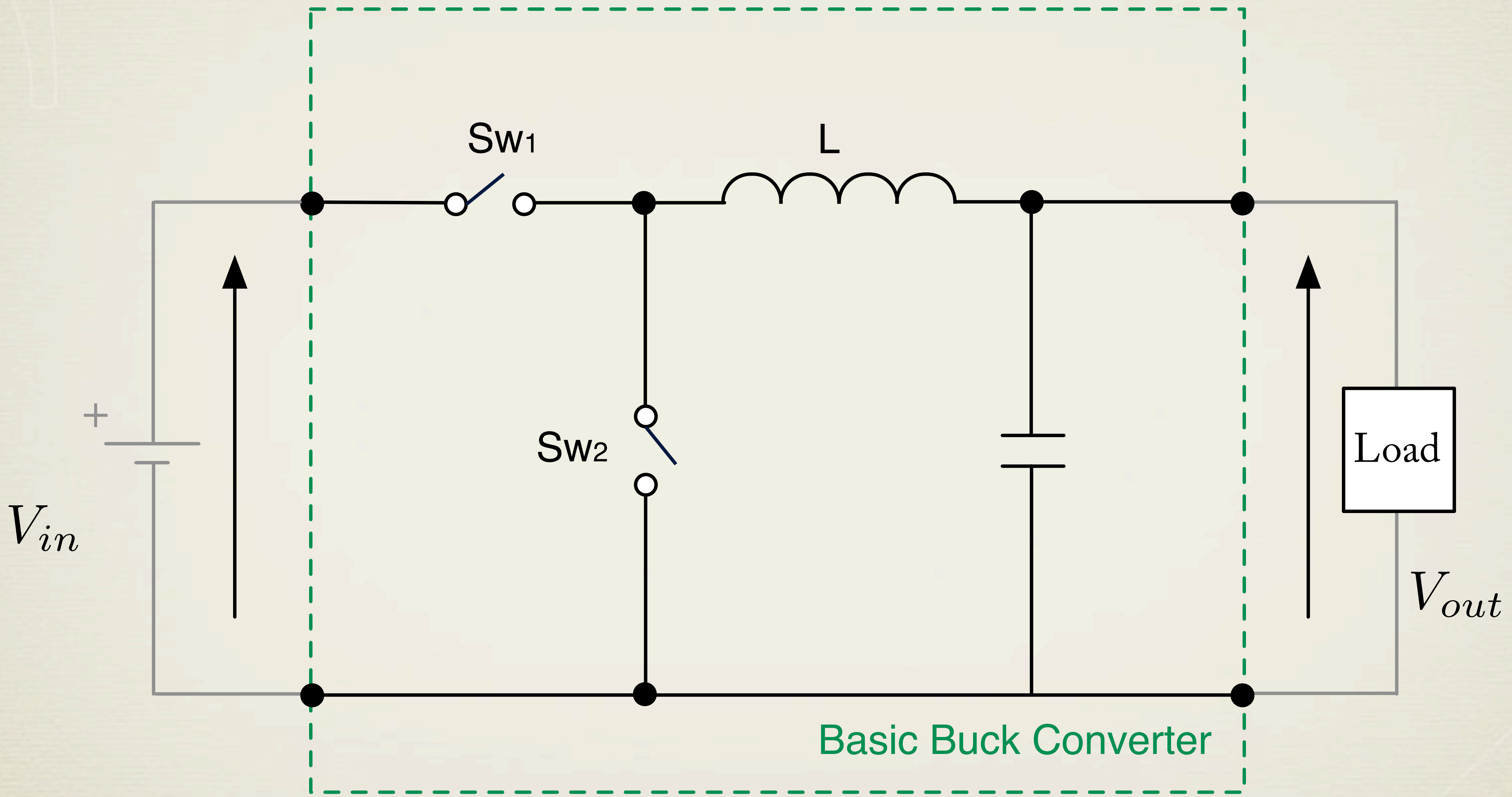

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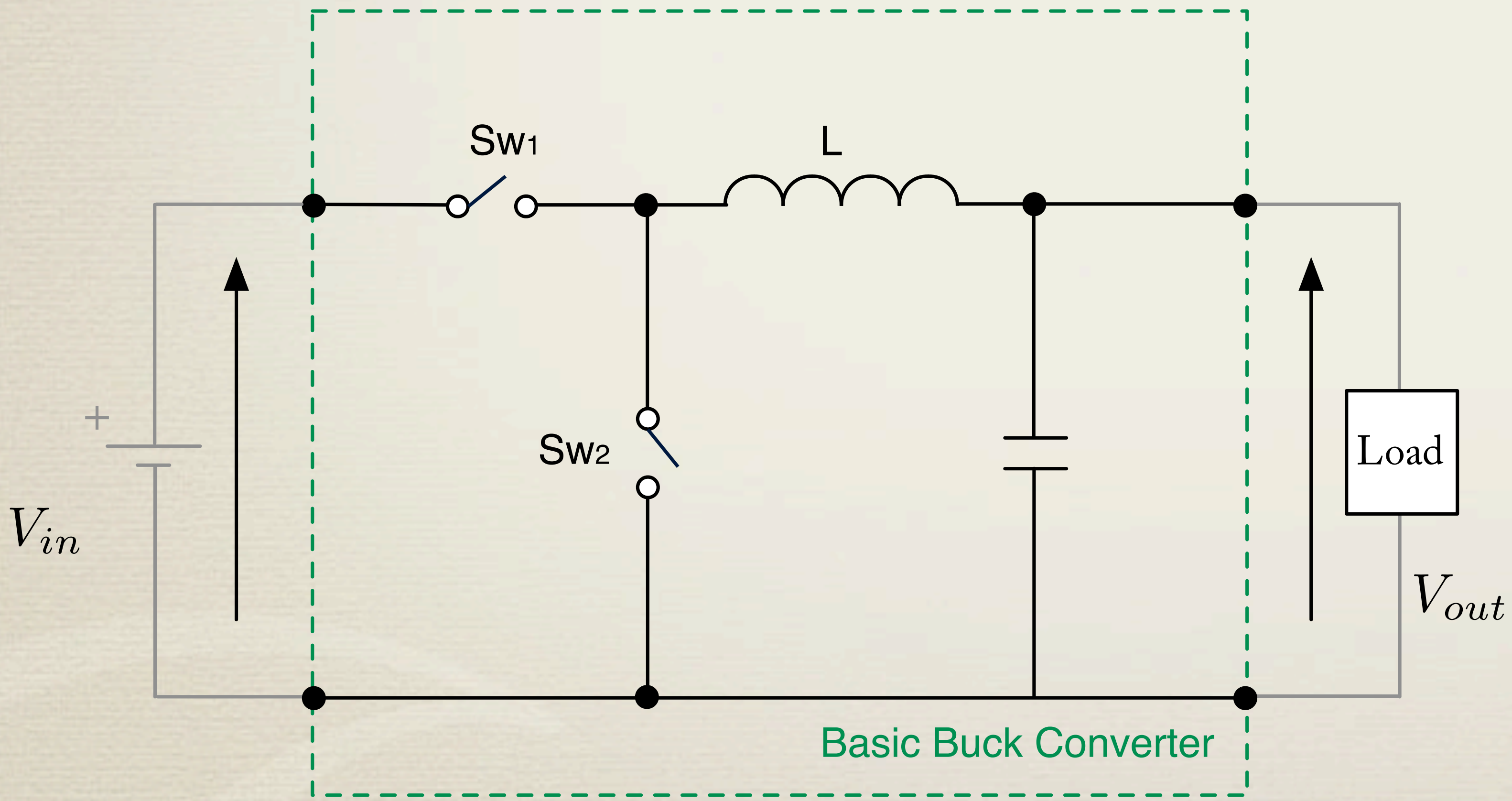

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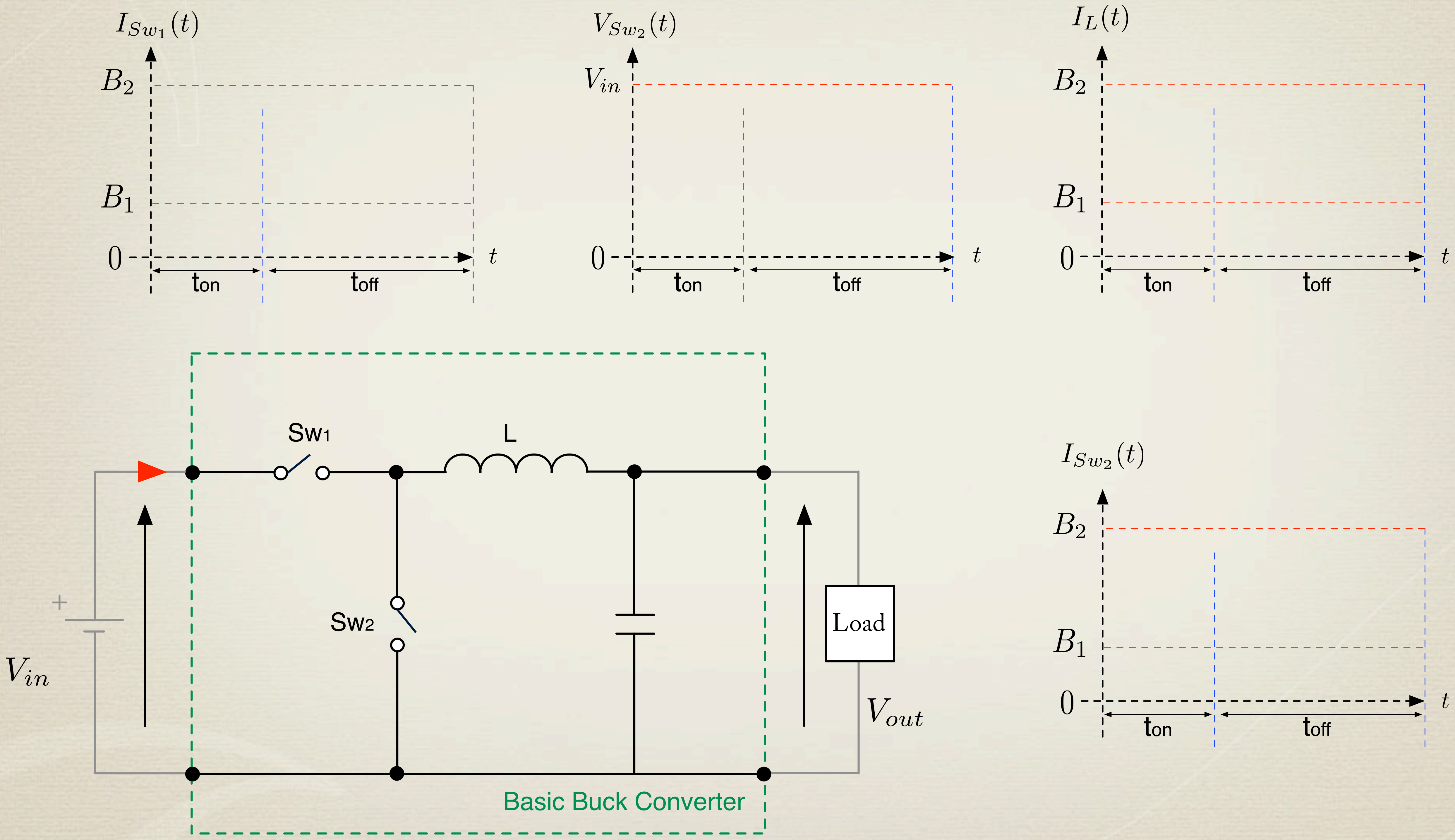

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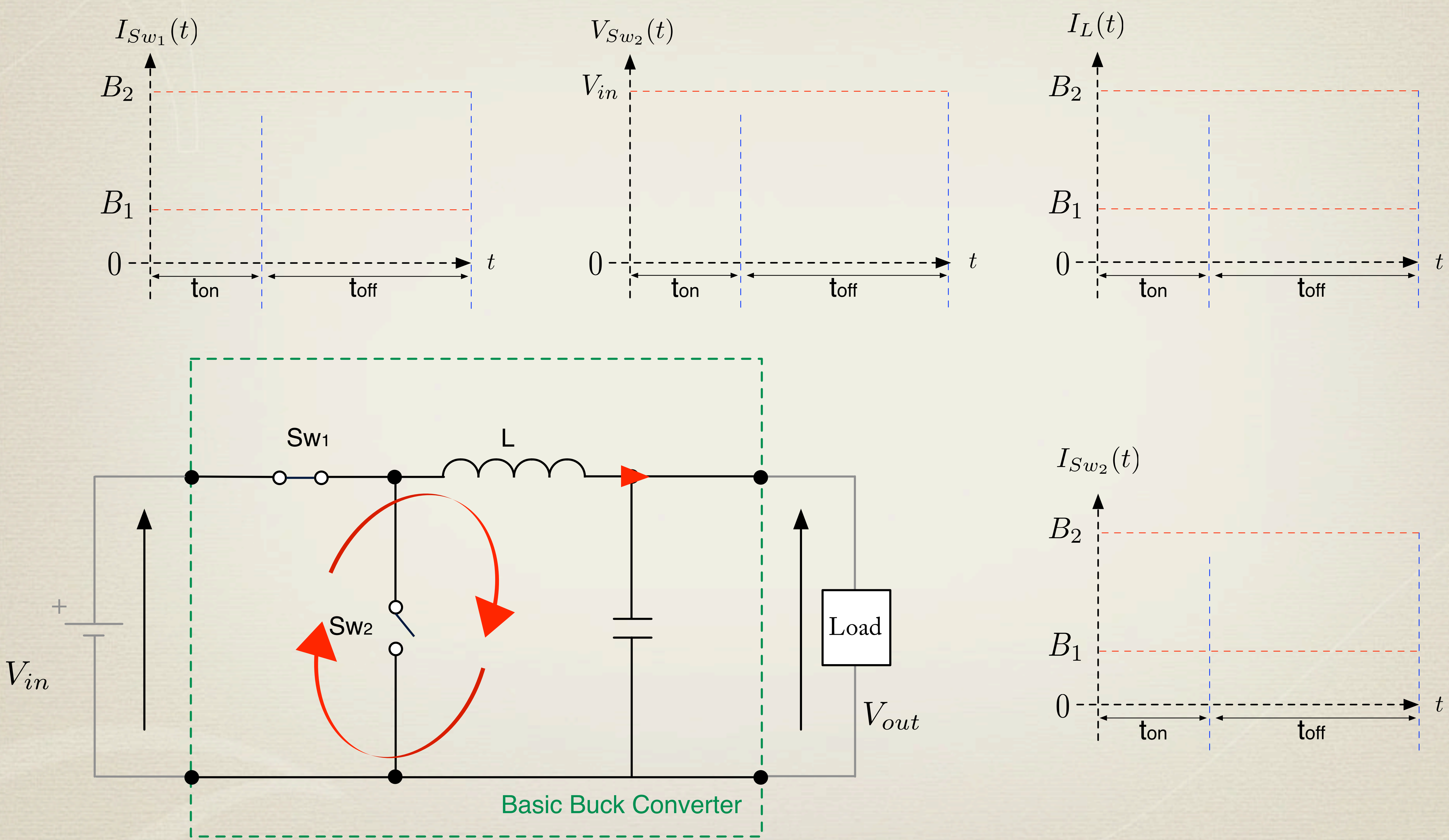

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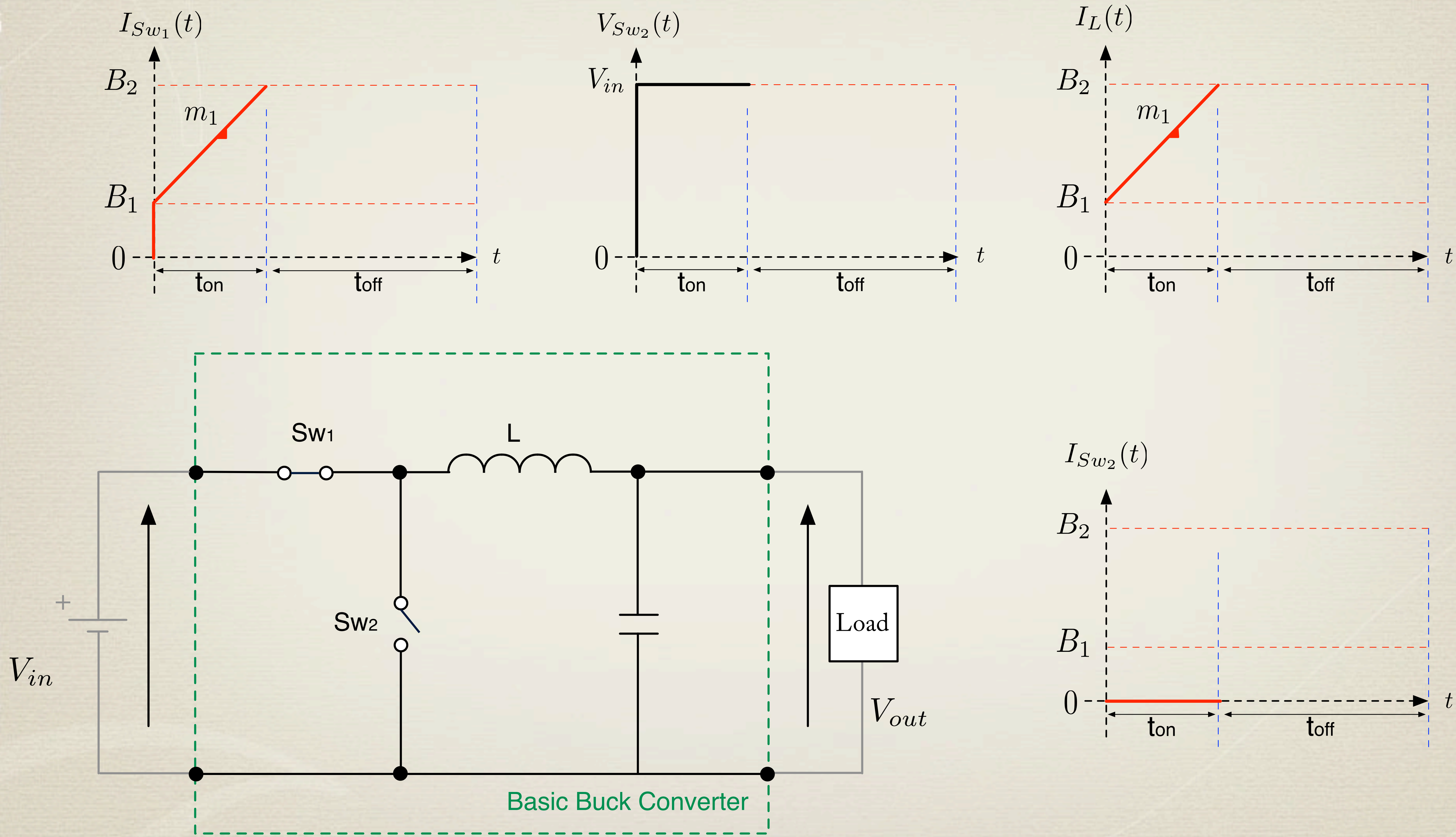

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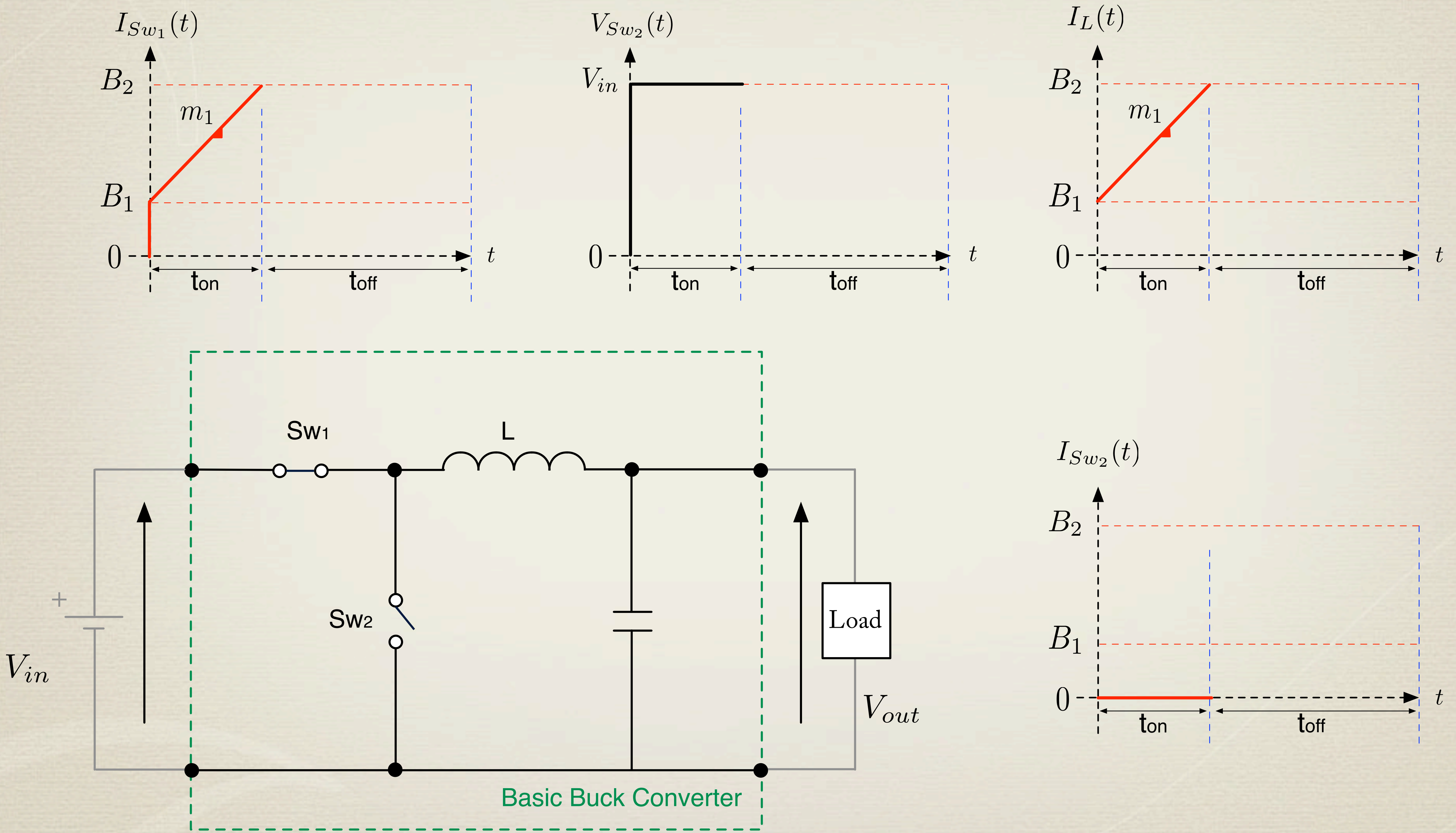

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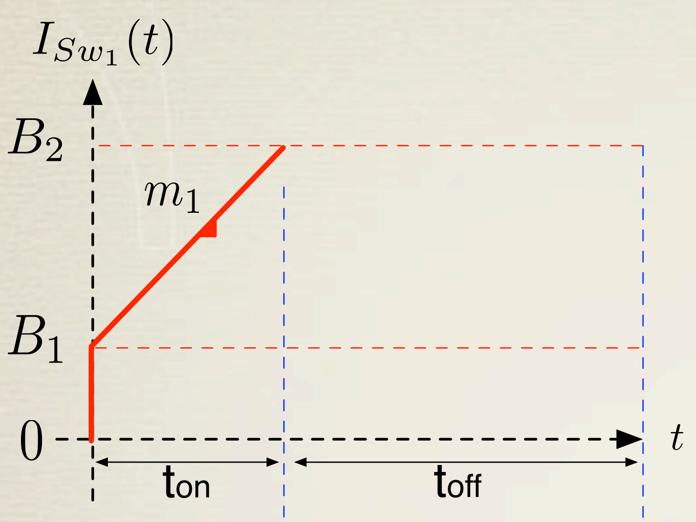

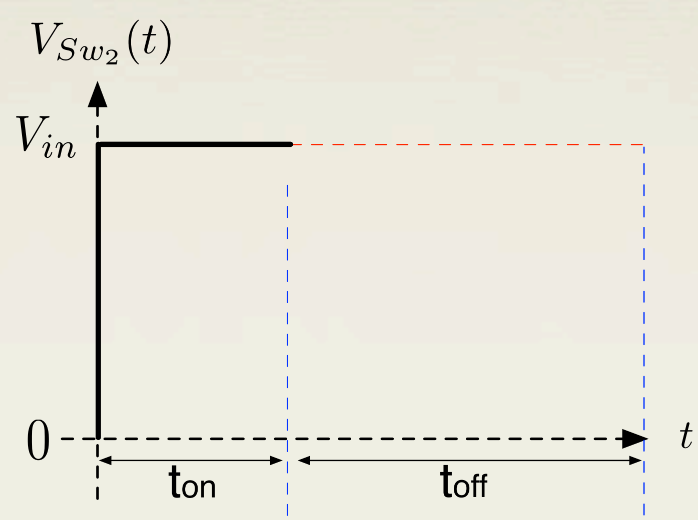

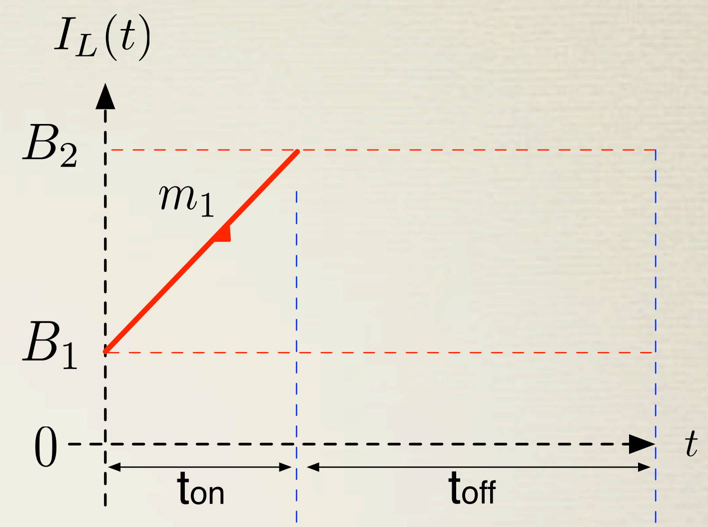

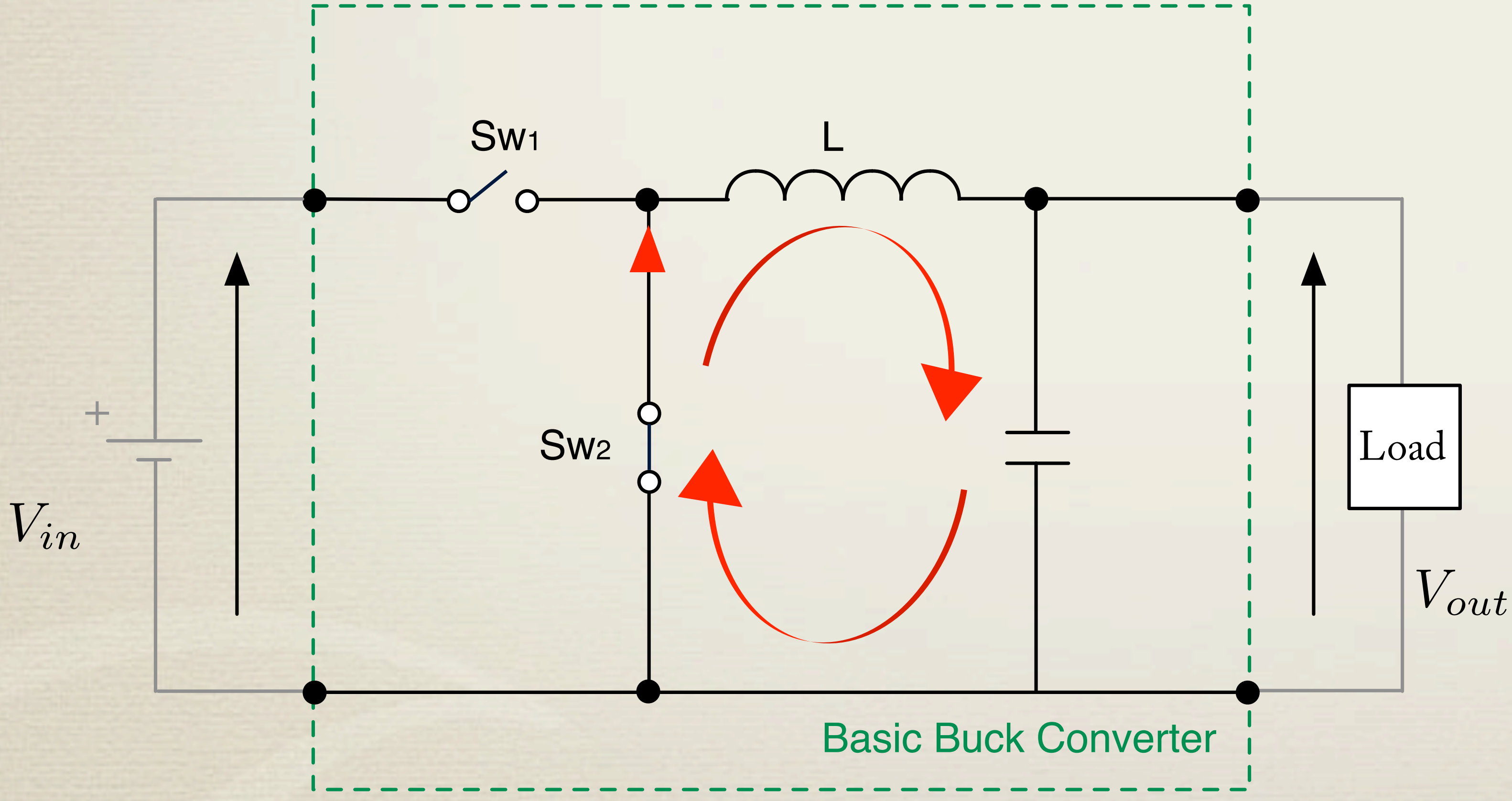

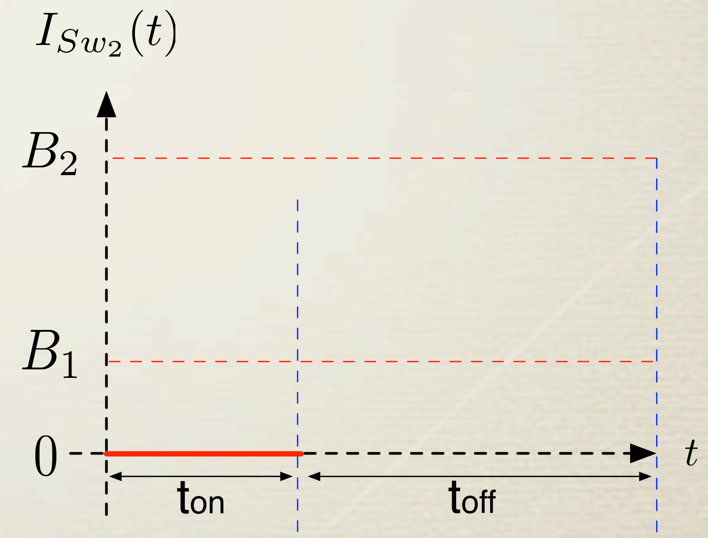

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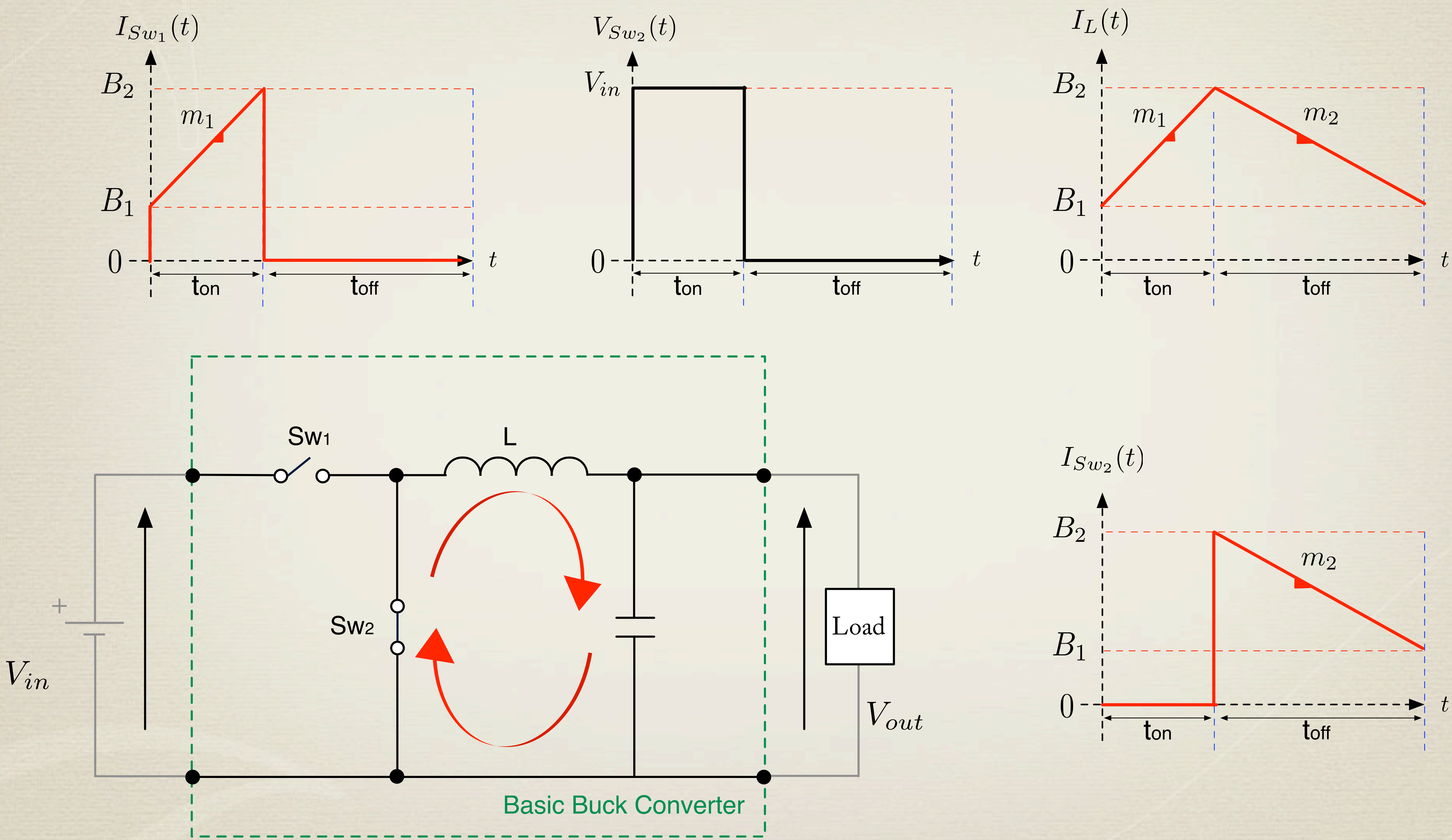

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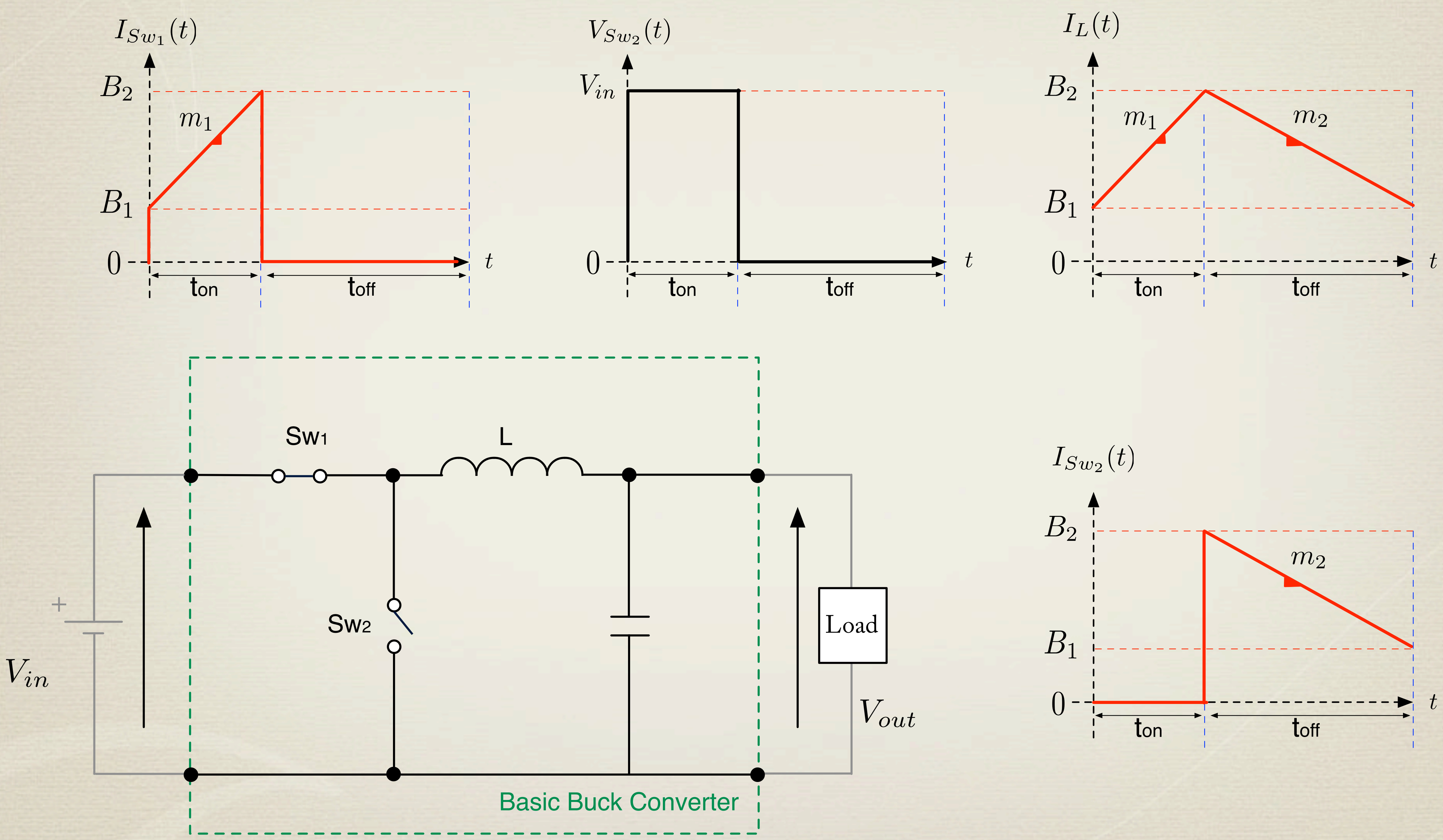

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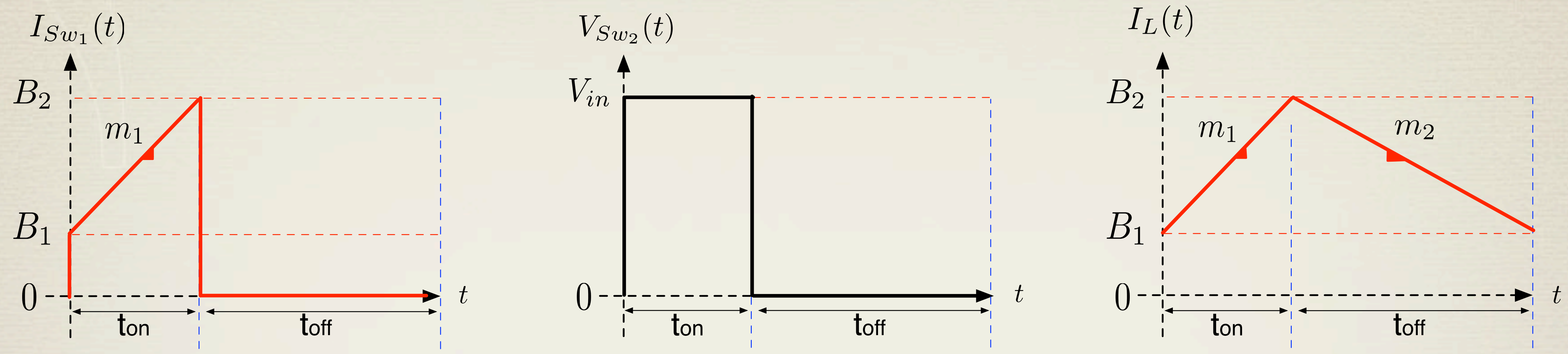

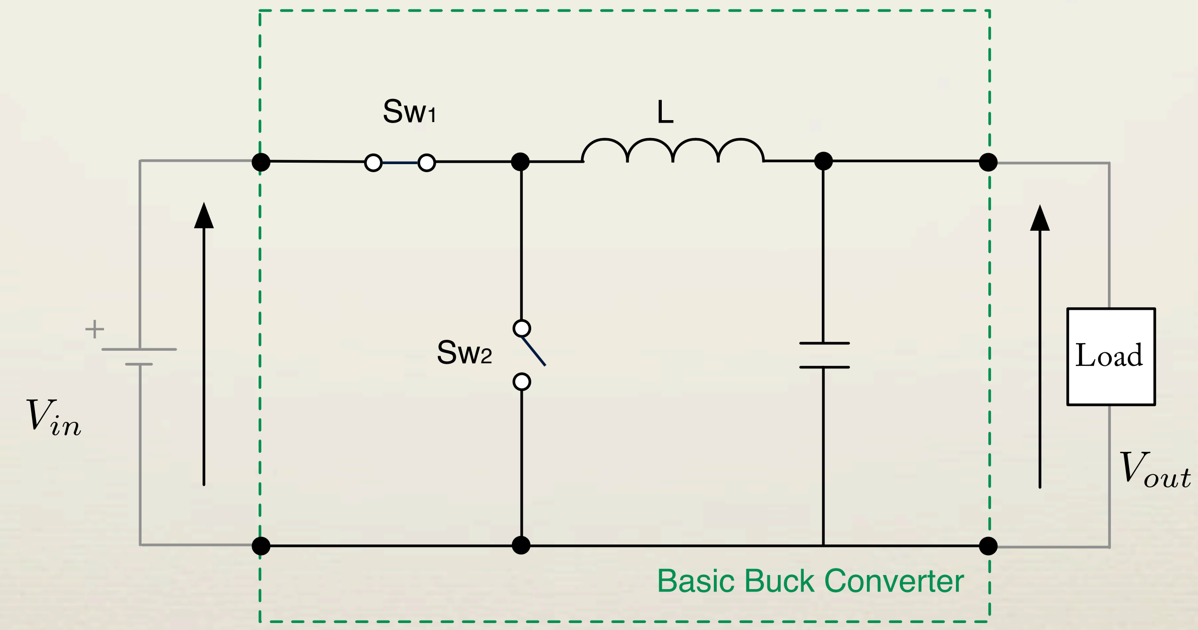

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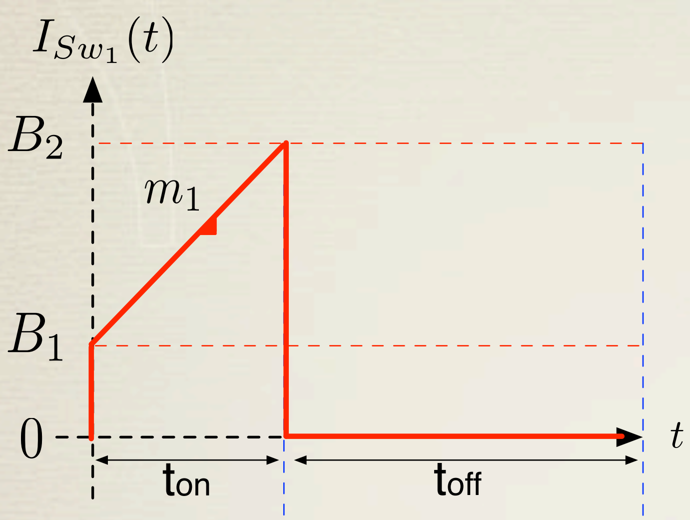

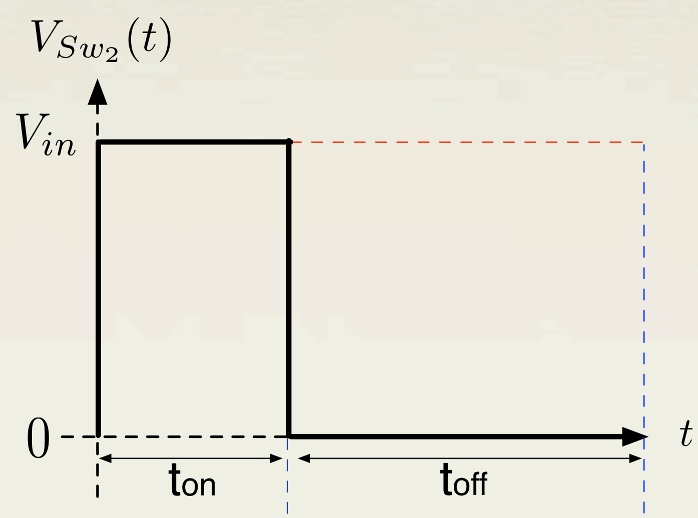

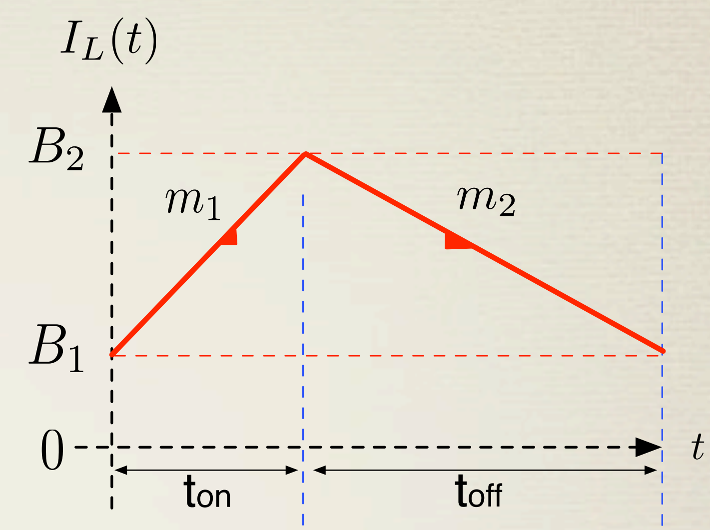

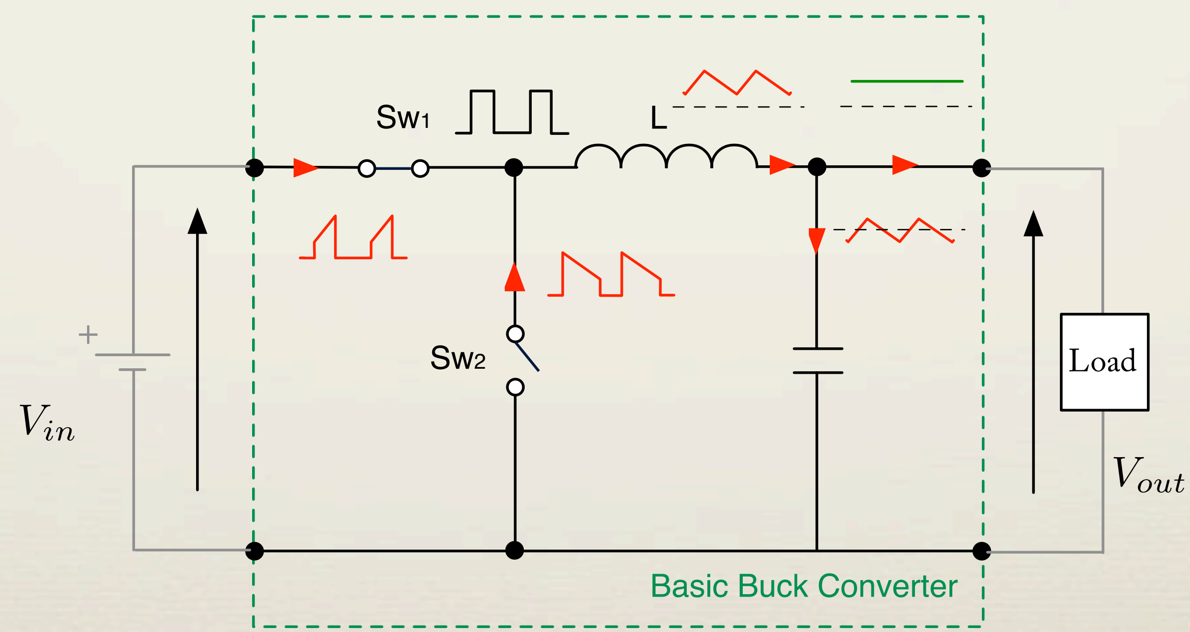

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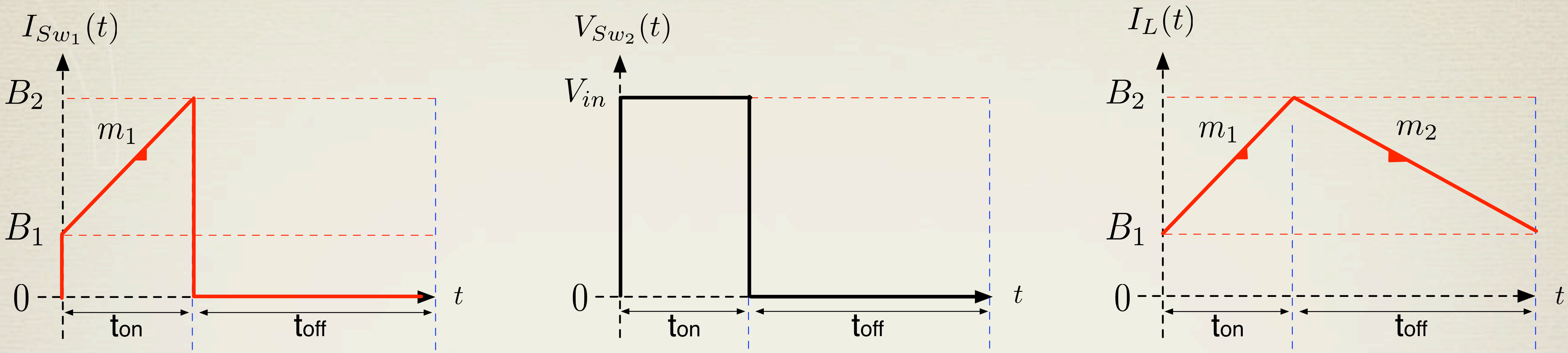
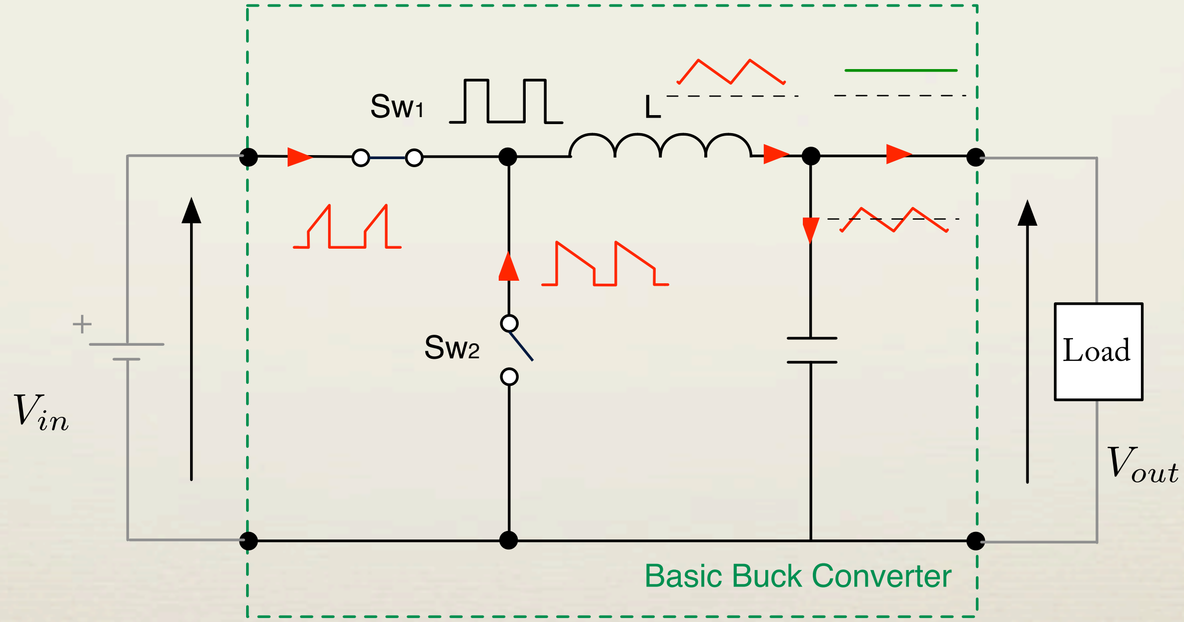


$$V_{out} = \frac{1}{T}\int_0^T V_{Sw_2}(t) \cdot dt$$



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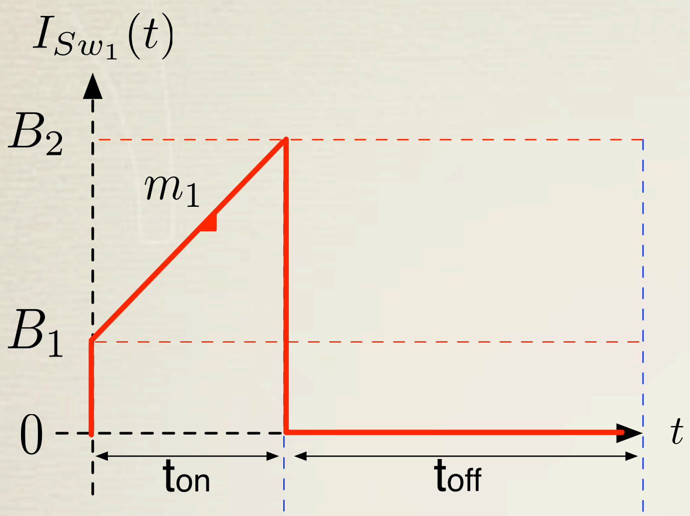

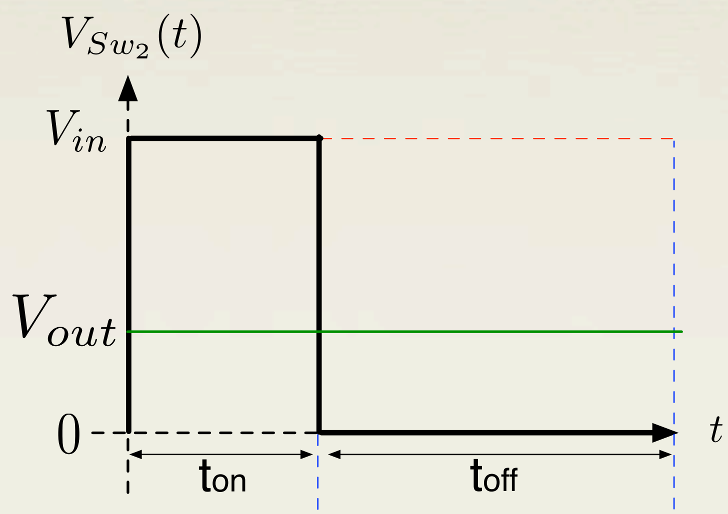

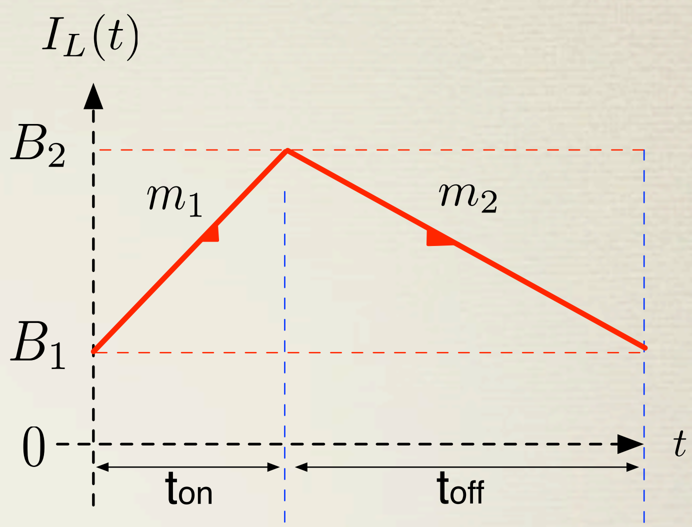

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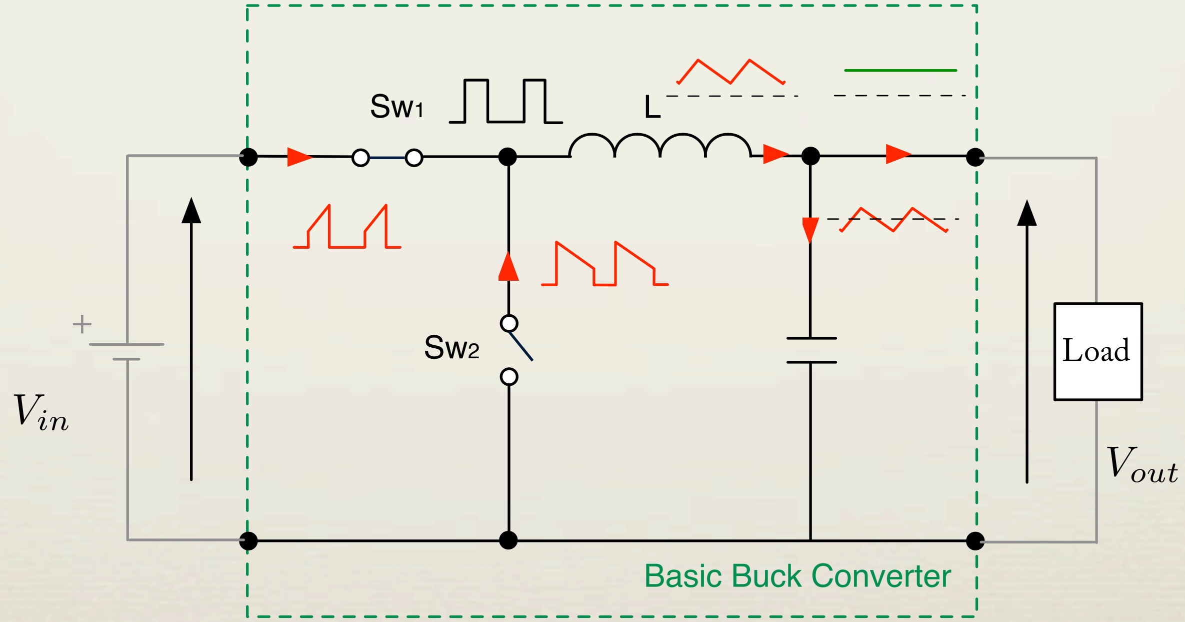

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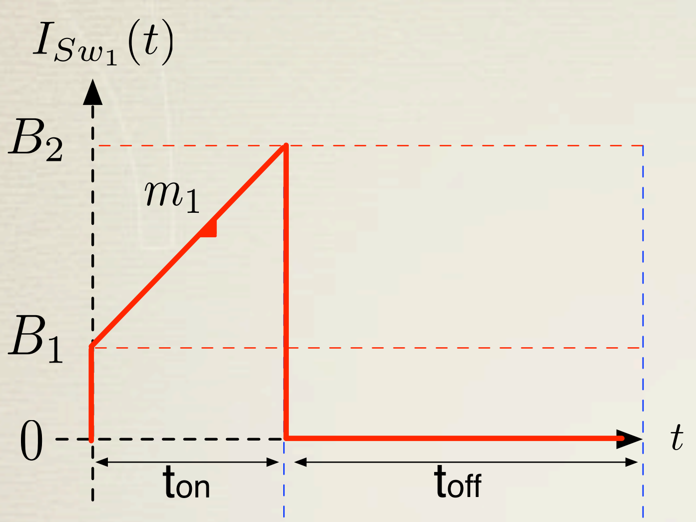
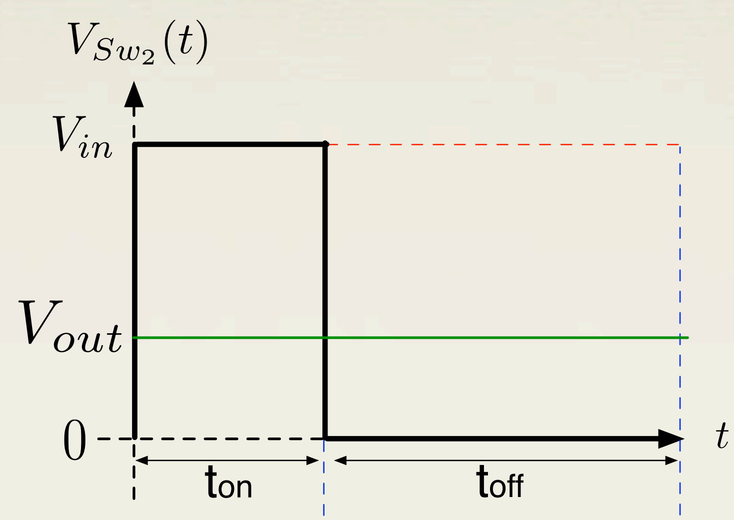
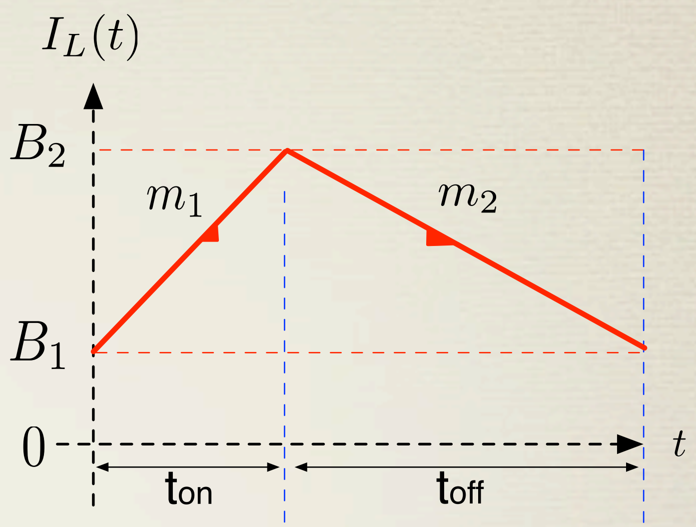
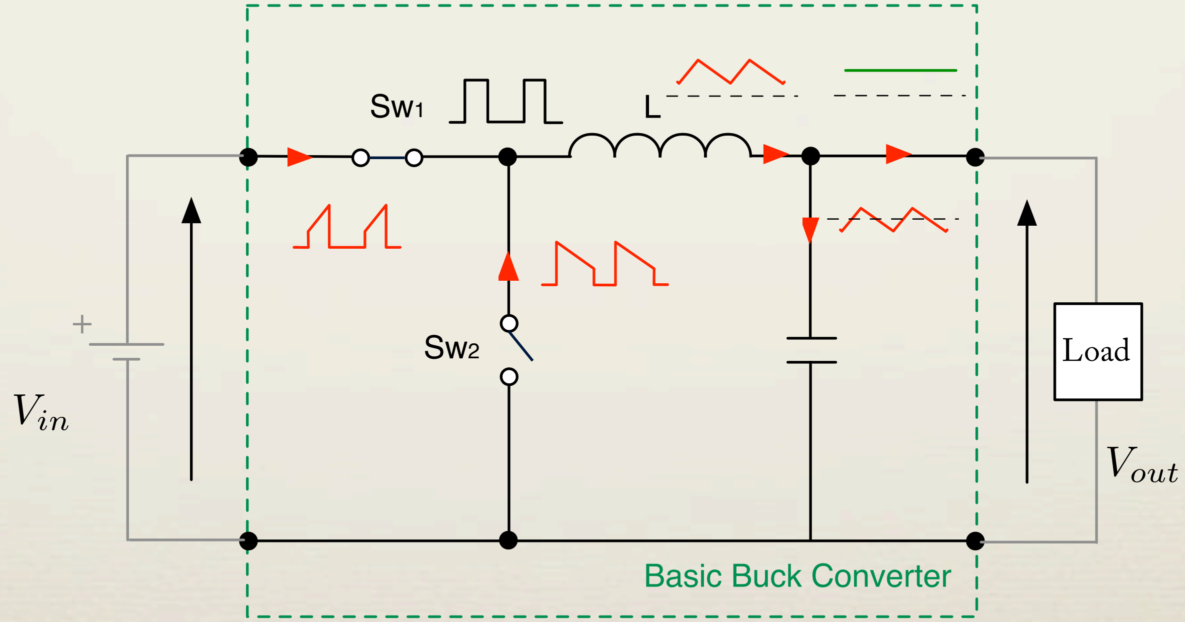






$$V_{out} = \frac{1}{T}\int_0^T V_{Sw_2}(t)\cdot dt \quad \Rightarrow V_{out} = \frac{t_{on}}{T}V_{in} = DV_{in}$$



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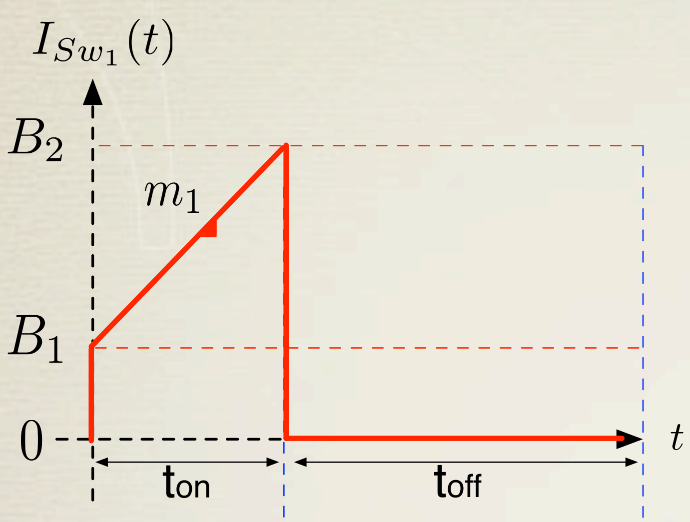

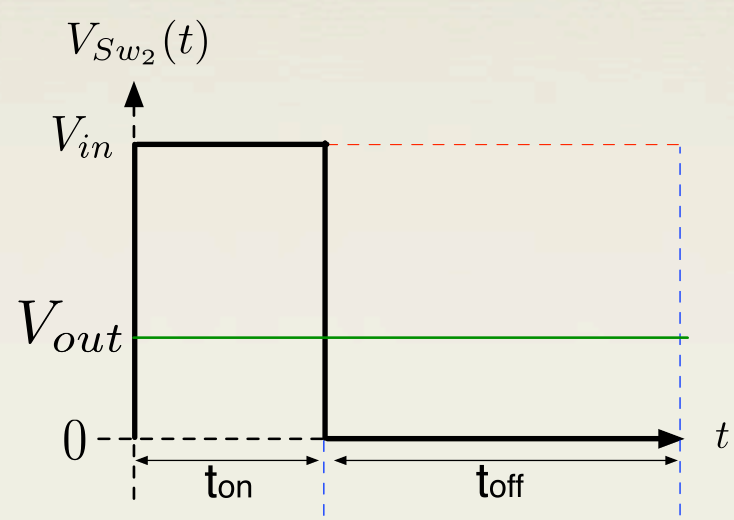

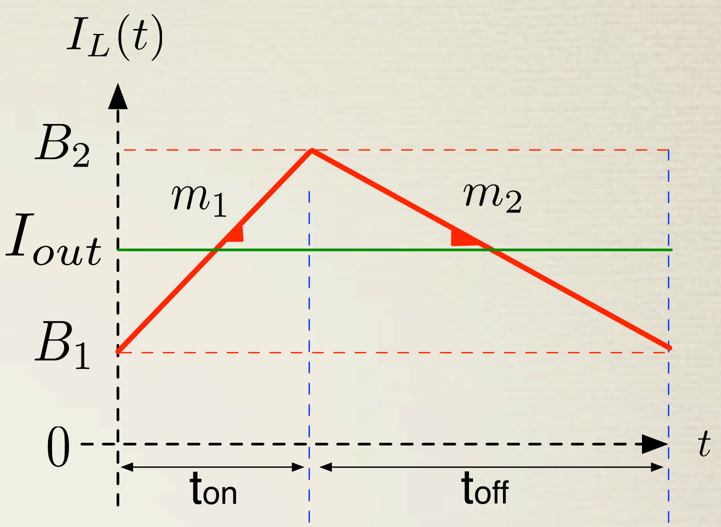

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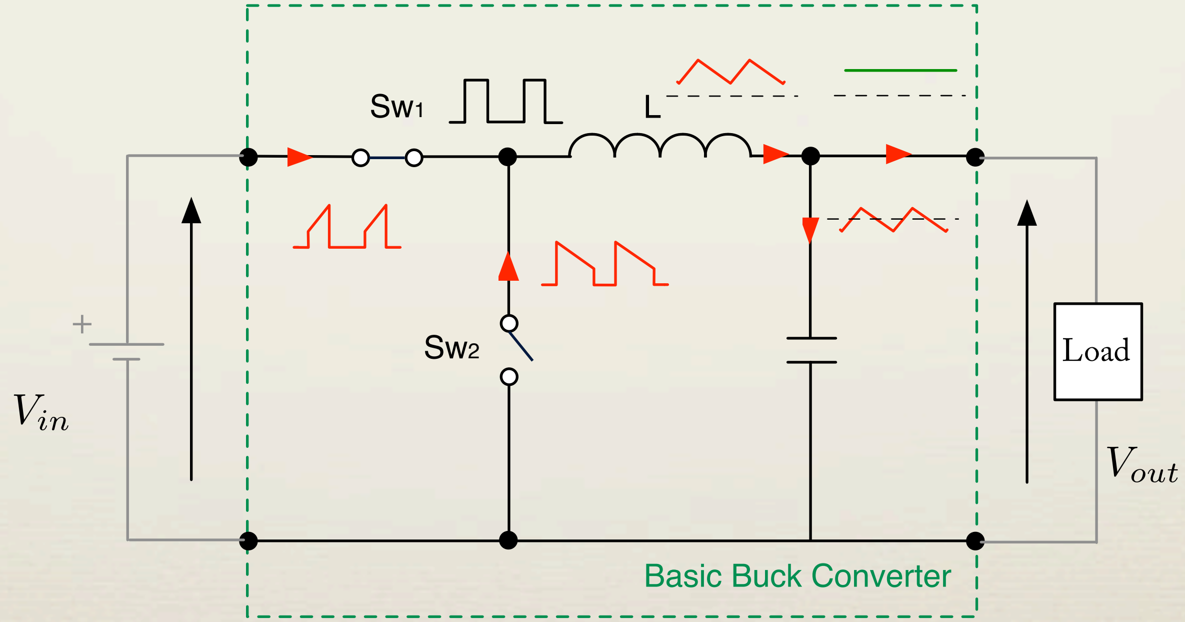

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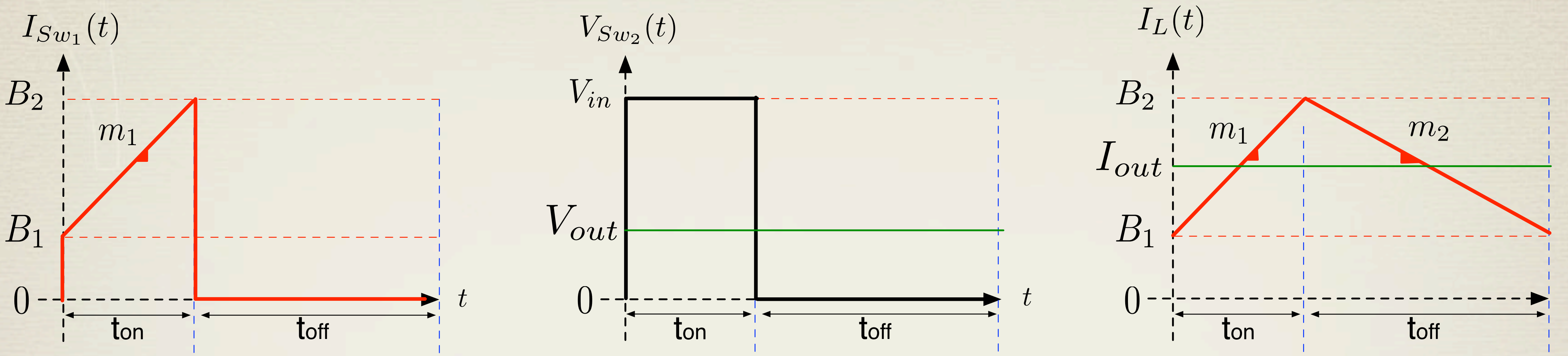

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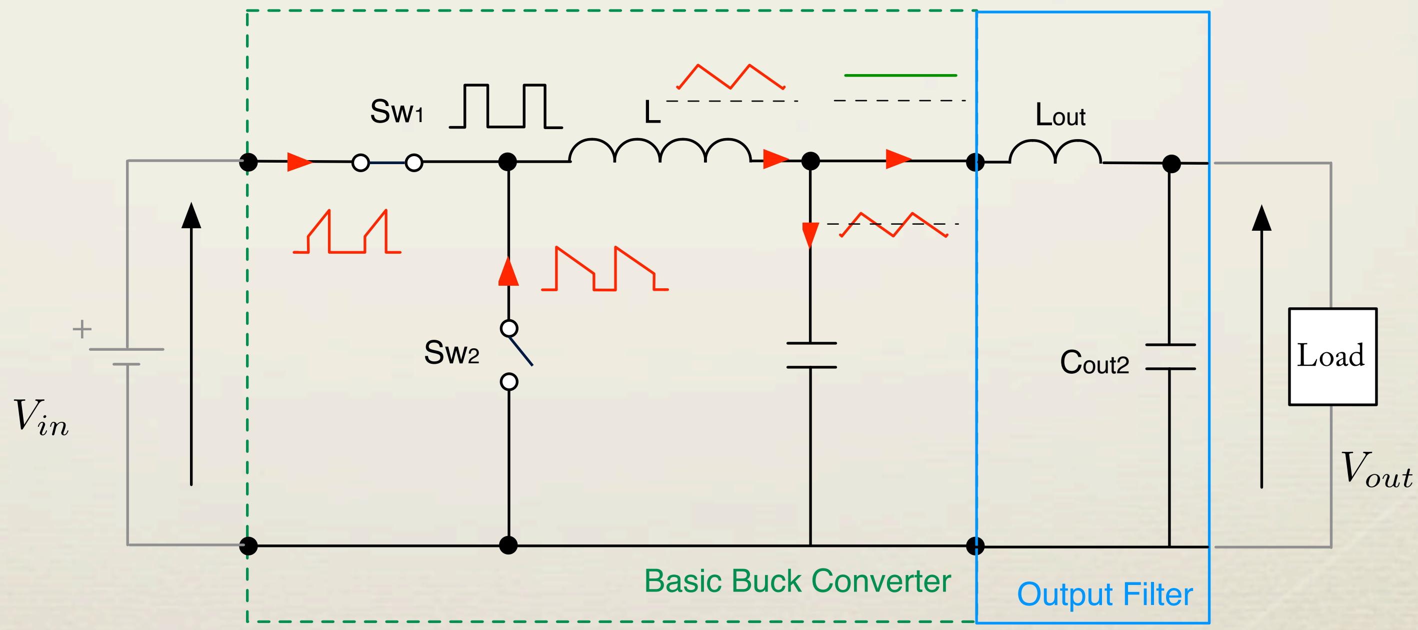

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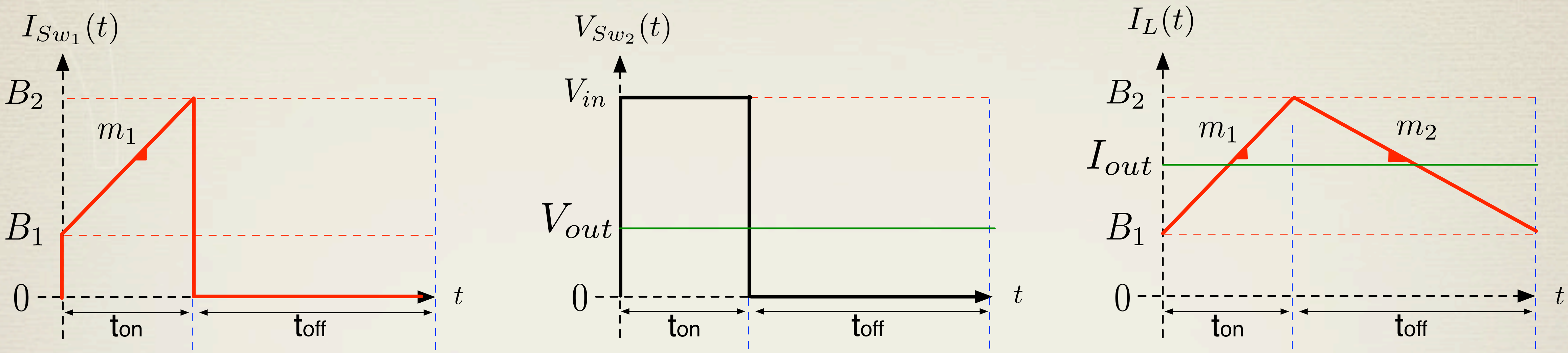

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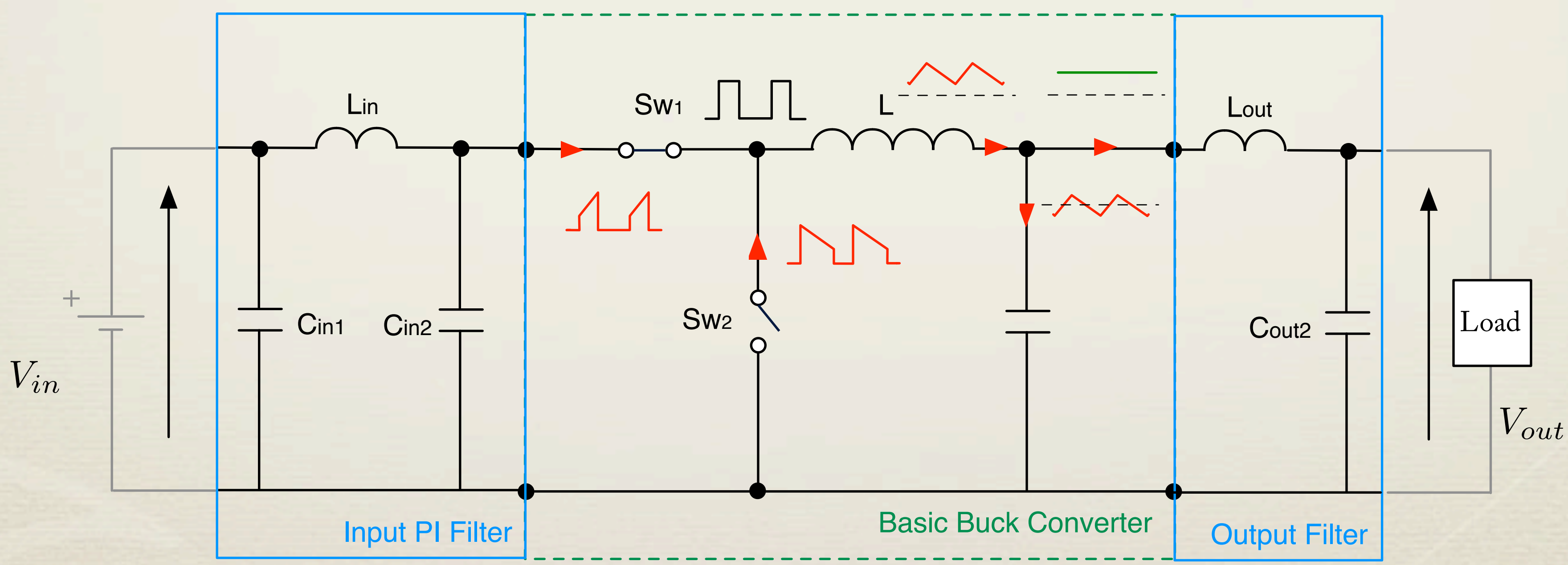

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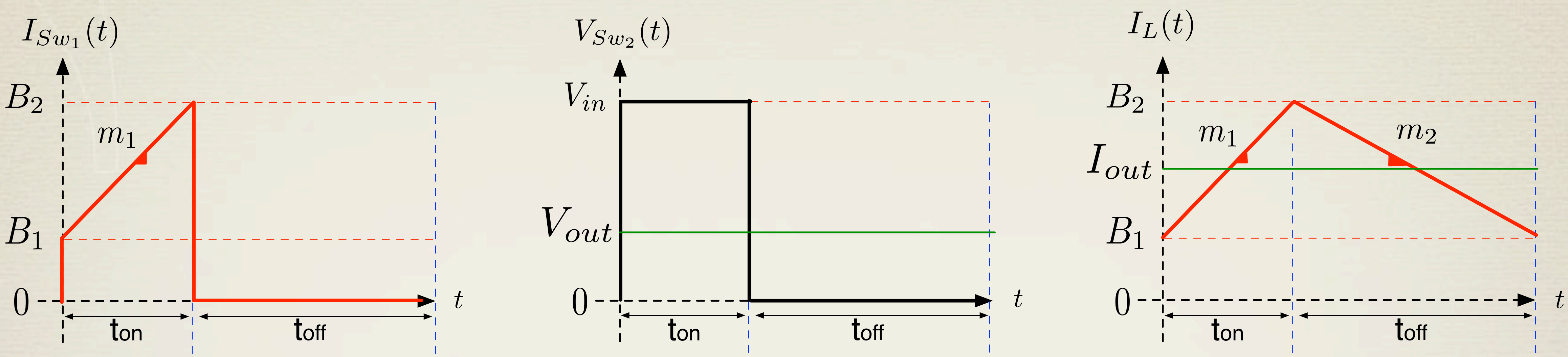

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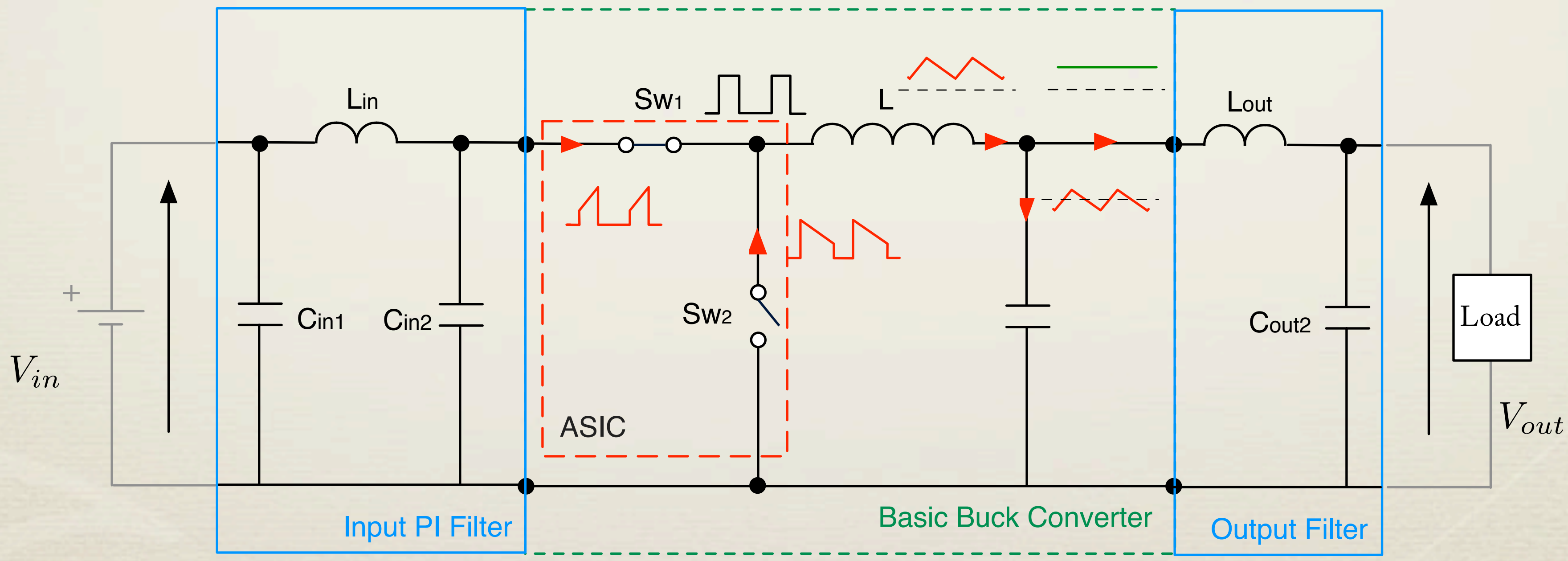

Advantages and constraints

Advantages

- Two switches and low parts count.
- Simple operation mode.
- Input current is significantly reduced.
- Output voltage is regulated close to the load.
- Conversion efficiency is high.
- Reacts fast to load current fluctuations.
- Individual control of the converter (on/off and monitoring).
- Widely used in industry, well known and established technology.

Constraints

- No radiation tolerant devices commercially available.
- Requires a relatively large air core inductor (L).
- Potential sources of electromagnetic noise.
- Non negligible mass.

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DC-DC ASIC Development Radiation tolerance qualification

Requirements for trackers

TID:	> 250 Mrad.
Displacement damage:	> $2.5*10^{15}$ n/cm^2
Single Events:	SEB and SEGR

Technologies qualification

Two vendors pre qualified:	On Semiconductor (AMIS) and IHP.
On Semi:	0.35μ LDMOS fully qualified.
IHP:	0.25μ LDMOS design of high voltage transistors not yet qualified.

ASIC prototypes

AMIS2 fully qualified, efficiency = 75% … 80%.
IHP1 qualified, efficiency > 80%

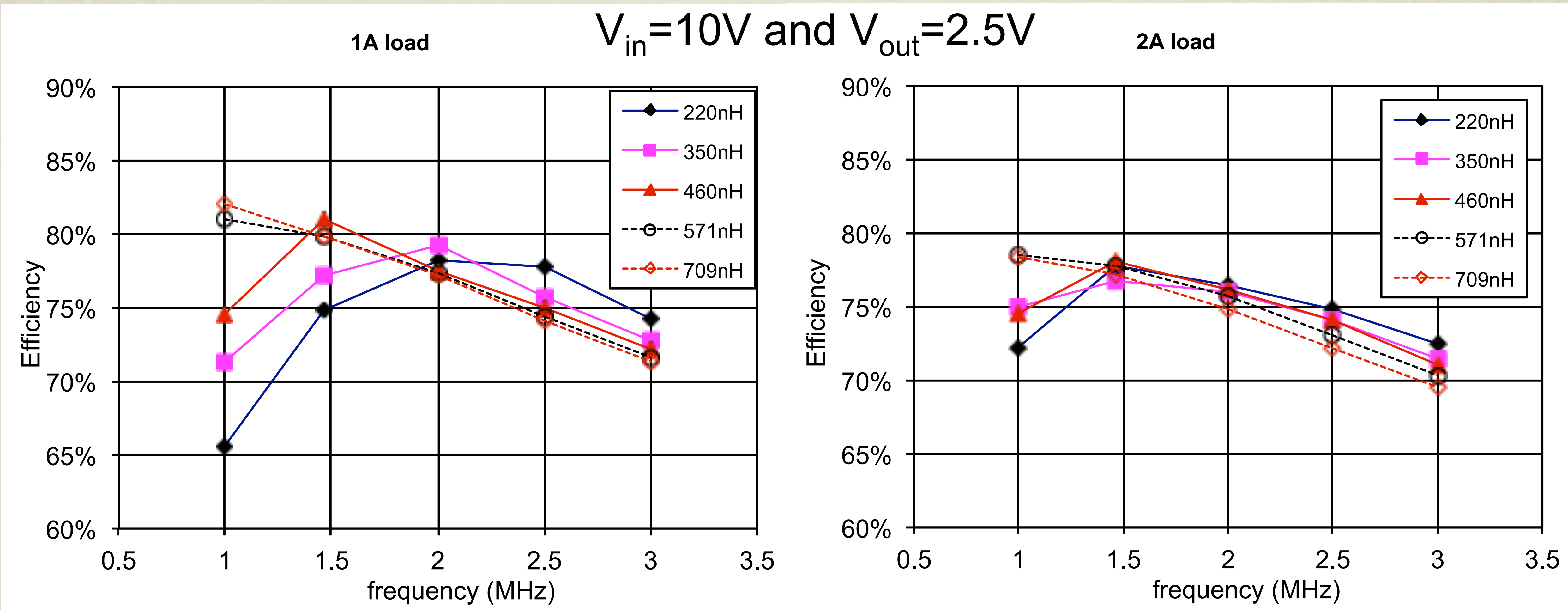
	AMIS2	IHP1	IHP2	AMIS3	AMIS4
Full control loop	✓	✓	✓	✓	✓
Dead times' handling	Fixed	Adaptive (QSW)	Adaptive (QSW and CCM, sharp transition)	Fixed	Adaptive (QSW and CCM, smooth transition)
On-chip regulator(s)	No	No	✓	✓	✓
Soft Start	Simple RC	Simple RC with comparators	Full sequence with comparators	Simple RC	State machine
Over-I protection	No	No	✓	No	✓
Over-T protection	No	No	No	No	✓
Under-V disable	No	No	No	No	✓

↕ Used in system tests (AMIS2)

Due by Mid April 2011 (AMIS3)

Due by end May 2011 (AMIS4)

AMIS2 efficiency



- The package technology contributes significantly the overall efficiency.
  The packaging scheme has been modified in new prototypes to improve this.
- The best efficiency is obtained at 1MHz with high value of inductance (>460nH).
- At 2MHz the efficiency drop is 2-3%, but it allows using a smaller inductor (220nH), helpful for limiting the total weight of the converter.

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DCDC plug-in modules

- Three DCDC plug-in modules Available:
  - One based on a radiation hard ASIC (AMIS2) developed at CERN.
  - Two based on the commercial chip LT3605 from Linear Technology
- PCB design based on guidelines presented at TWEPP10.

  (C.Fuentes et al: Study and methodology for decreasing noise emissions of DC-DC converters through PCB layout)

  http://indico.cern.ch/contributionDisplay.py?sessionId=18&contribId=199&confId=83060
- Electrical Properties:

  -Nominal Input Voltage: 10V (stands up to 15V)

  -Power rated for ABCN25 hybrids: 5A at 2.5V.

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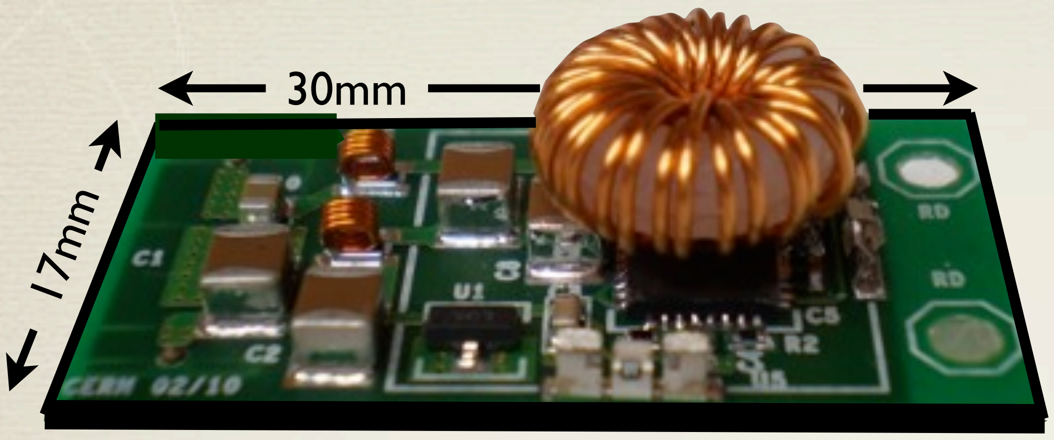
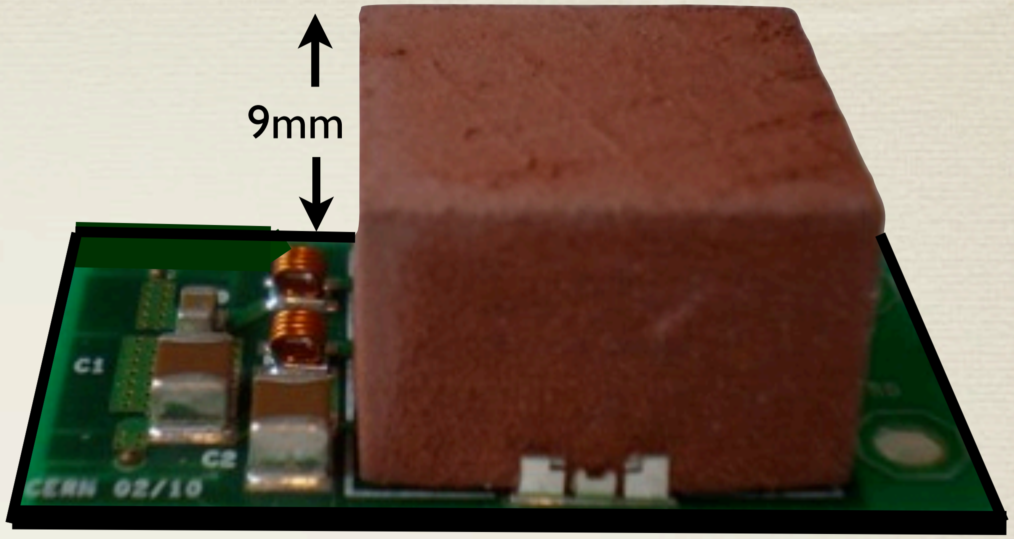
  -Power rated for ABCN25 hybrids: 5A at 2.5V.

The output voltage can be adjusted to the experiment needs.

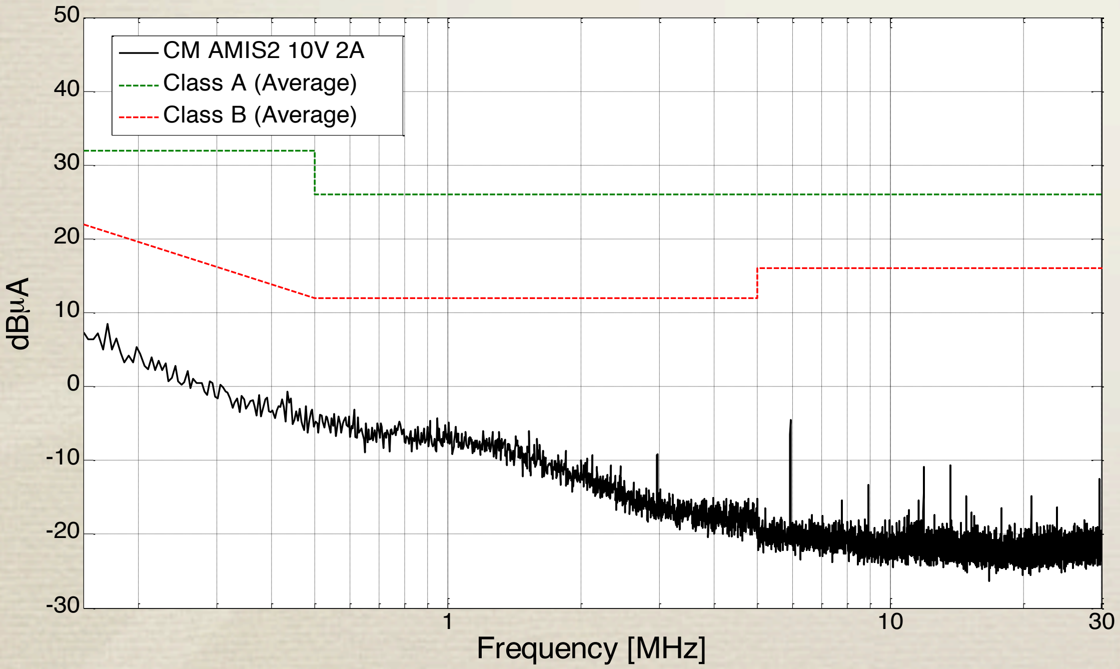
a) AMIS 2

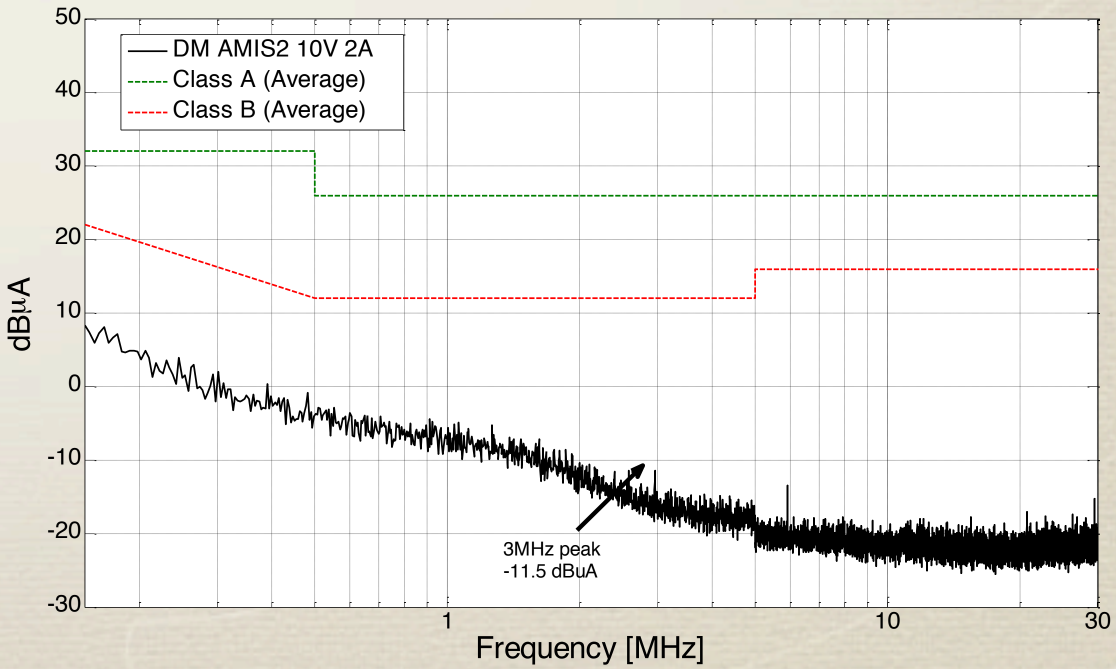




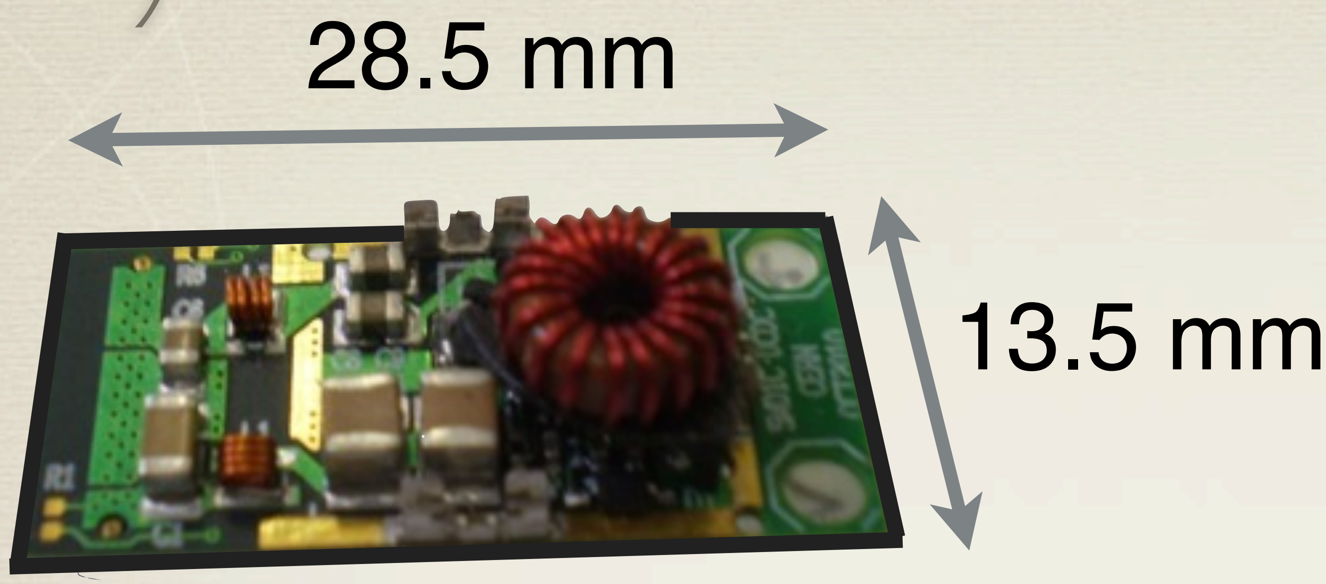
Uses the radiation tolerant AMIS2 ASIC.
Switching at 3 MHz.
Vin = 10 V, Vout = 2.5V.
Output Current = 2A max, tested up to 3A.
Coil = 500 nH.

Low noise optimized layout.
Thermal interface for cooling.
Shielding.
Efficiency between 75% and 80%.



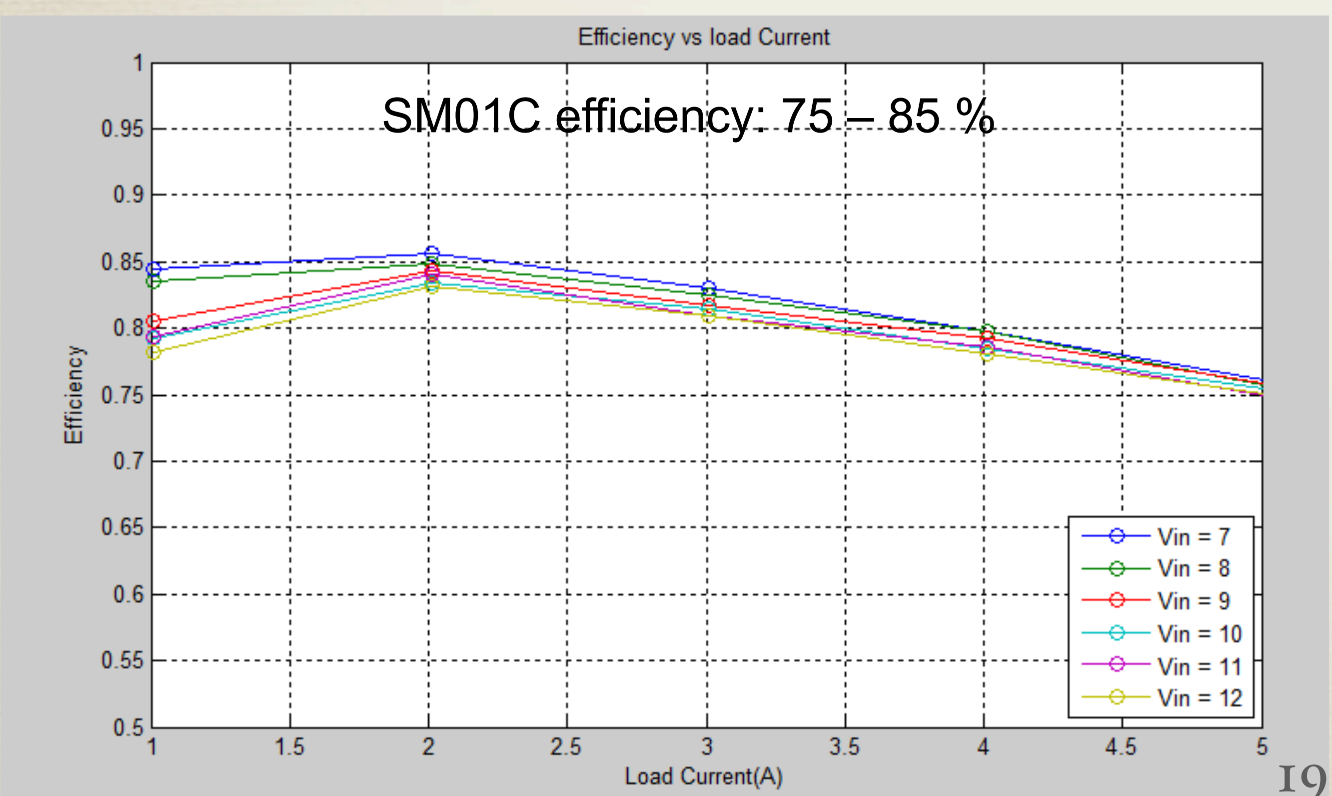


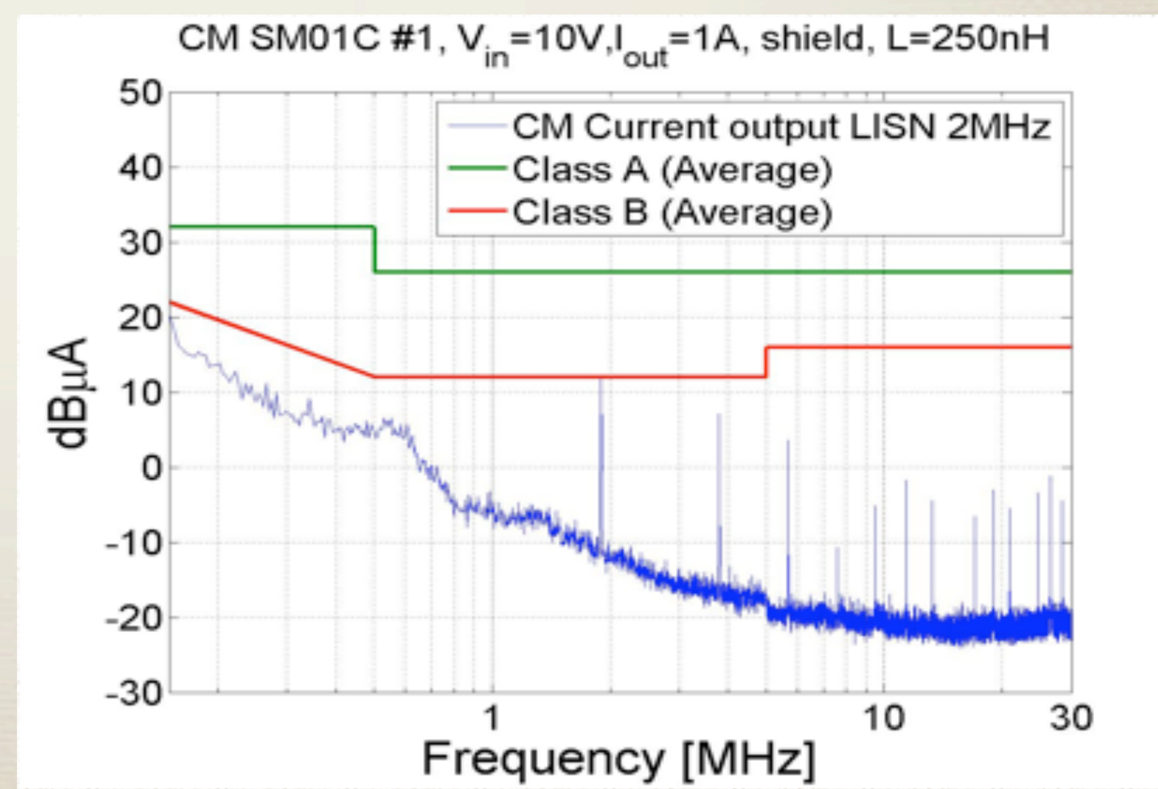
b) SM01c for Super Module



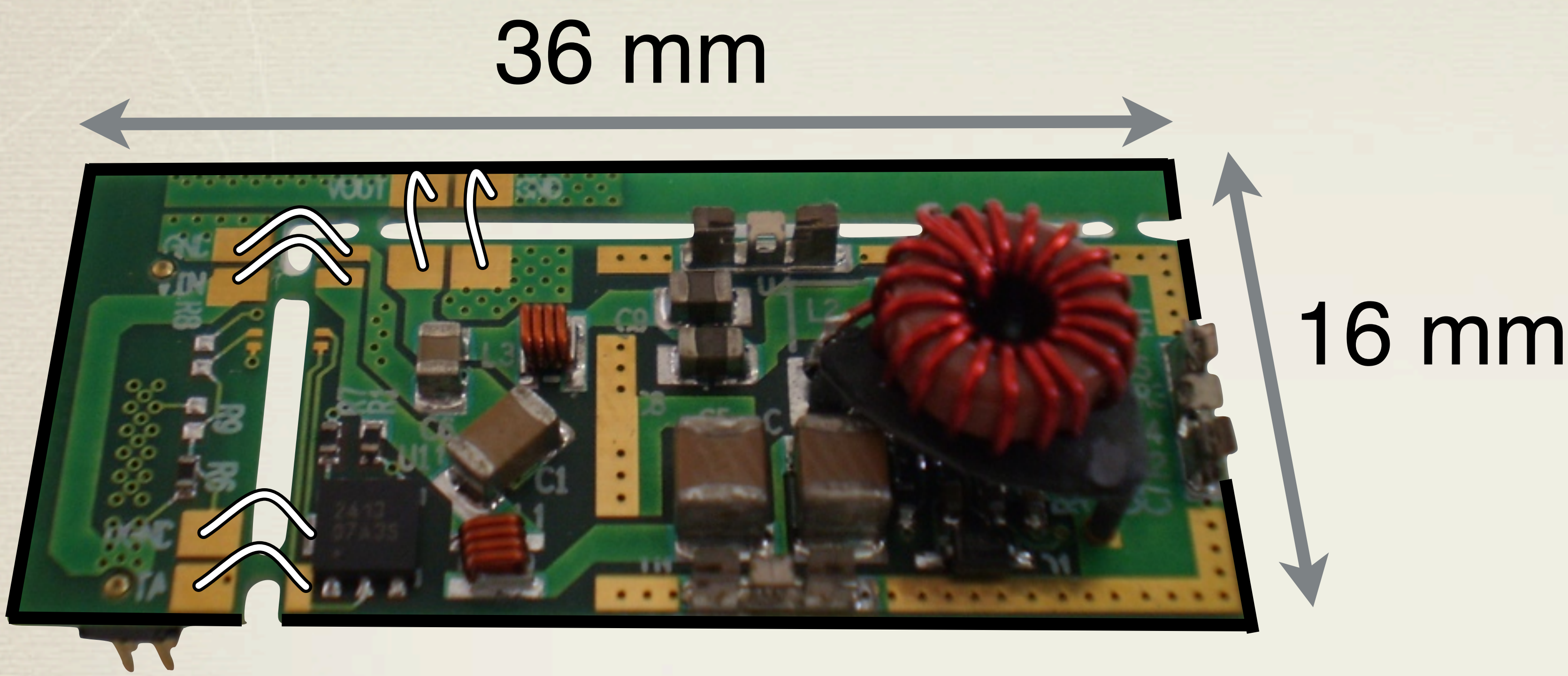
Designed for ATLAS Super Module (UNIGE)

34 SM01 converters have been produced, tested and given to UNIGE collaborators.
More prototypes are being manufactured and will be available for other experiments.





c) STV10 for Stavelet

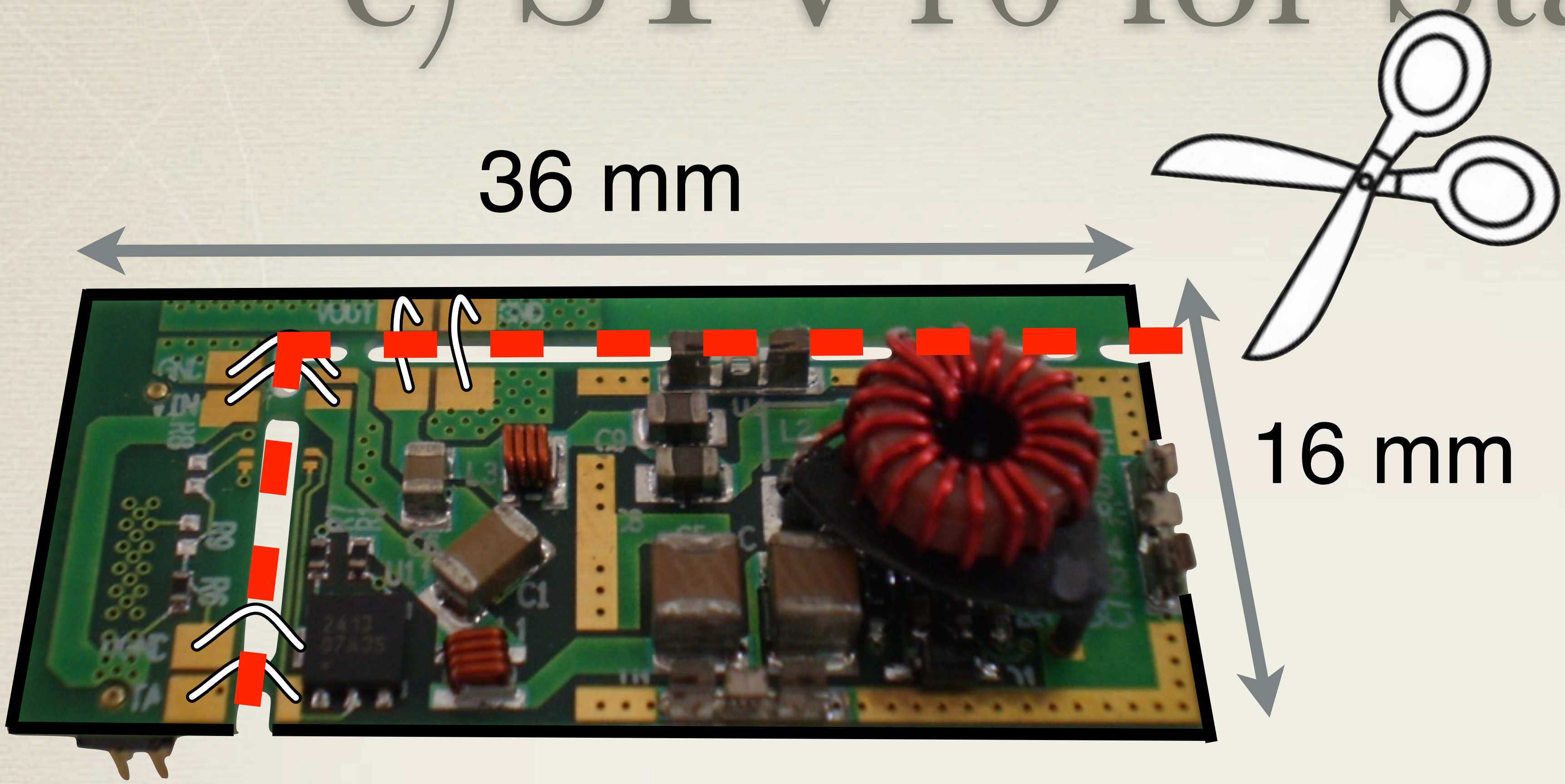


DCDC for
test on LAB

Designed for:
Stavelet ATLAS (Liverpool)

40 STV10 converters are being produced for Liverpool collaborators

c) STV10 for Stavelet



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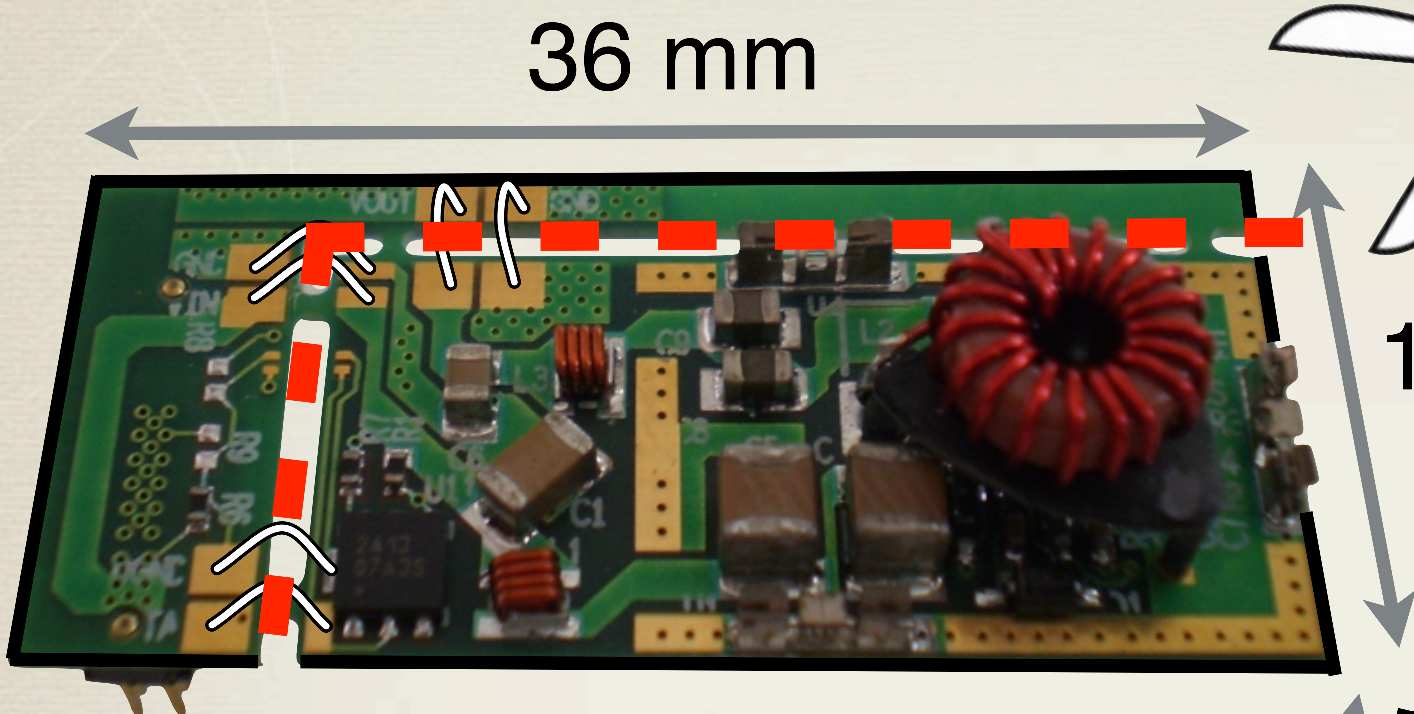

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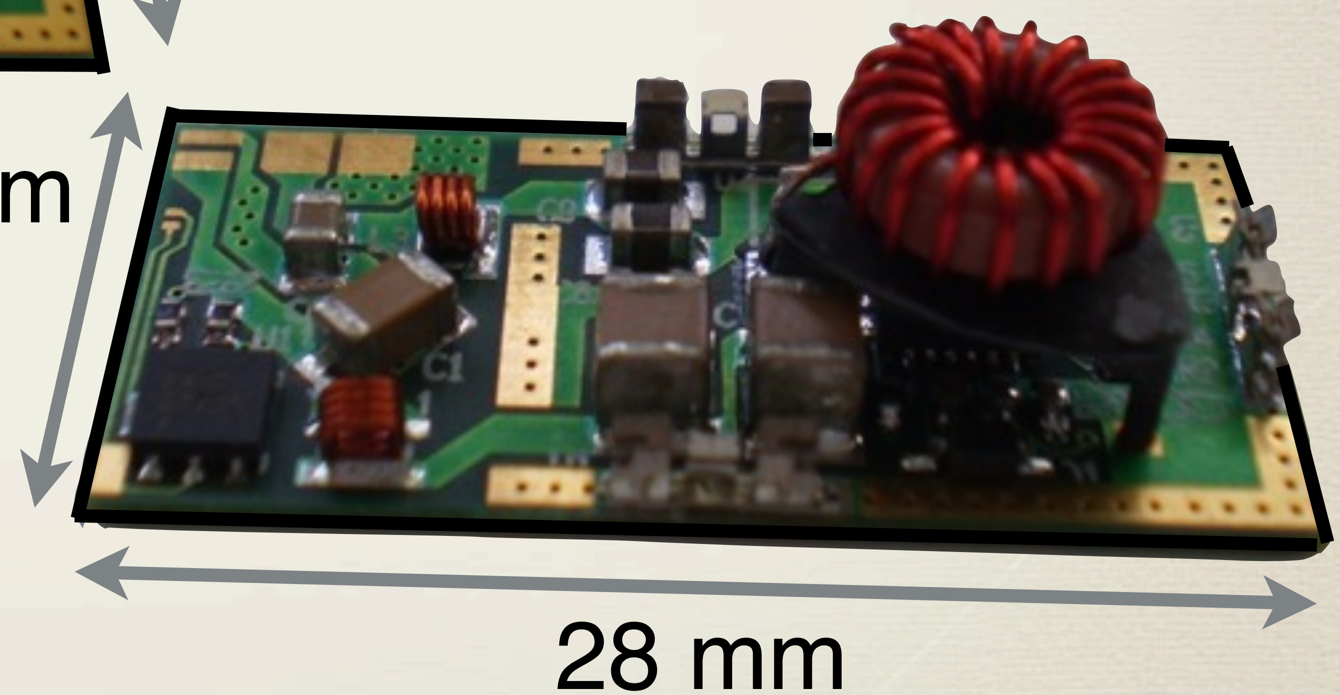

DCDC for Stavelet (bonded)

Designed for:
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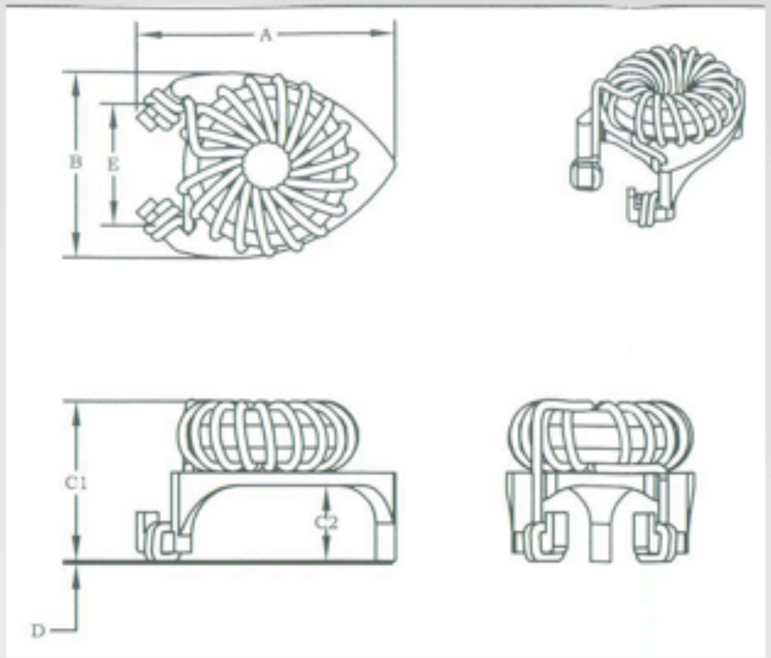
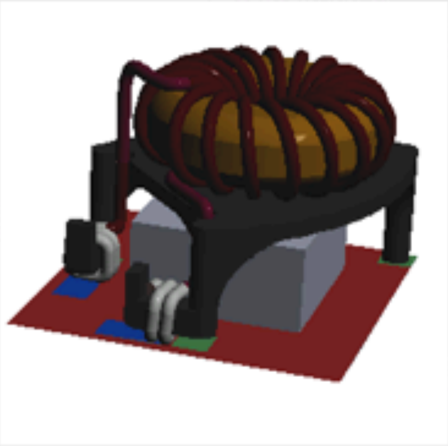
Coil Development

- **Tolerance to B field imposes air core coils**
  - Typical inductance values range up to 700 nH max.
- **Toroidal topology was selected in 2009**
  - Compact geometry.
  - Radiates significantly less magnetic field than other topologies.
  - Air core toroidal inductors not available commercially: custom development for mass production is required.
- **Development with Coilcraft**
  - 220nH/30mΩ air core toroid.
  - Coil mounted on plastic stand-off to fit precisely above the ASIC.
  - Prototypes delivered in 2010.



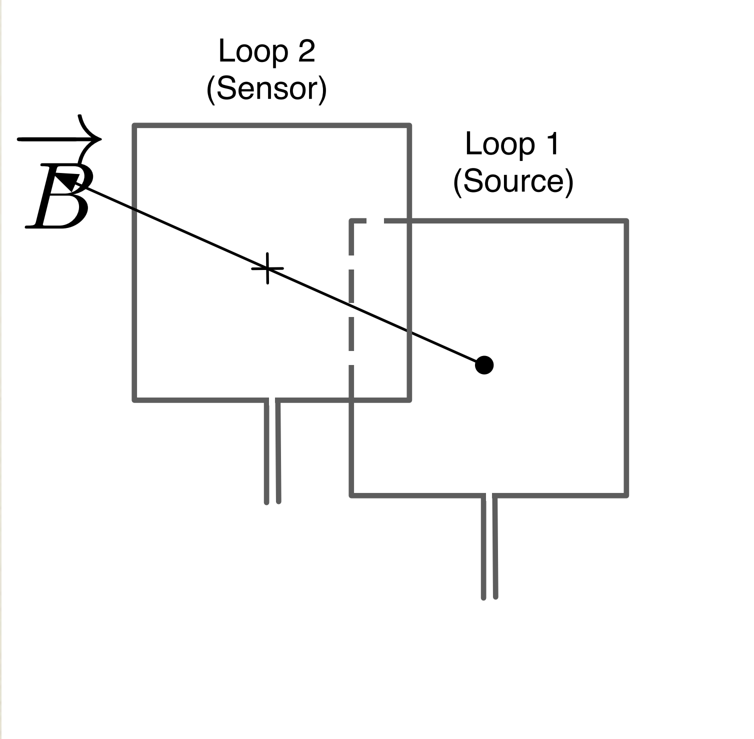


Irradiated with protons at the cern IRRAD1 facility up to 8*10^15 proton/cm^2

Shielding effectiveness

The sensitivity of FE systems to magnetic field yields to studies of how to improve B-field shield effectiveness. As well, a way to measure their effectiveness for comparison purpose must be defined.

Top Side View



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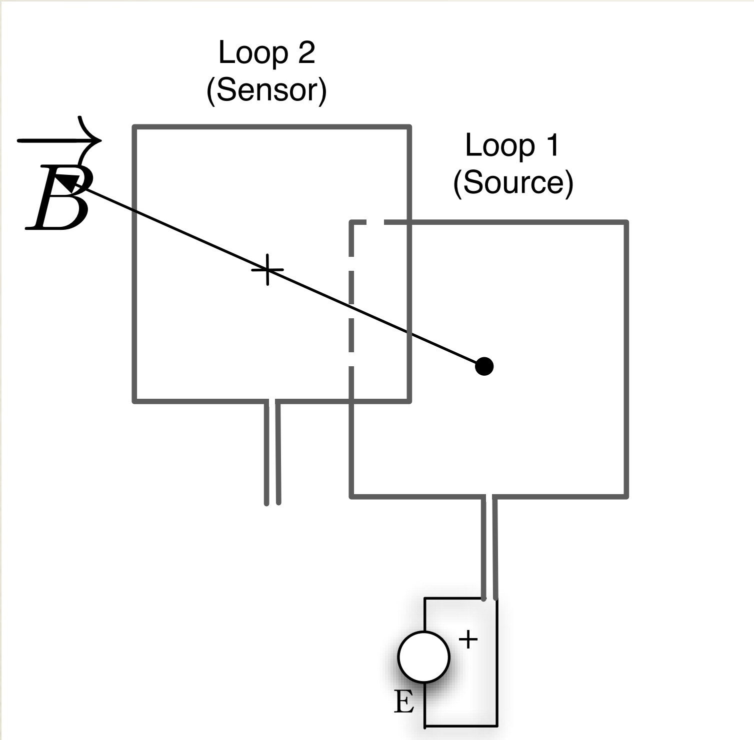

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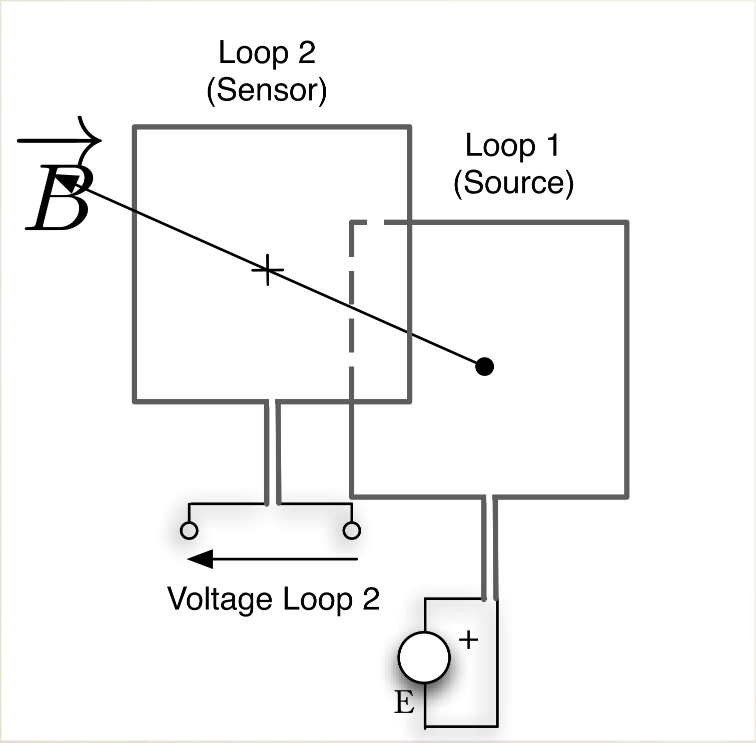

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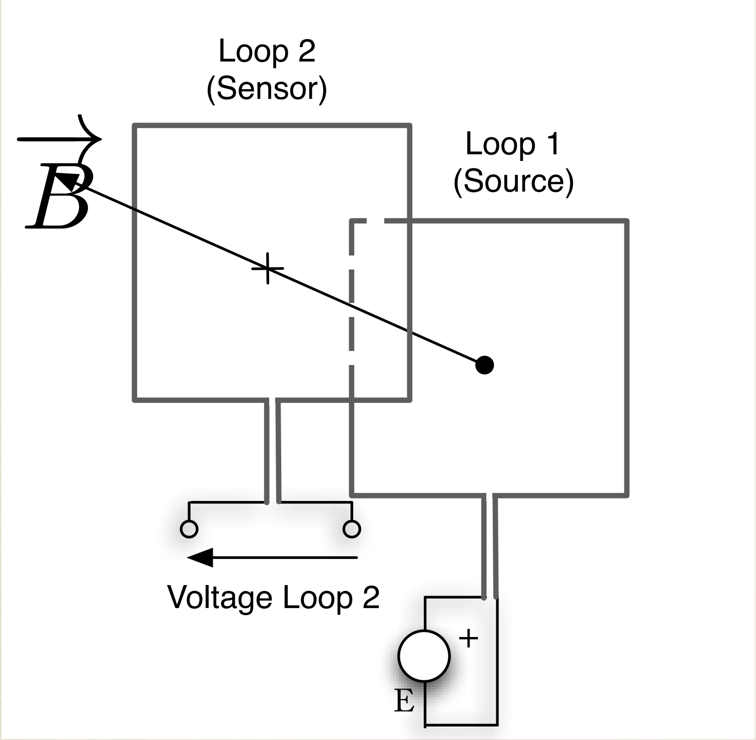
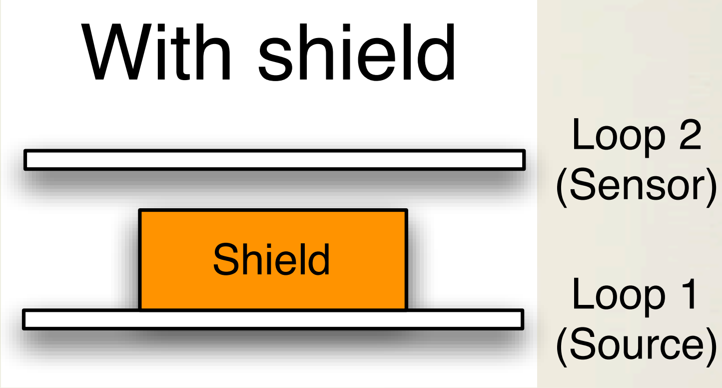


Front View



Shielding effectiveness

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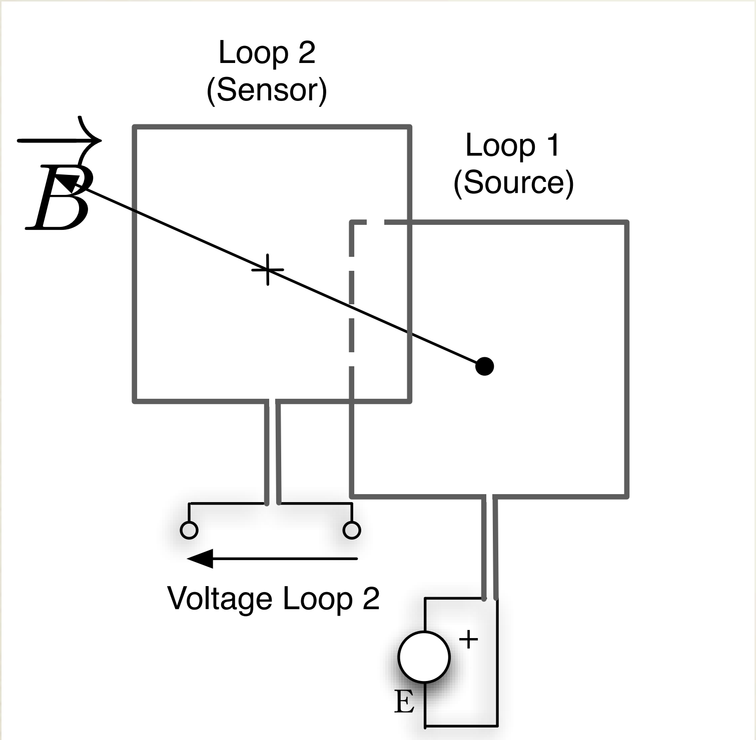
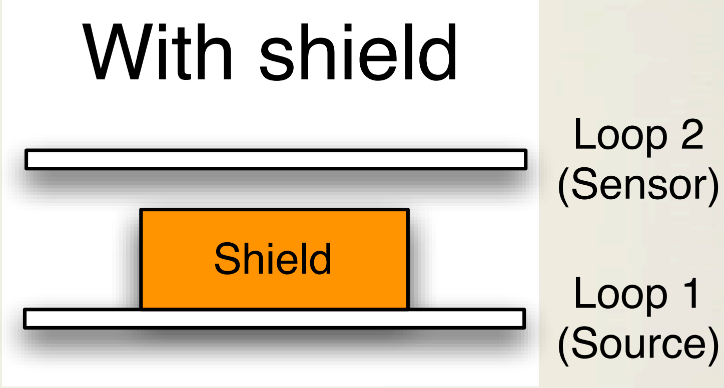
Top Side View

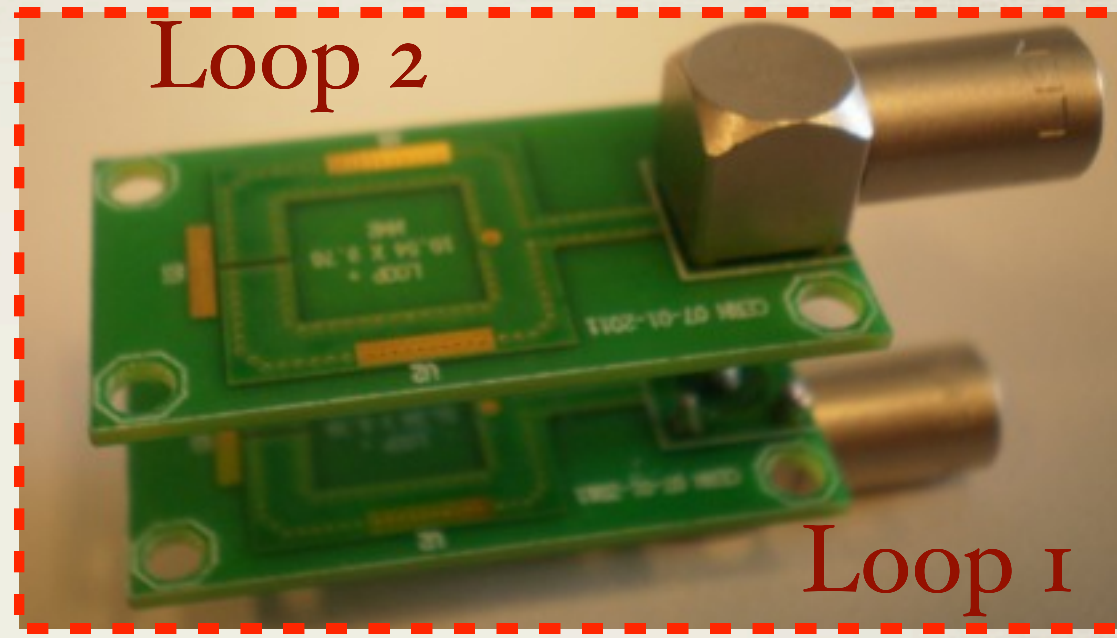


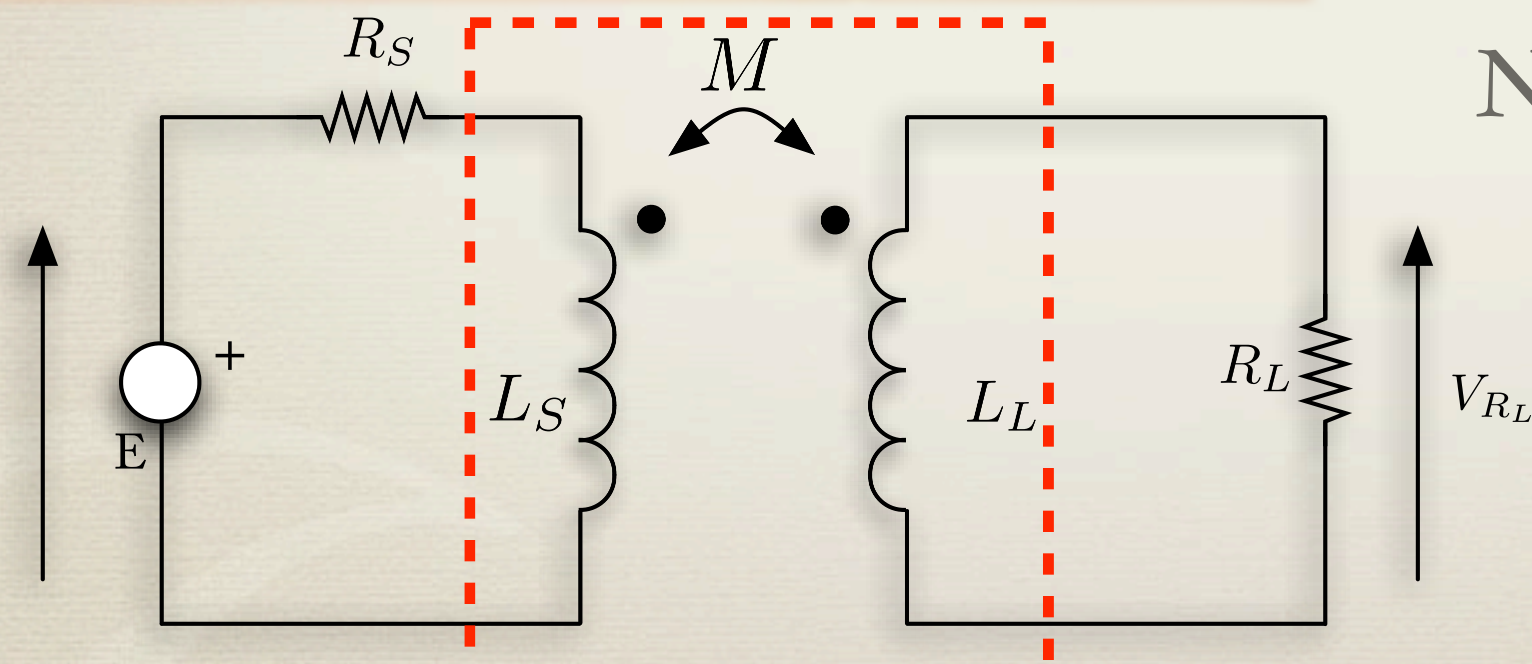
Front View



$$\text{Shielding Effectiveness} = \frac{\text{Voltage Loop 2 without shield}}{\text{Voltage Loop 2 with shield}}$$

Shielding effectiveness

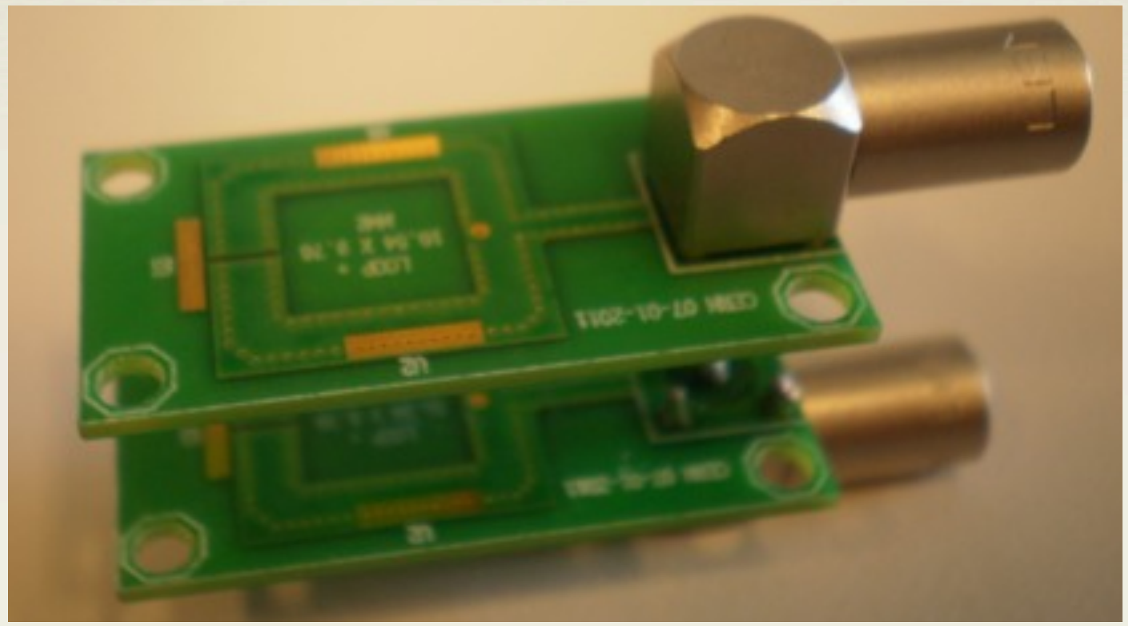




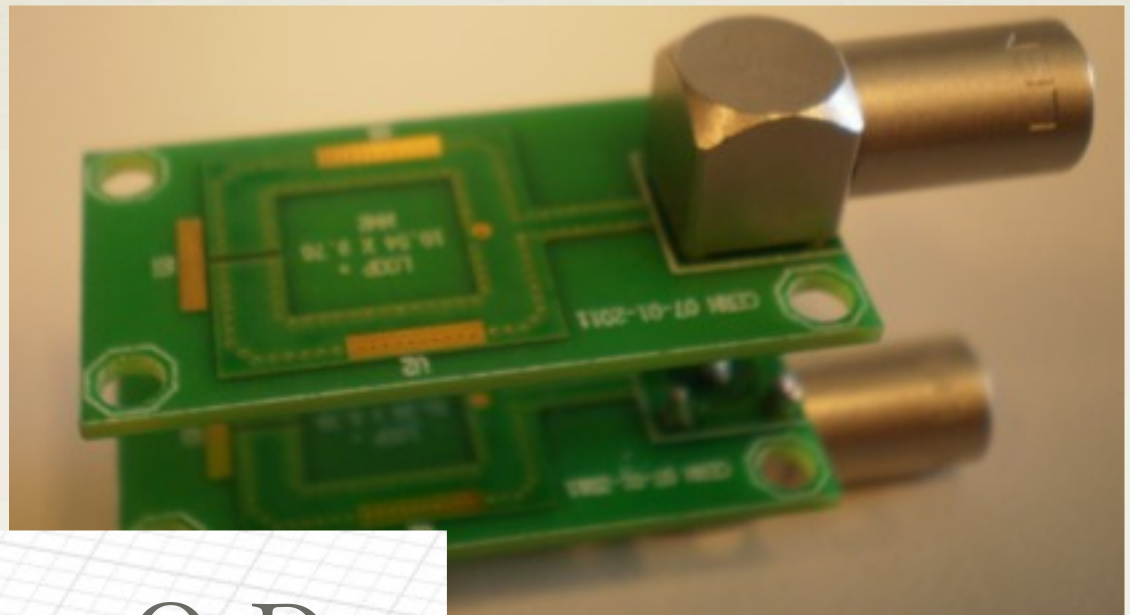
Network Analyzer output

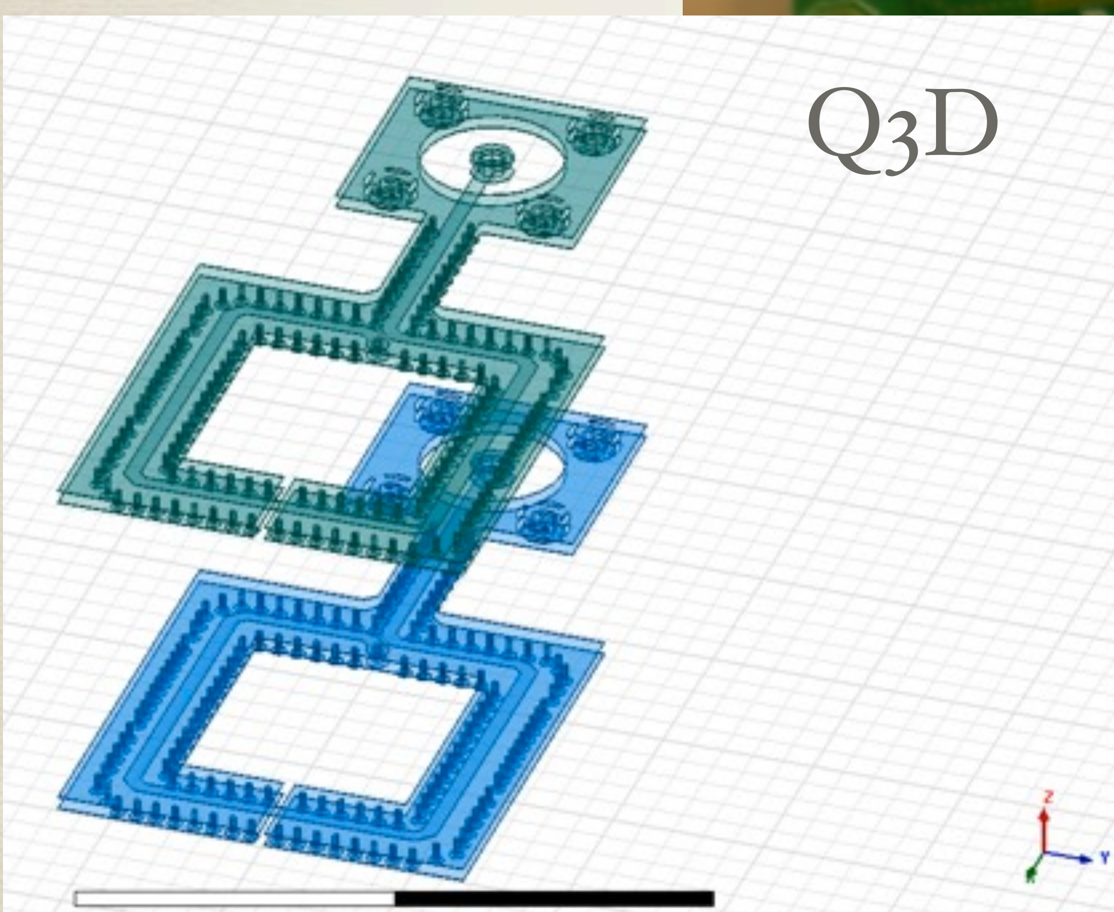
$$S_{21} = 20 \log \frac{2V_{R_L}}{E}$$

Simulation & validation

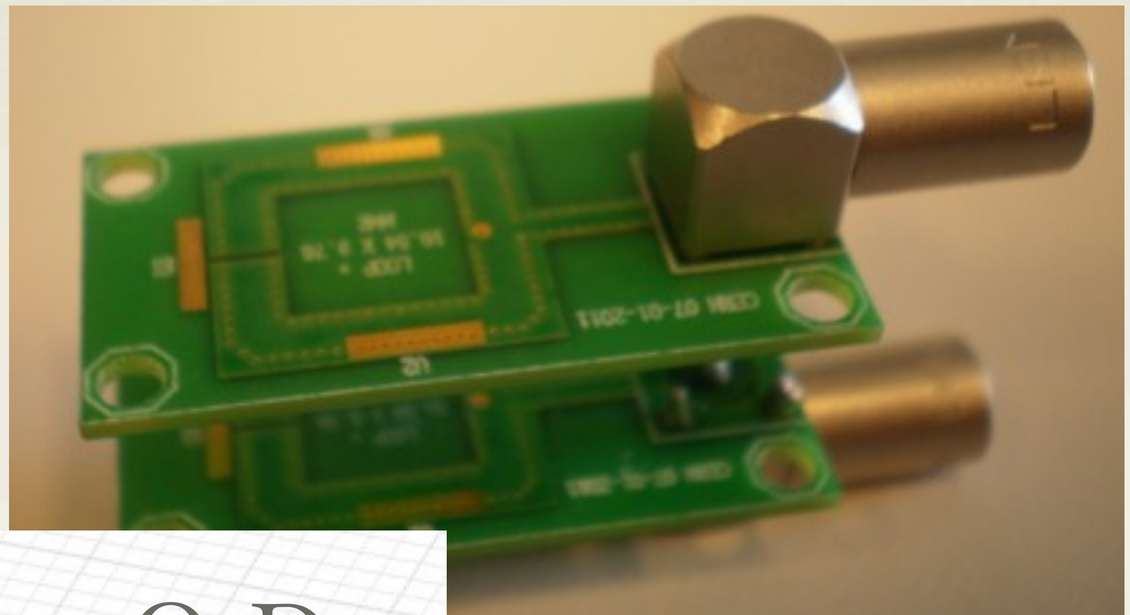


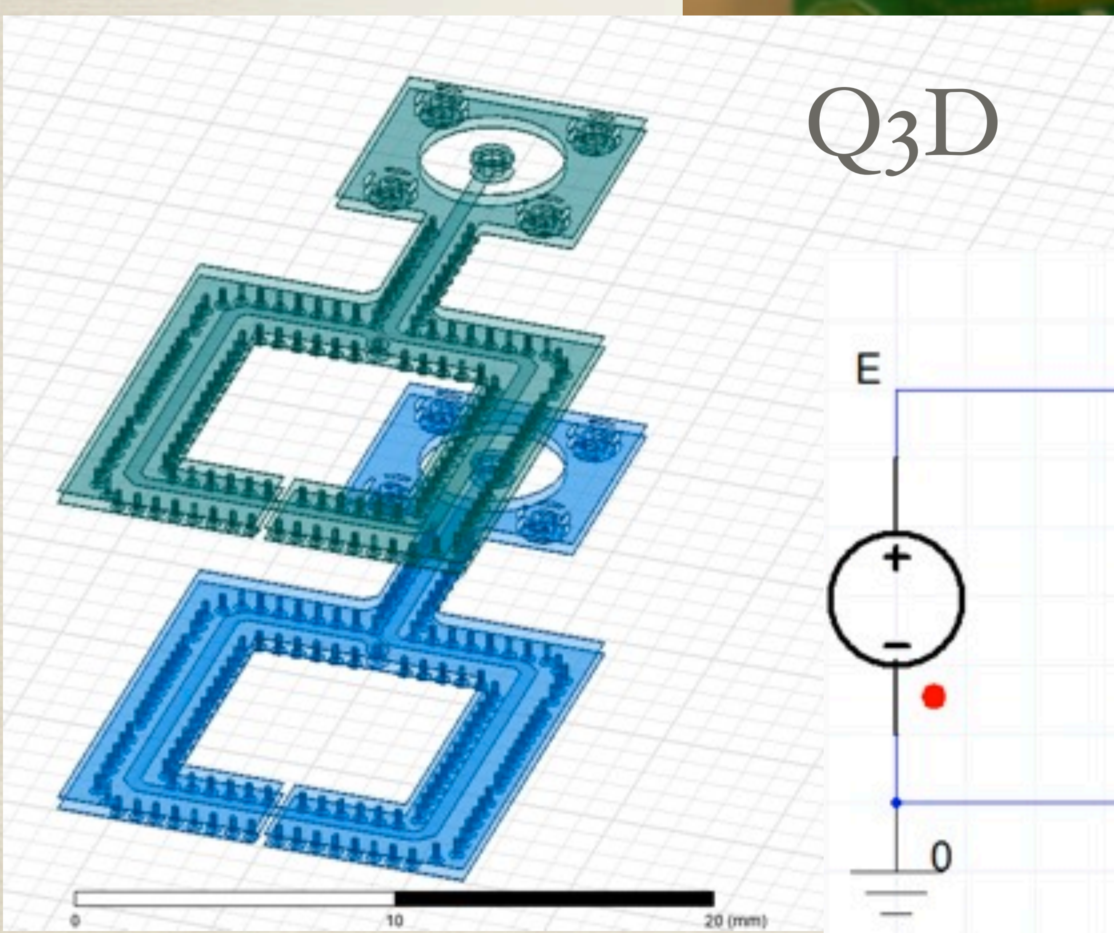
Simulation & validation

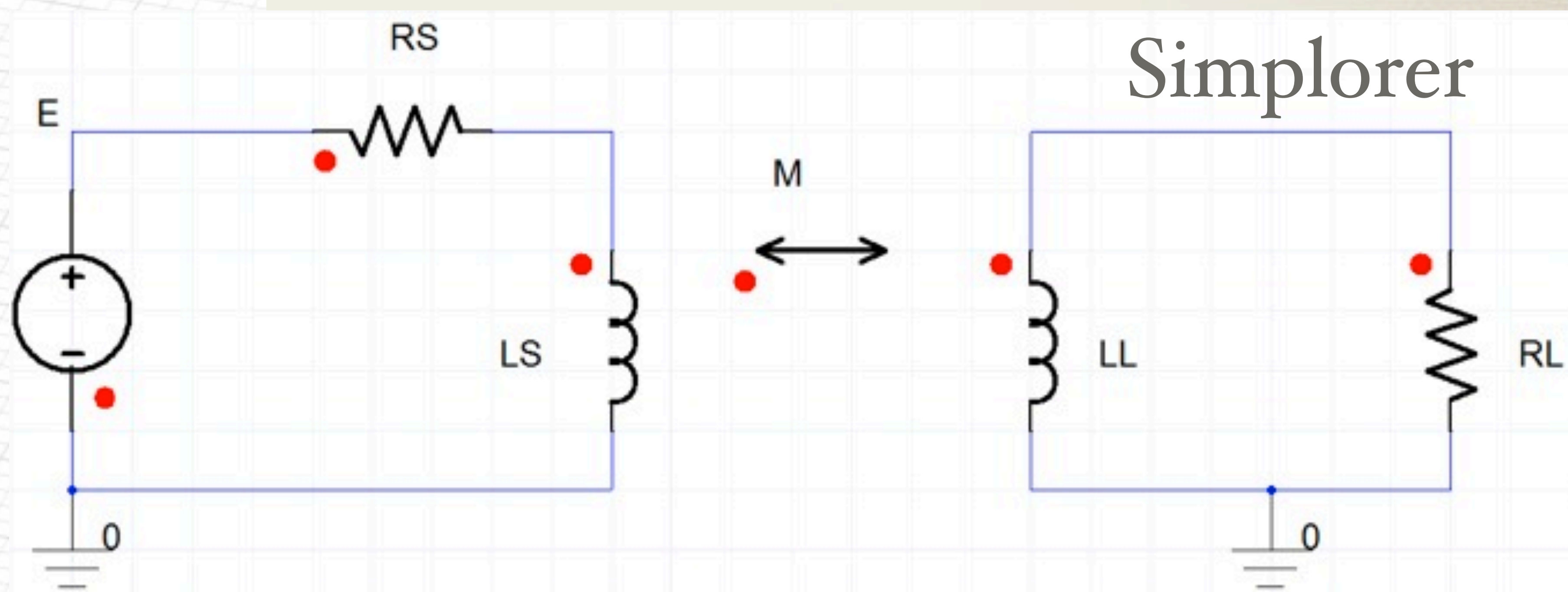




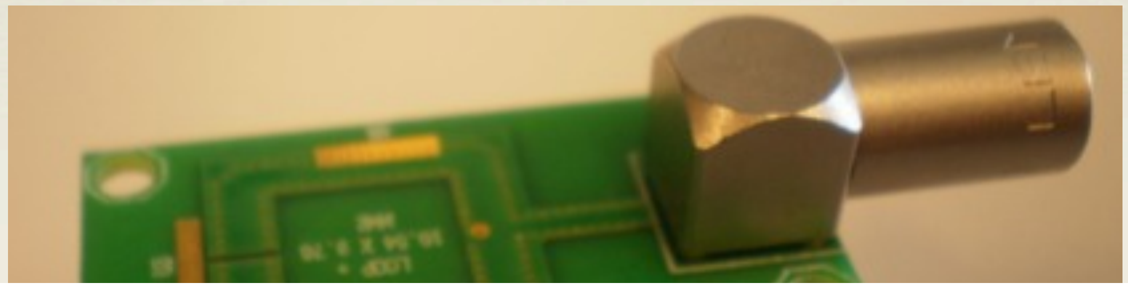
Simulation & validation

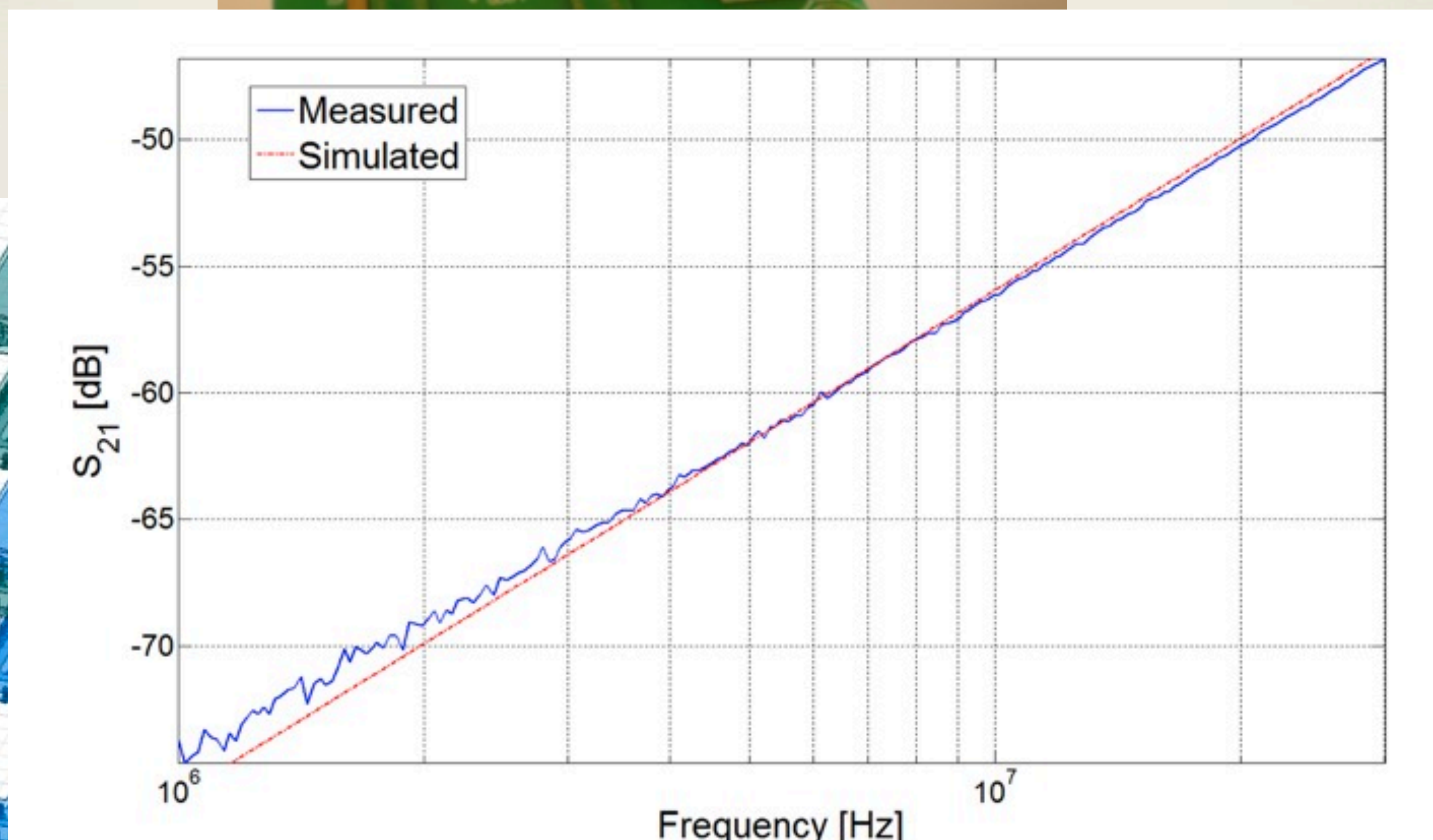


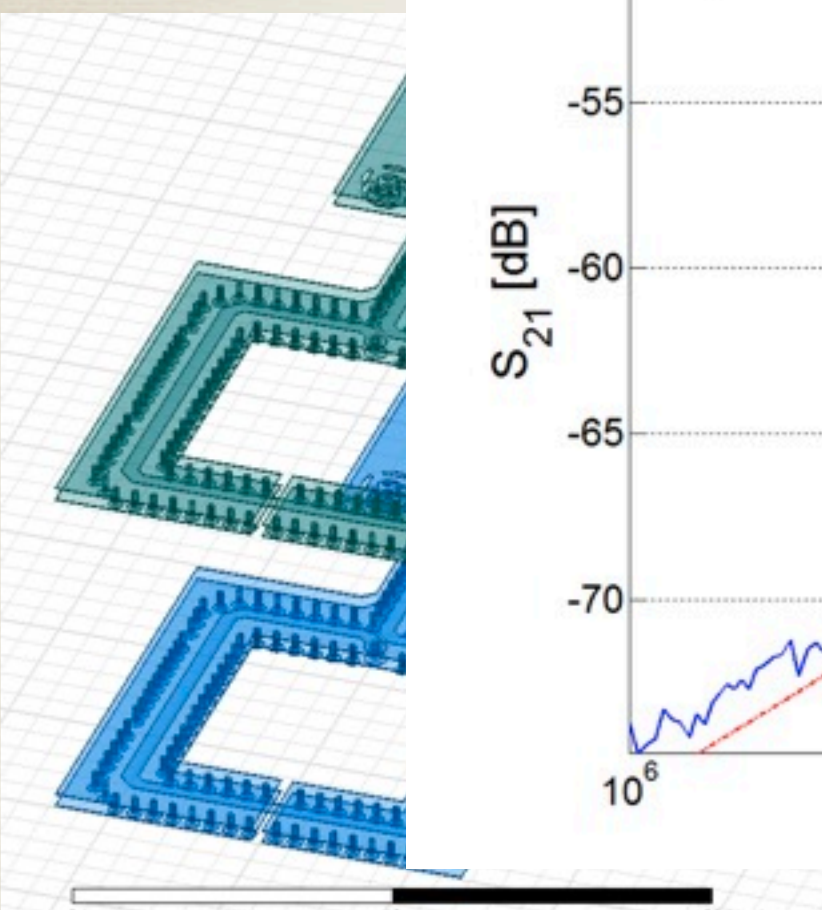




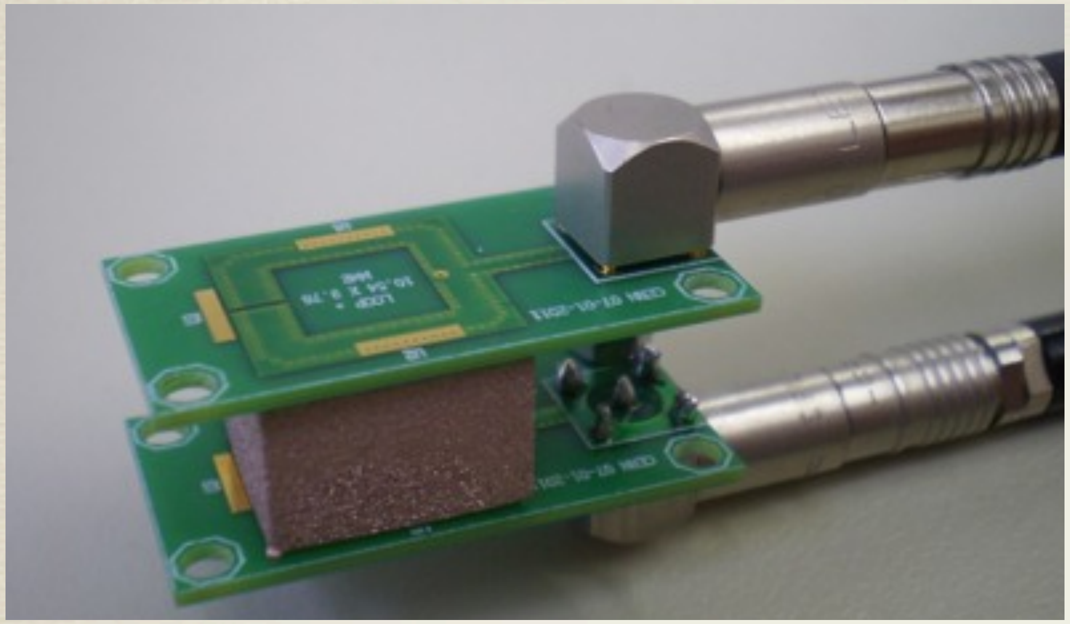
Simulation & validation



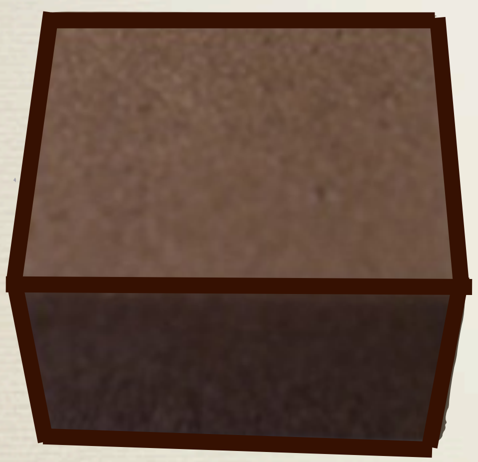




SE of some shields



Different constructions
and thickness (t)

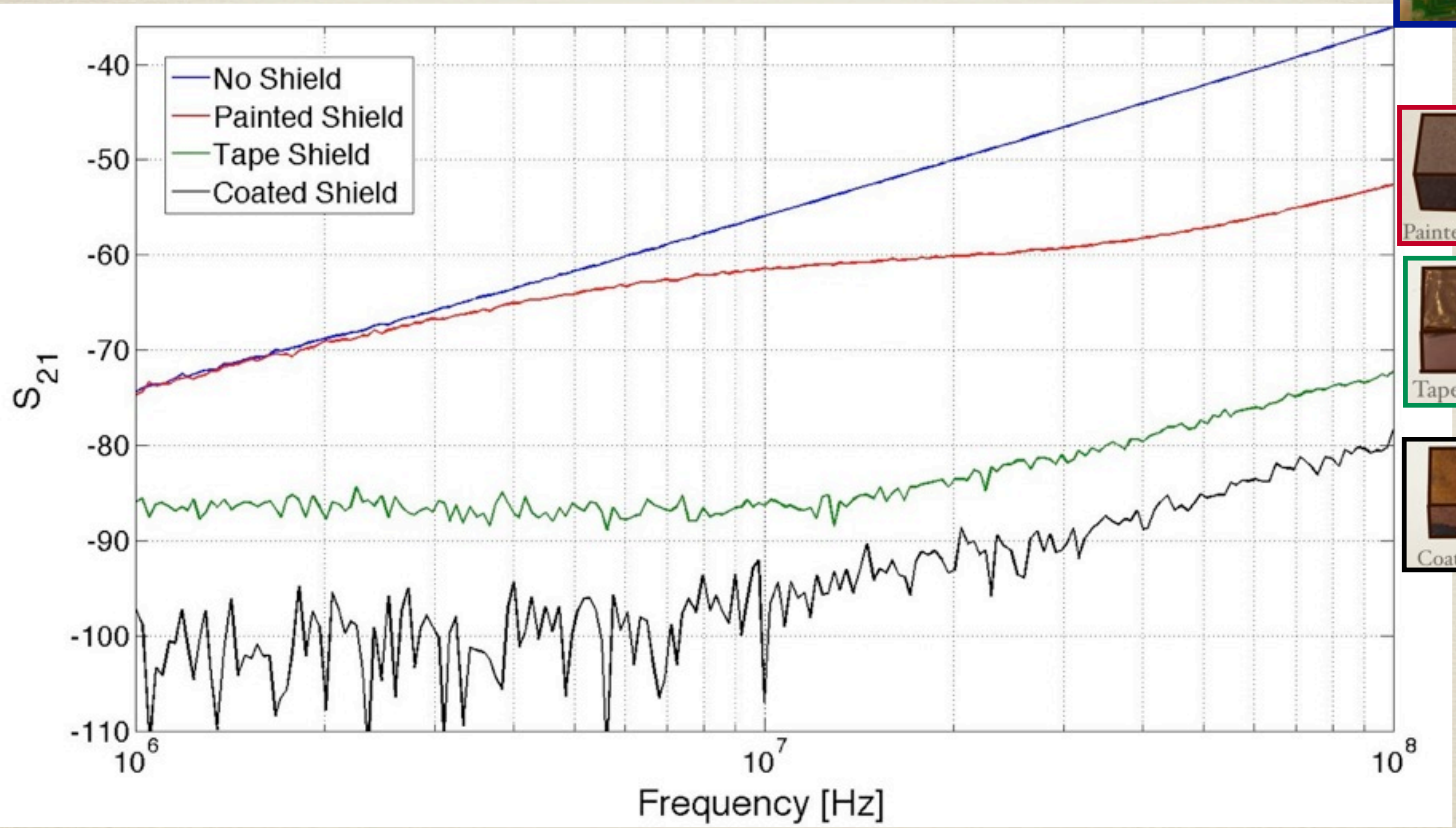


Painted Shield
$t = ???$

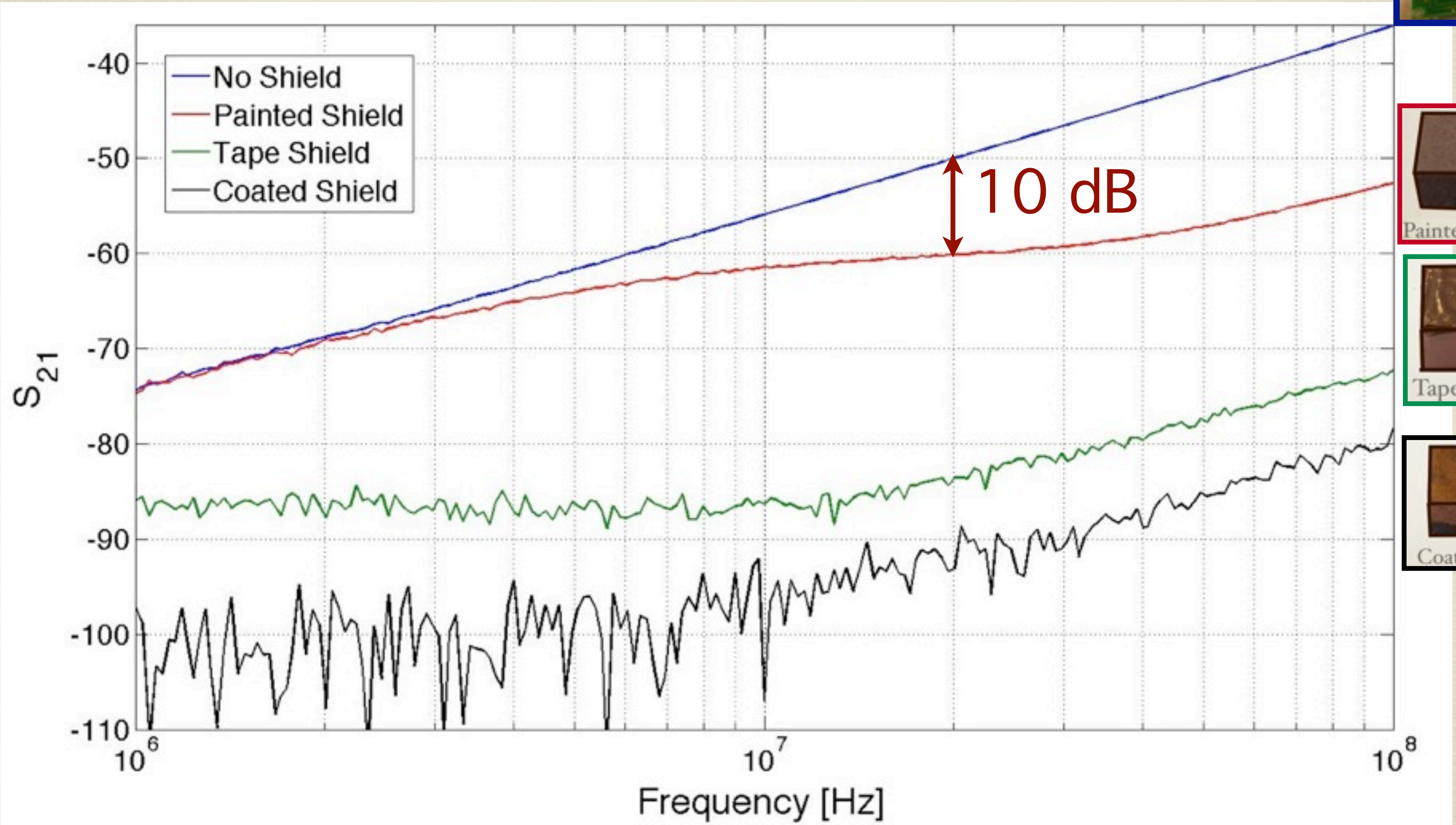
Tape Shield
$t = 35[\mu m]$

Coated Shield
$10 < t < 100[\mu m]$

SE of some shields



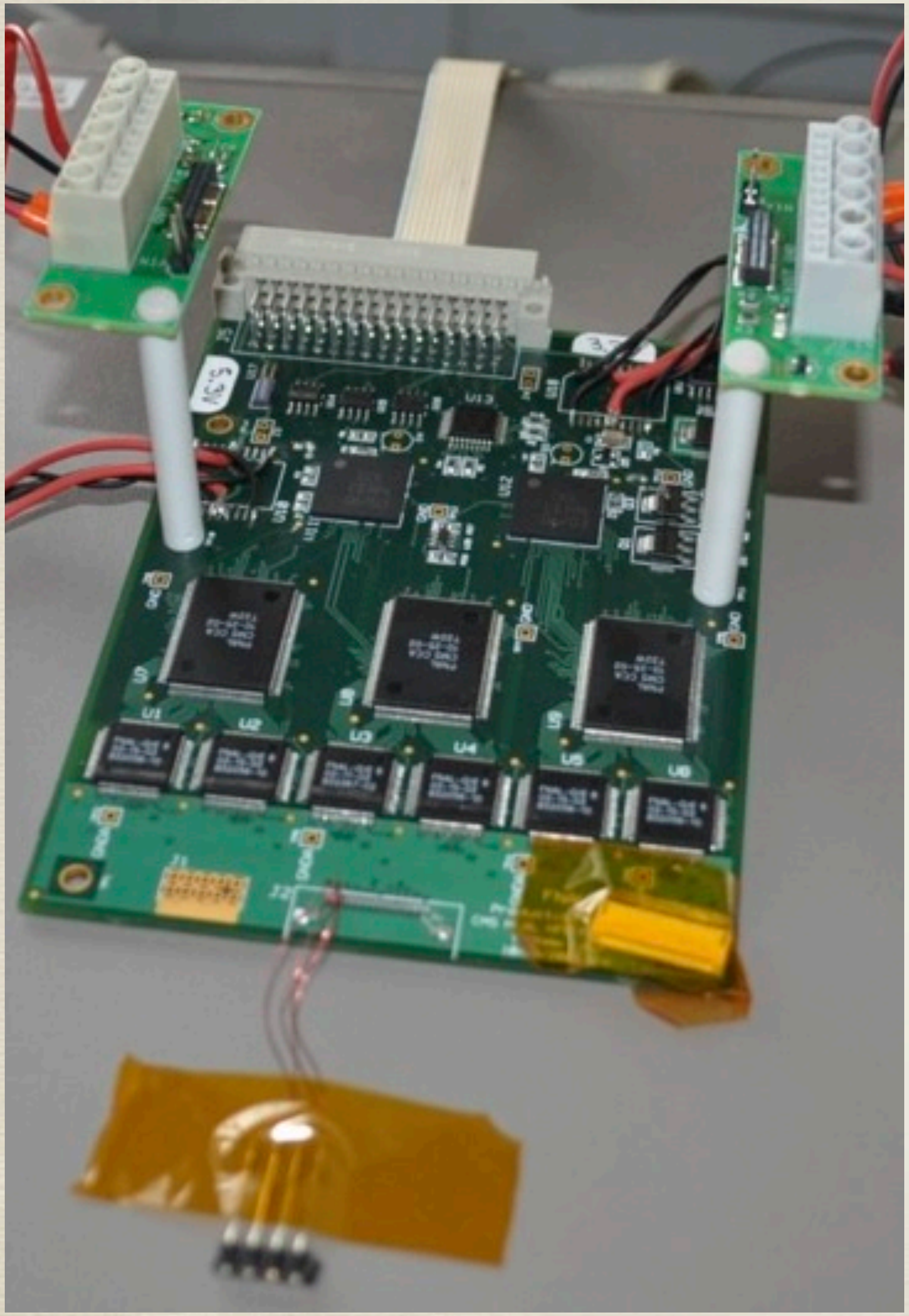
SE of some shields



Outline

- Motivation and project goal.
- Buck converter topology.
- ASIC developments.
- DC-DC Plug-in modules.
  - Coil development.
  - Shield development.
- System tests.
- Stability and dynamic properties.
- Conclusions.

1) Test with FEE Hcal CMS

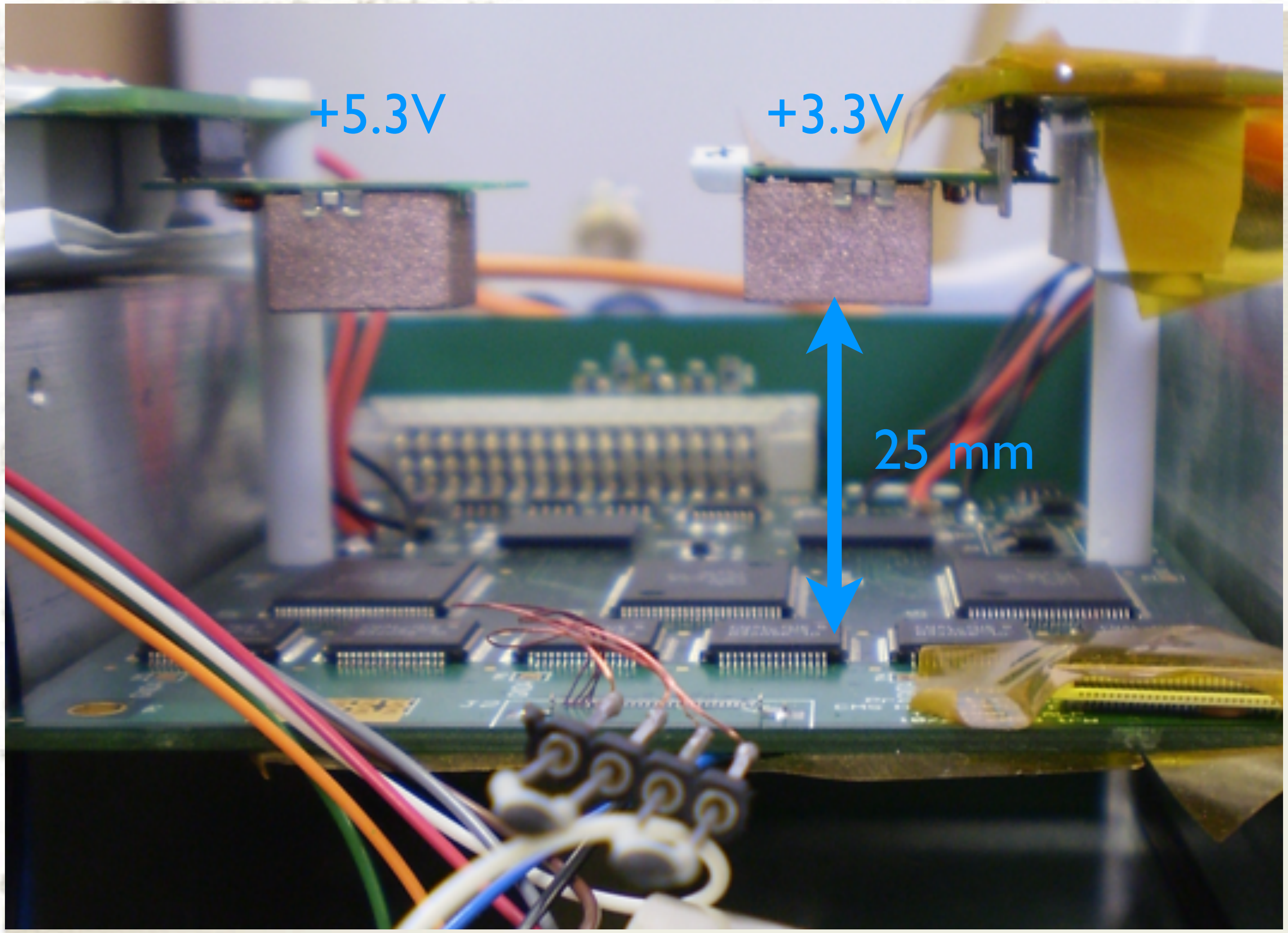


A front end board was powered using two SM01c dcdc converters.

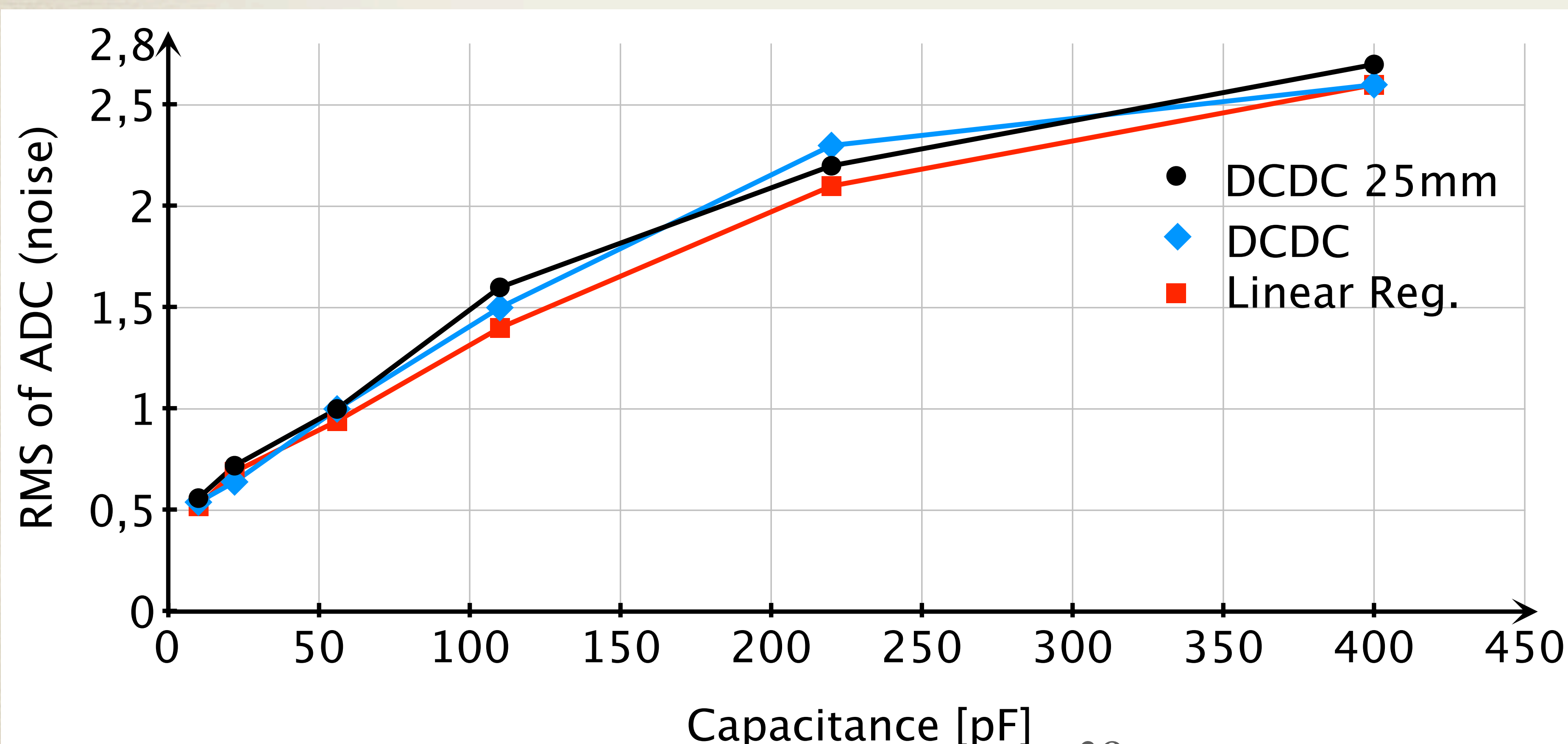
The converters were modified to fit the application needs. One converter providing 5.3V and the other 3.3V.

The system noise was compared with the one obtained while powering the FE board with the nominal Linear Regulator.

Thanks to: Tullio Grassi



- The same measurement was repeated for the converters upside down at 25mm from the QIE ASICs
- The use of DCDC converters at close proximity do not degrade the system performance.

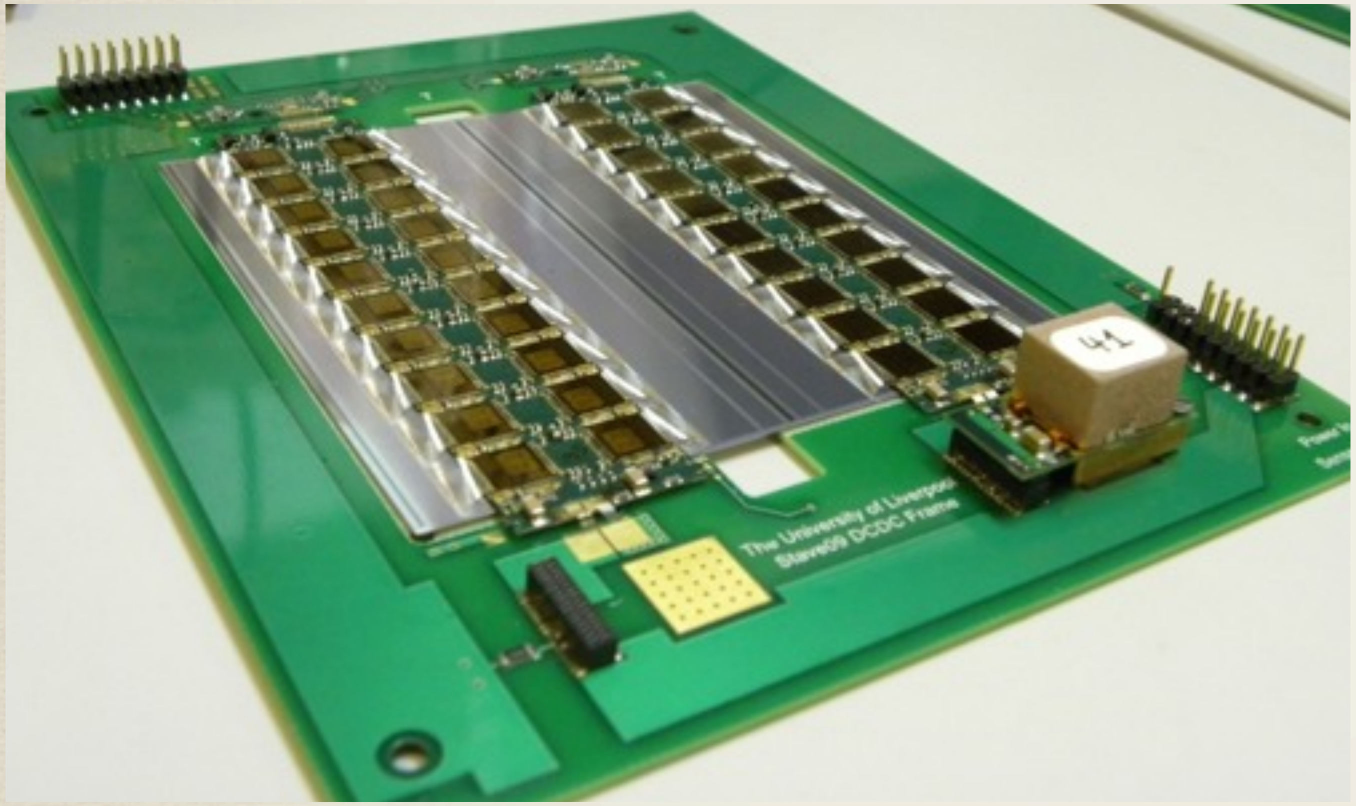


SWITCHING REGULATOR
(25 mm from QIE ASIC)

Capacitance (pF)	RMS of ADC
*10000	--
400	2,7
220	2,2
110	1,6
56	1
22	0,72
10	0,56

*10nF does not represent a feasible capacitance value for the photodiode

2)Test with Frame Module (Liverpool)

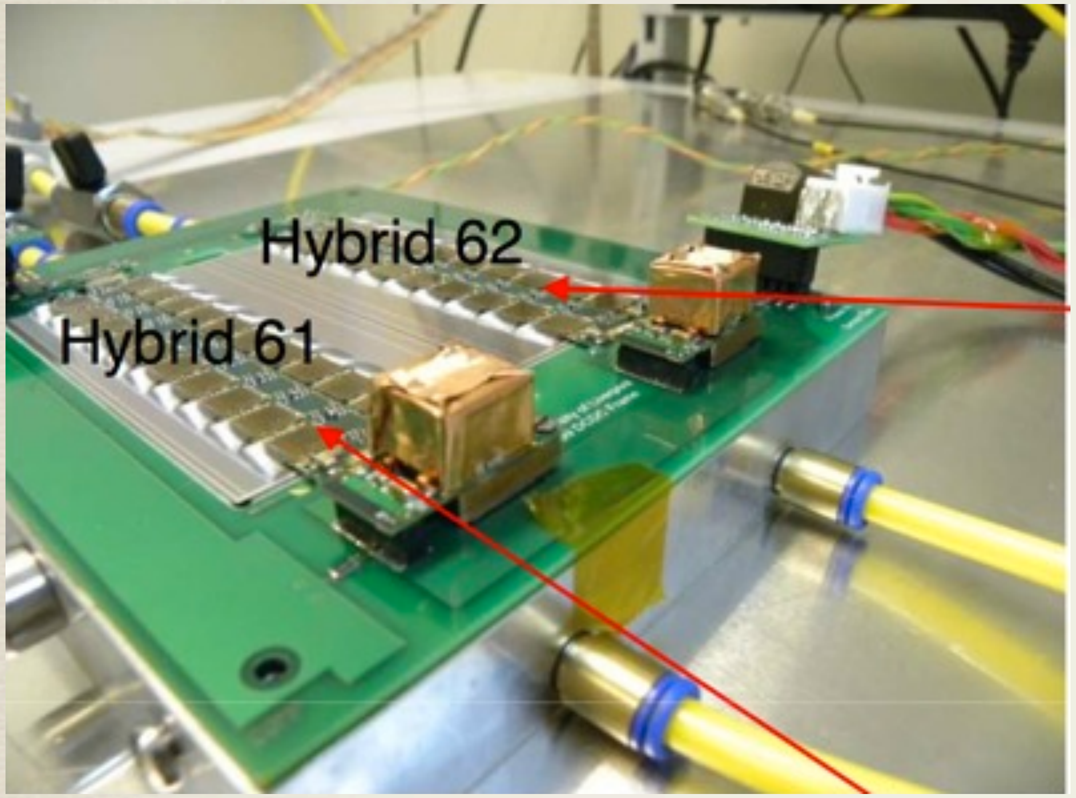


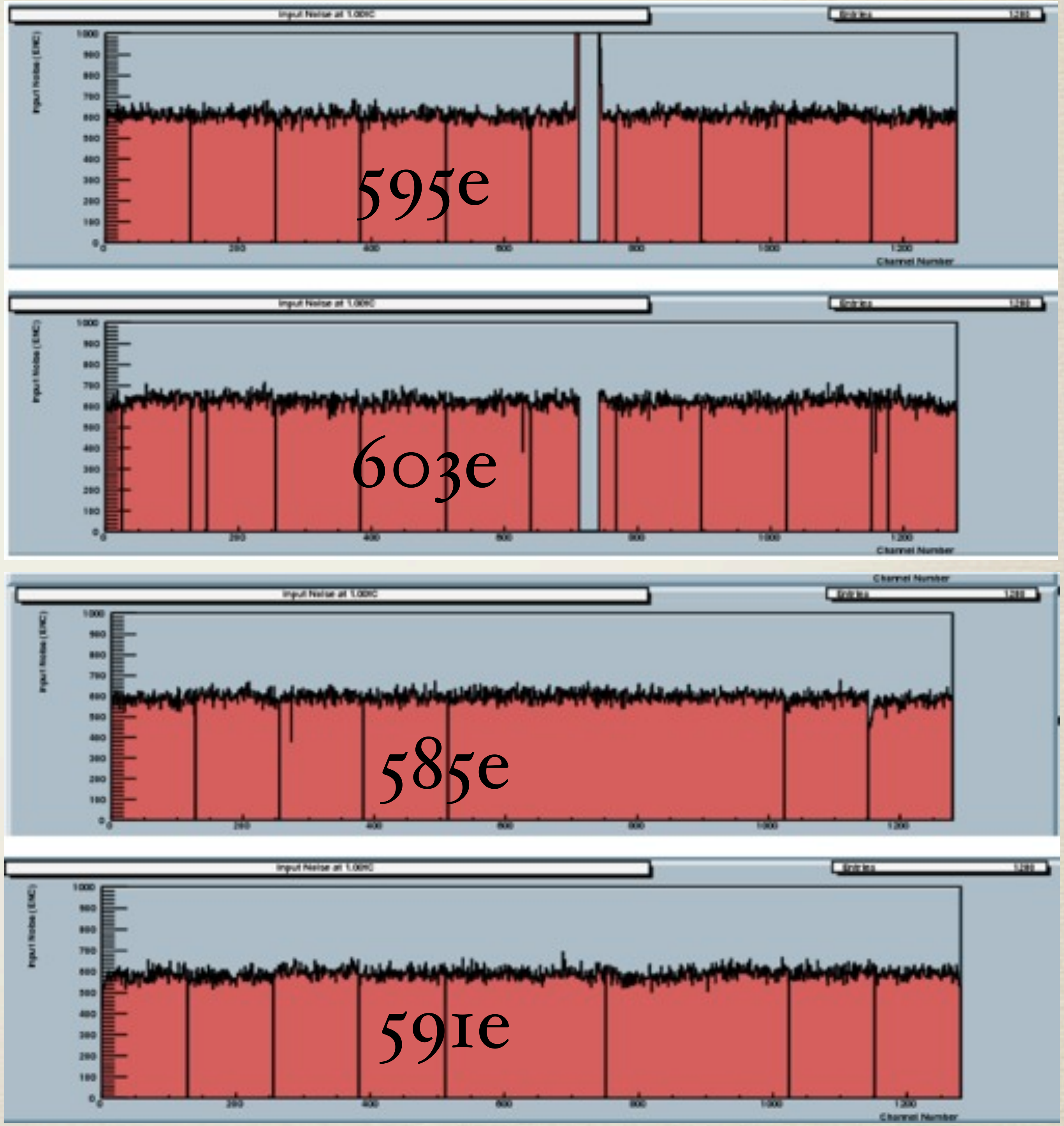
A Frame Module dedicated for DCDC converters have being tested using the two available converters.

Different shield were tried, in order to undestand compatibility issues.

Thanks to: Ashley Greenall & Tony Affolder

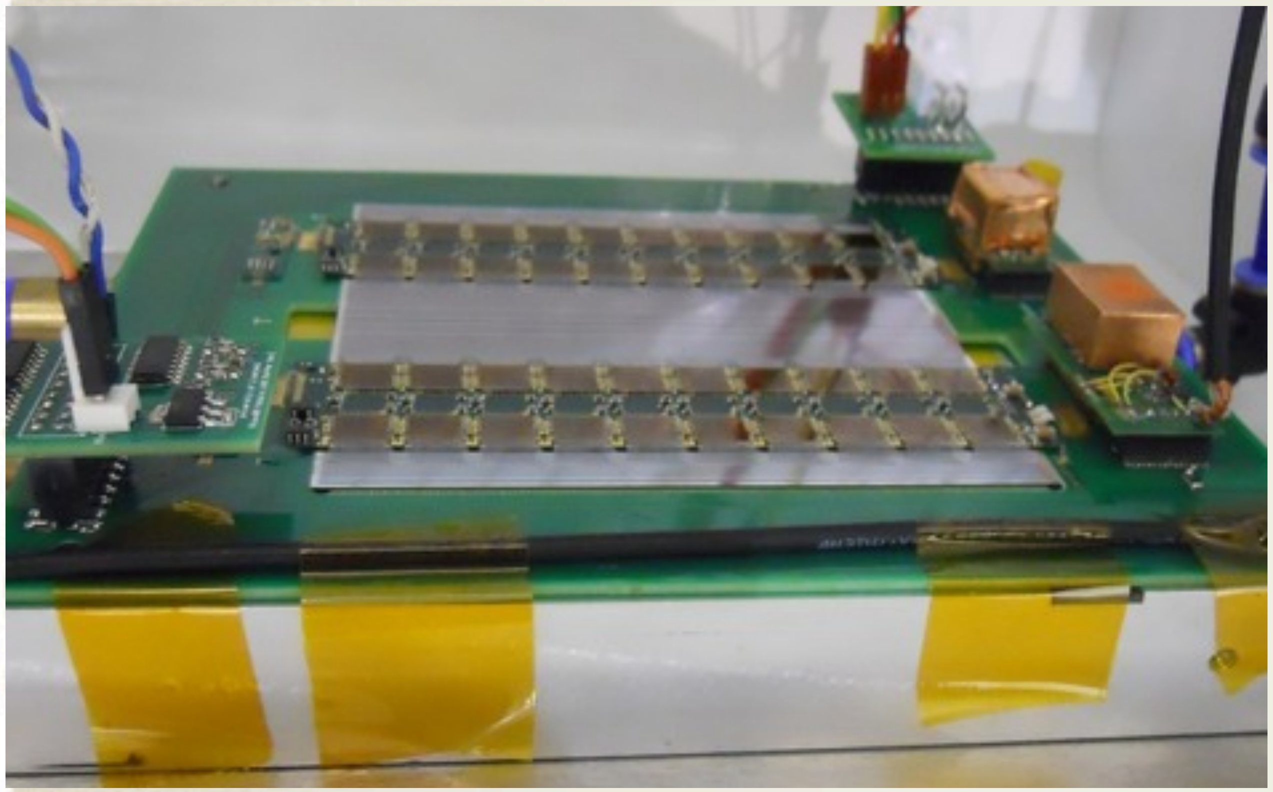
Shields wrapped with cu tape



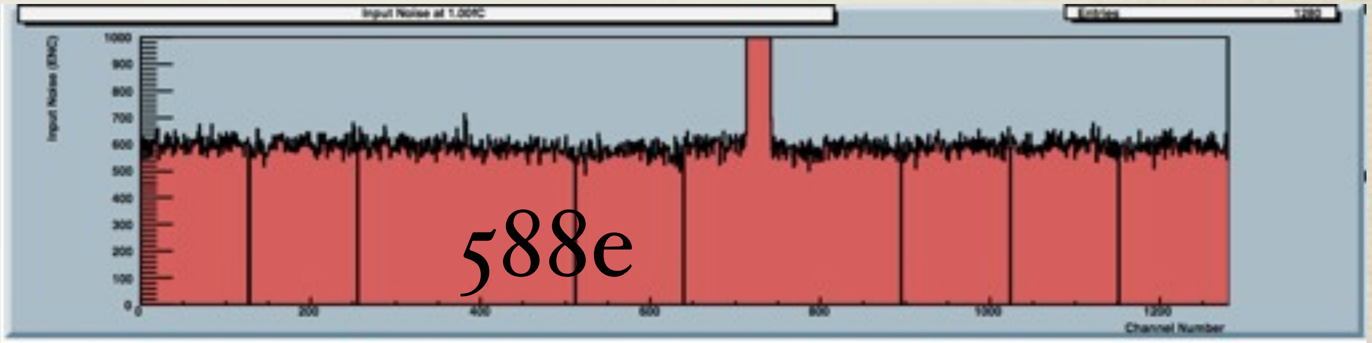


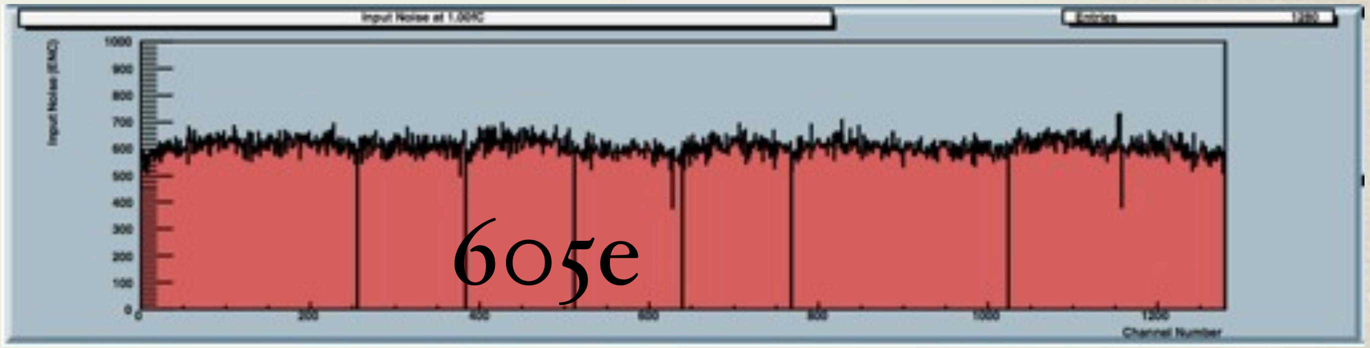
Hybrid	Linear regulator [ENC]	DCDC Shield Tape [ENC]
62	570	595
	596	603
61	585	585
	591	591

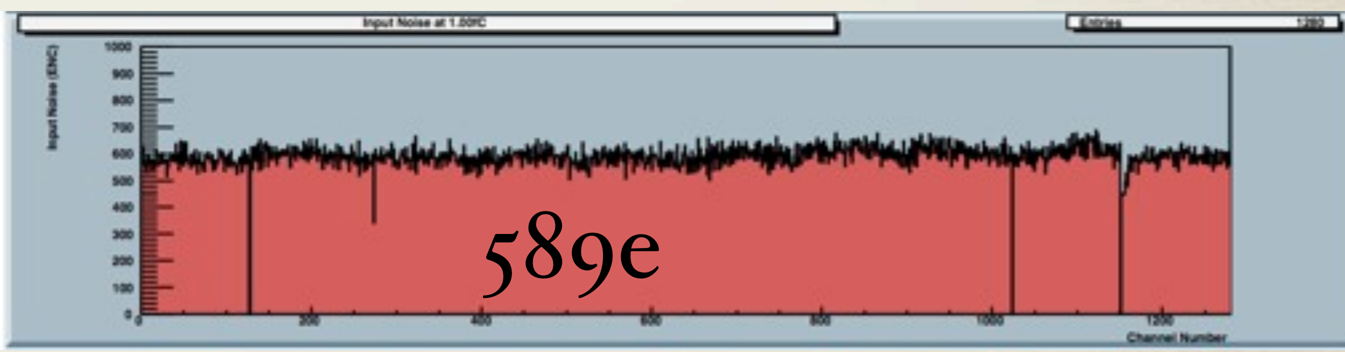
2)Test Frame Module with STV10 converter (@ bdg 180)

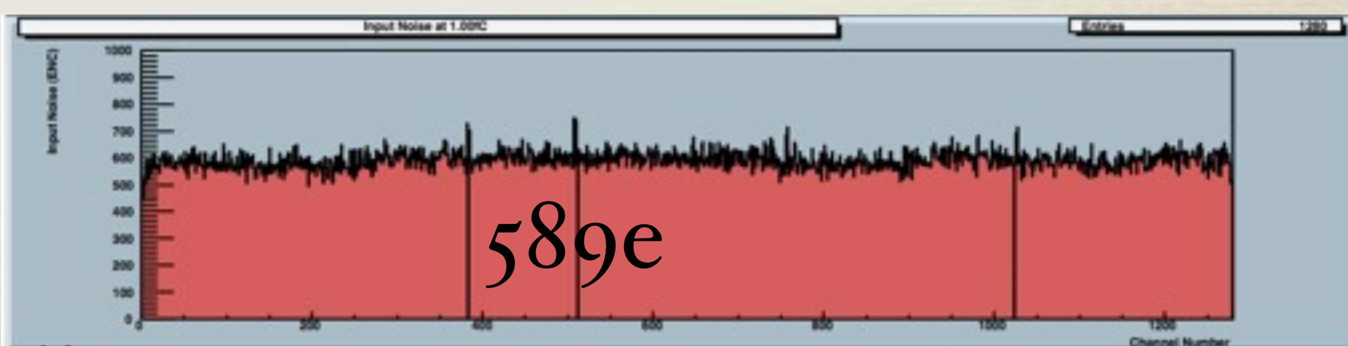


Hybrid	Linear regulator [ENC]	DCDC STV10 [ENC]
62	570	588
	596	605
61	585	589
	591	599









3)Test with UNIGE Module

Column	Reference ENC	ENC with SM01C + Cu tape
A	590	579
B	614	596
C	607	600
D	614	604

Thanks to: Didier Ferrere & Sergio Gonzalez-Sevilla

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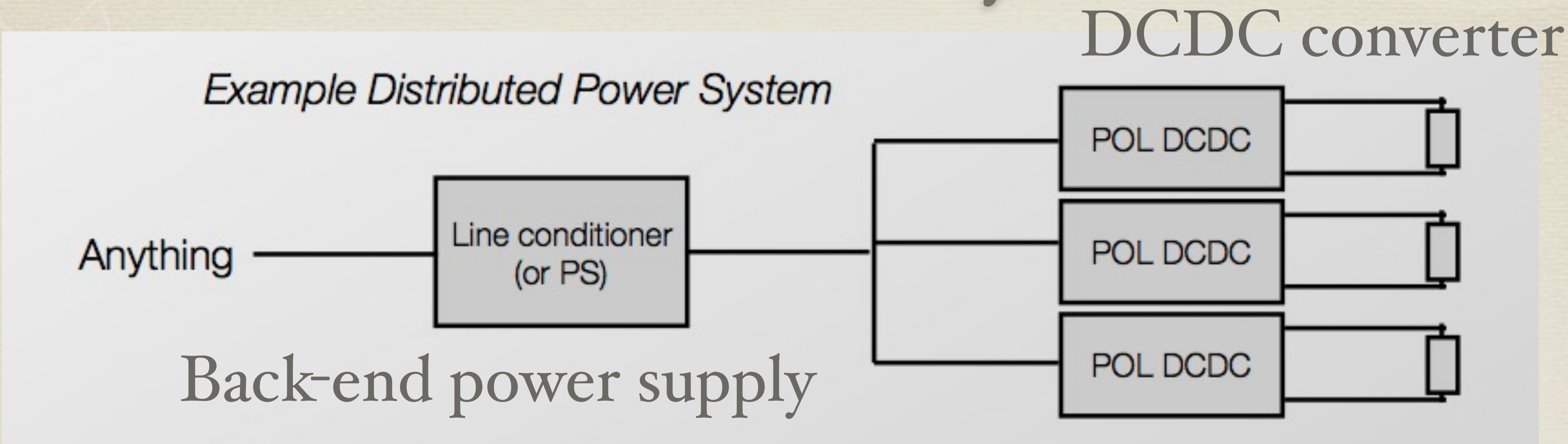
Stability



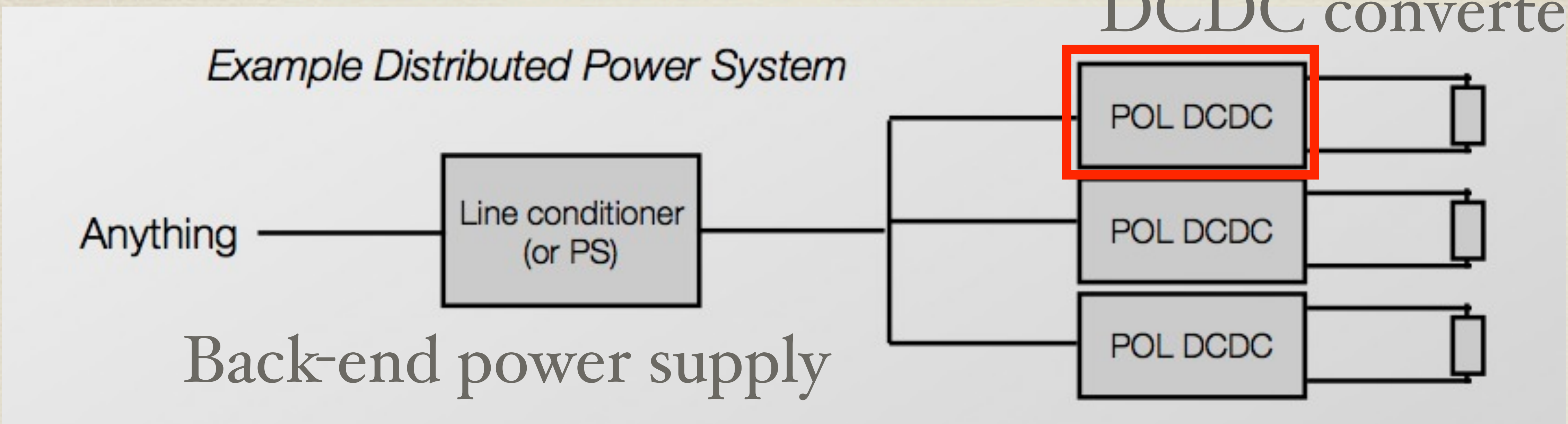
Federico Faccio et al: DC-DC stability studies

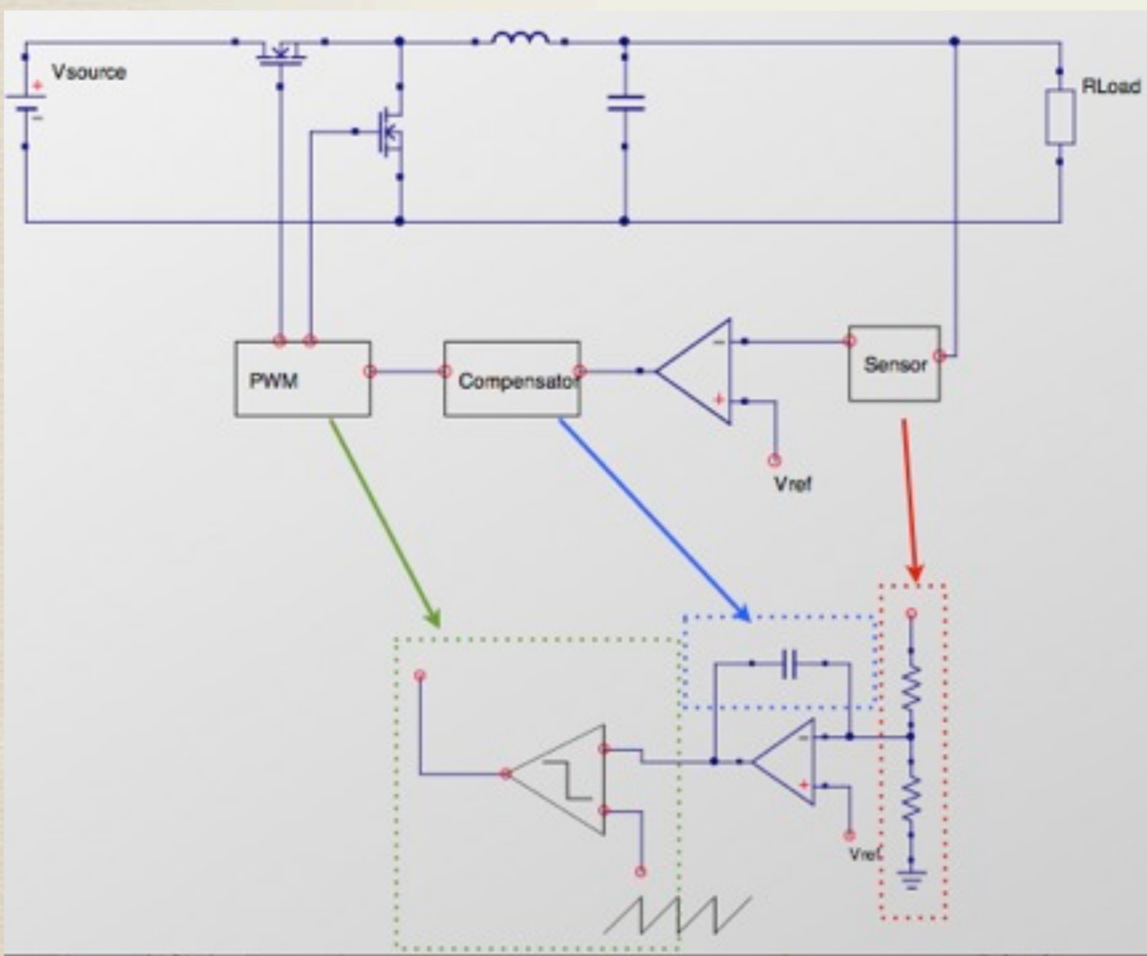
ATLAS-CMS Power Working Group

http://indico.cern.ch/getFile.py/access?contribId=7&resId=0&materialId=slides&confId=127662

Stability

DCDC converter





T(s) = loop gain = product of all gains around forward and feedback paths of the loop

Federico Faccio et al: DC-DC stability studies

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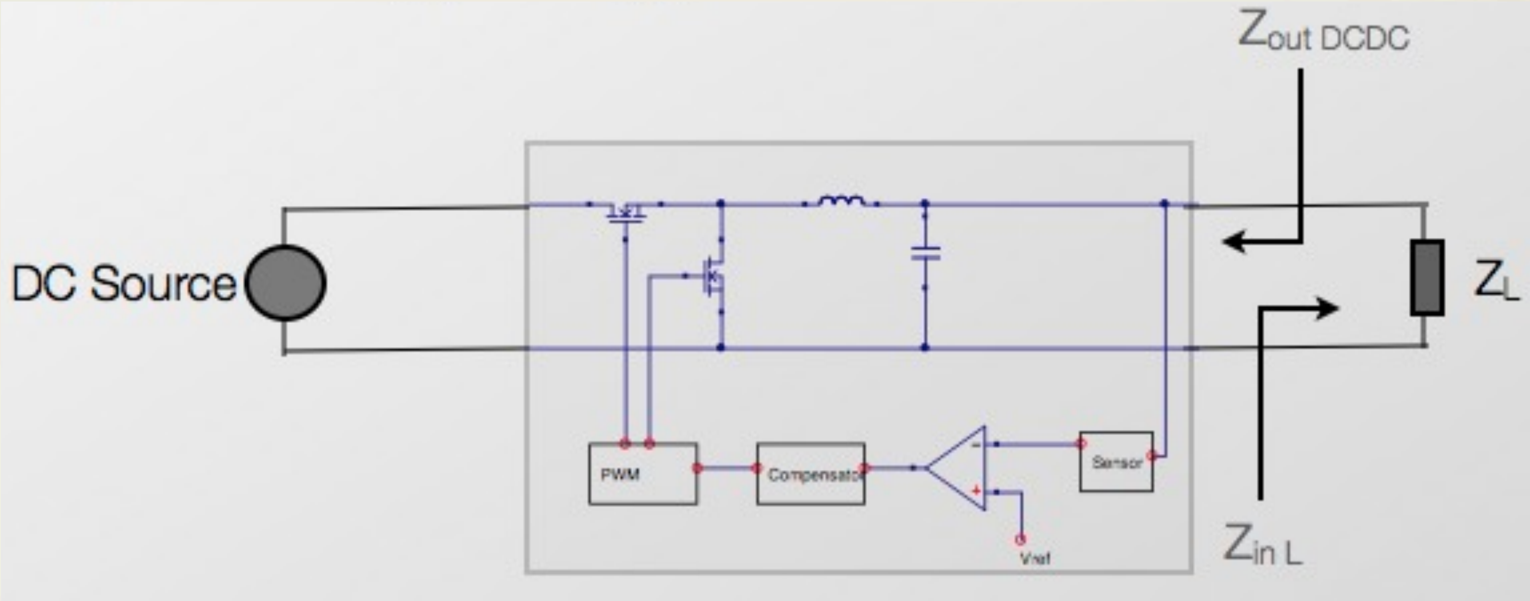
http://indico.cern.ch/getFile.py/access?contribId=7&resId=0&materialId=slides&confId=127662

Load effect on converter's loop gain

The addition of a 'generic' load impedance Z_L to the 'nominal' R_L modifies the Loop Gain: T(s) -> T'(s)



$Z_o << Z_L$

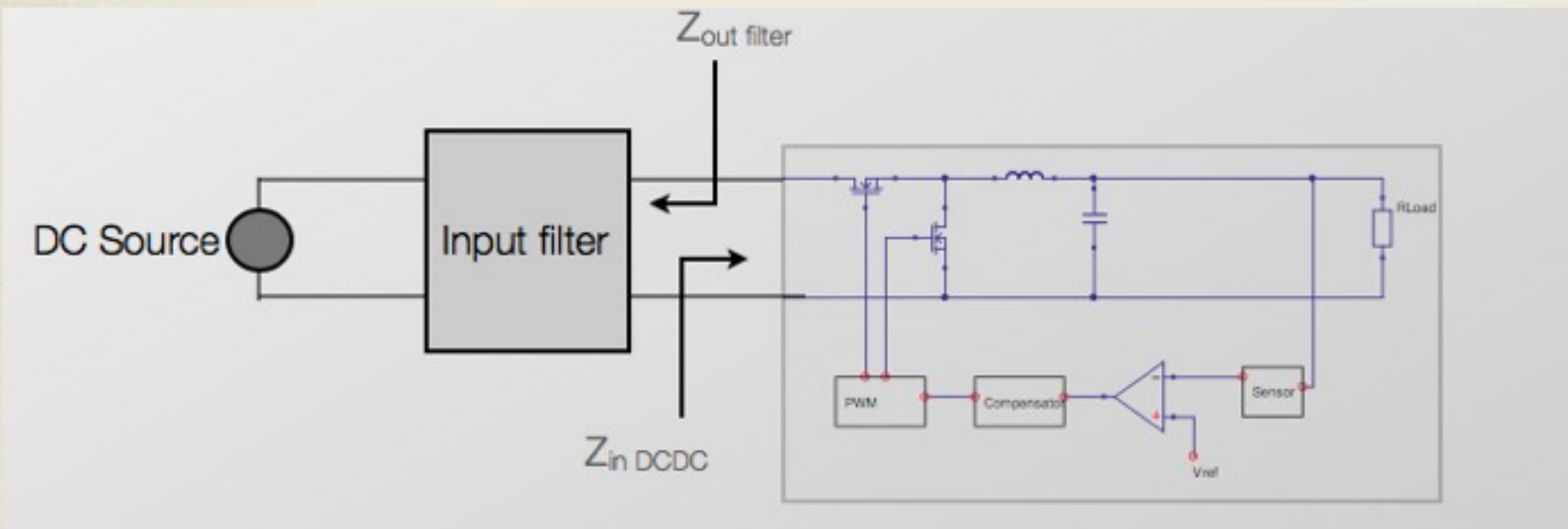
If $Z_o/Z_L << 1$ then $T'(s) = T(s)$ and the stability of the converter is NOT affected by the addition of the output impedance. This translates in the commonly used stability criteria:

$$T'(s) = \frac{T(s)}{(1+T(s))Z_o/Z_L + 1}$$

NB: if the criteria is not satisfied, T(s) is modified but the converter could still be stable

Input effect on converter's loop gain

- So far the input voltage was provided by an ideal source

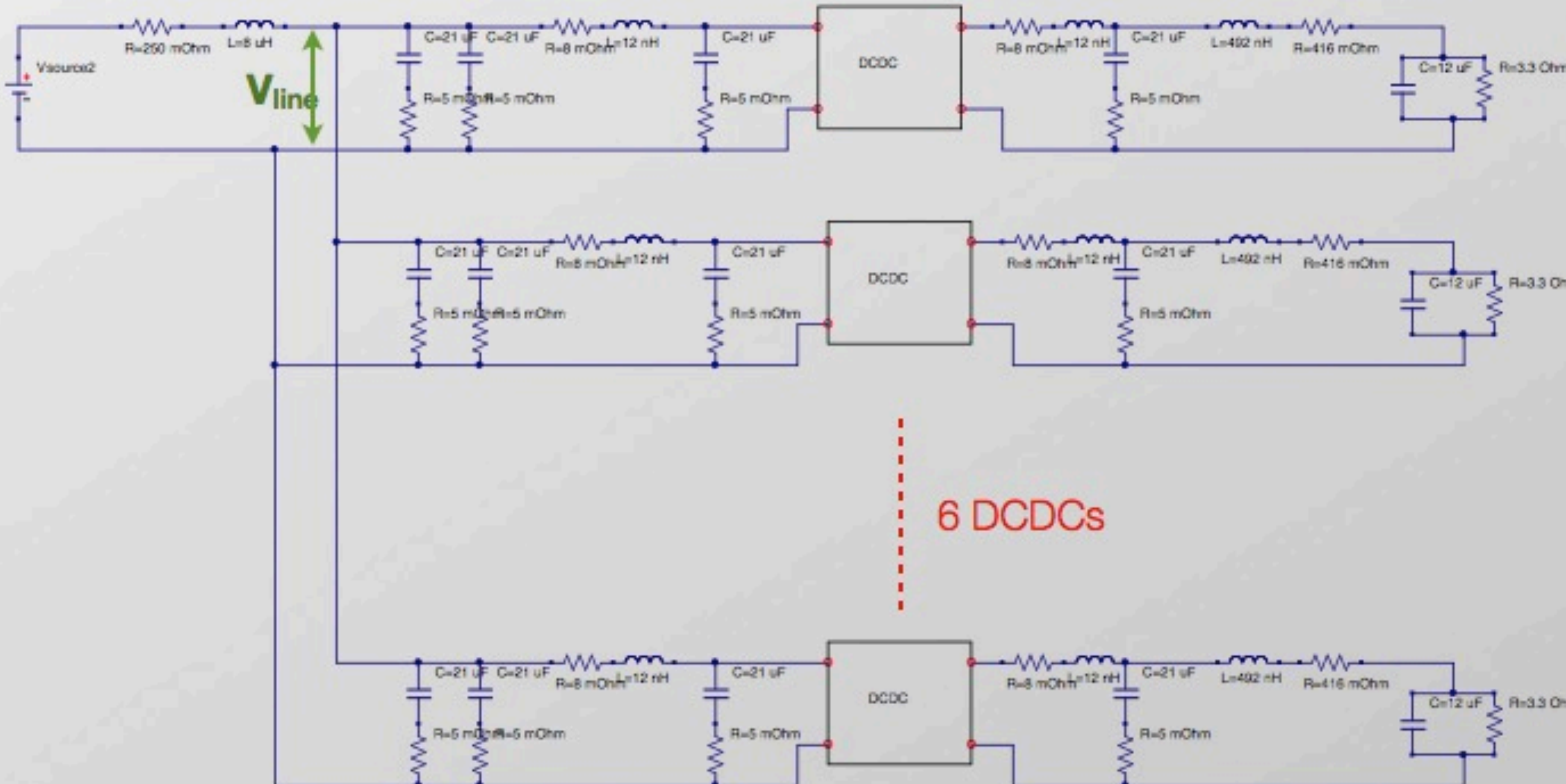


- Anything making the source non-ideal (R,L,C) can be seen as an input filter
- As before, there is a condition involving the impedances of the filter and DCDC converter for the loop gain T(s) NOT to be modified by the filter
- For the buck converter, this condition can approximately be expressed as

$$Z_{out\ filter} << Z_{in\ DCDC}$$

Case study: CMS pixels upgrade phase 1

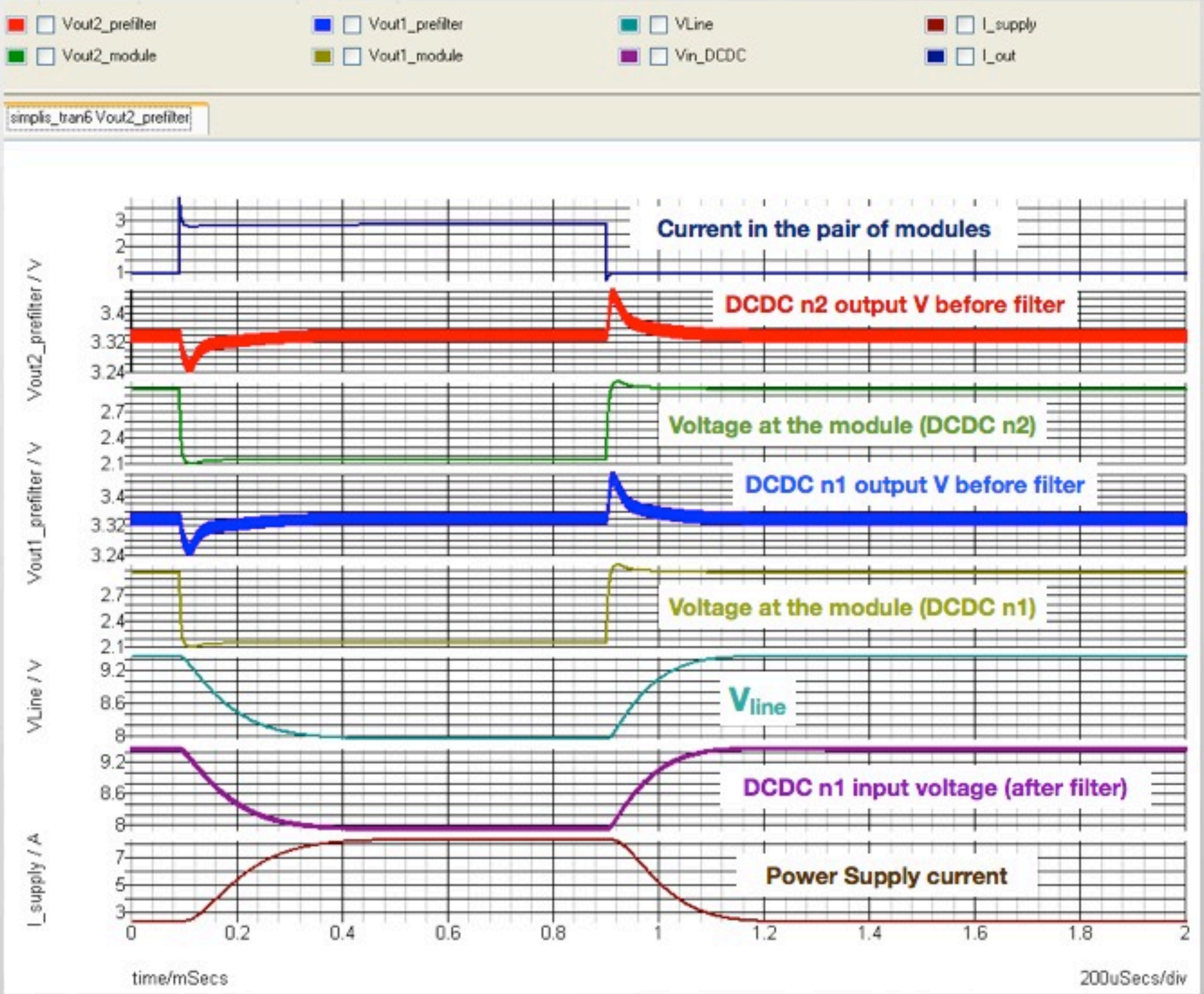
- The full distribution scheme (with ideal PS) is studied, using the best available estimates
- As case study, and to have the maximum current transient, a specific (unreal) configuration is chosen: 1 PS channel powering 6 DCDCs belonging to Layer1 (2 modules powered by each DCDC)



Load transients for each DCDC
1A -> 2.8A -> 1A

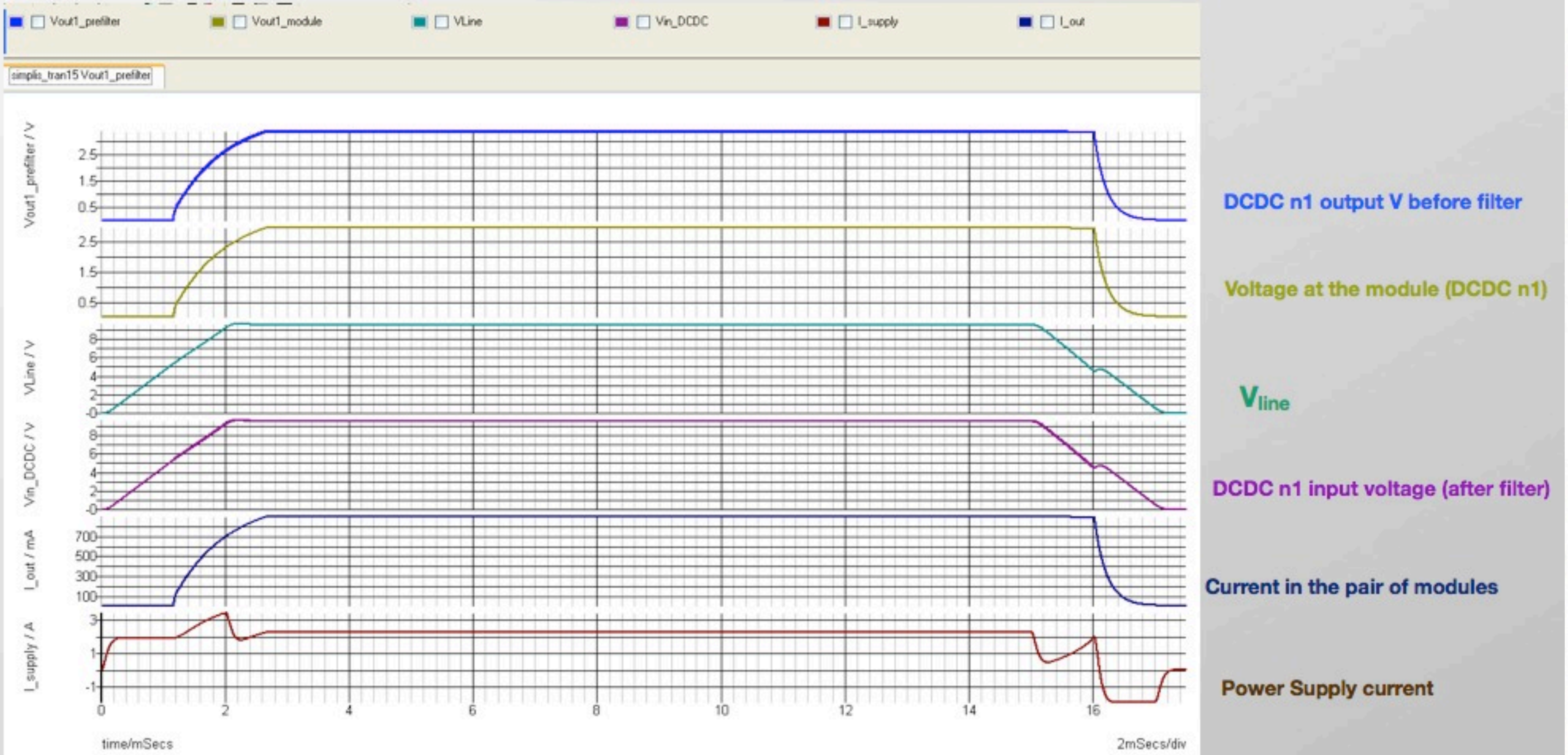
Two load transients

- Each module pair instantaneously (NOT in 100ns as in reality) changes current from 1A to 2.8A, then back



Power-on & power-off of full PS channel

- Voltage ramp from the PS (rise & fall time 2ms) to turn-on and -off all 6 converters loaded with an equivalent 1A current



Conclusions

- **SM01C power module is available for system tests**
  - Available now.
  - High conversion efficiency (expect 85%).
  - Individual control and monitoring possible.
  - Datasheet available. http://project-dcdc.web.cern.ch/project-DCDC/
- **Radiation tolerant ASICs are available**
  - AMIS2 power module is very low noise and is qualified for high radiation tolerance.
  - AMIS3 and AMIS4 will be more performant than AMIS2 and will become available in few weeks.
  - Ongoing R&D to reach radiation tolerance with IHP.
- **System tests showed good compatibility even with the most demanding tracker configurations.**
  - Noise is comparable to the one obtained using a linear power supply.
  - Stability and dynamic properties can be studied for different systems.
  - Material reduction studies are carried out for material budget critical systems.