Status of Development of ECS unit for Counting Room Electronics

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Topics

The Concept

goal

Gen Purpose ECS unit for Config, Mon and Debug: access PVSS in control room (CR)

CR $\leftrightarrow$ Ethernet $\leftrightarrow$ embedded PC $\leftrightarrow$ $\underbrace{\text{PCIe}}_{\text{high speed (HS)}}$, $\underbrace{\text{I}^2\text{C, JTAG, SPI}}_{\text{low speed (LS)}}$ $\leftrightarrow$ board

focus on TELL board

TELL ECS Scenarios

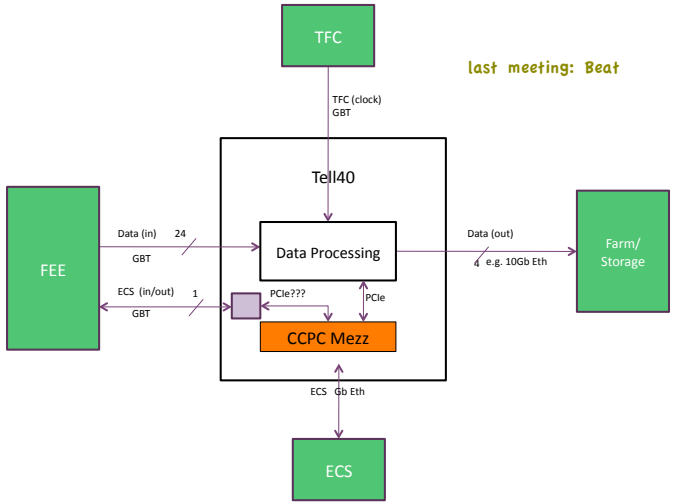
dedicated Processor for TELL

dedicated Processor for TELL $\leftrightarrow$ FEE

Compactness

Unique Mezzanine &

exploring FPGA in low speed line



The Schedule

Schedule expectation of previous meeting

Prototype → Final HW & SW → Validation 2011-12

Mass Production → Installation (?)/16

Schedule

$\underbrace{1^{st}\ \text{PROTOTYPE}}_{2011} \leftrightarrow$ Testing with TELL $\leftrightarrow \underbrace{\text{SMALL PRODUCTION}}_{2012} \leftrightarrow$ *3 years*:

$\underbrace{\text{firmware}}_{\text{debugging,kernel}}$, $\underbrace{\text{HardWare}}_{\text{New Tech (only CCPC)}} \leftrightarrow \underbrace{\text{LARGE PRODUCTION}}_{2015} \leftrightarrow \underbrace{\text{SHUTDOWN}}_{2016}$

- 1^{st} Prototype will be ready 2^{nd} semester (22^{nd} oct - 22^{nd} nov)

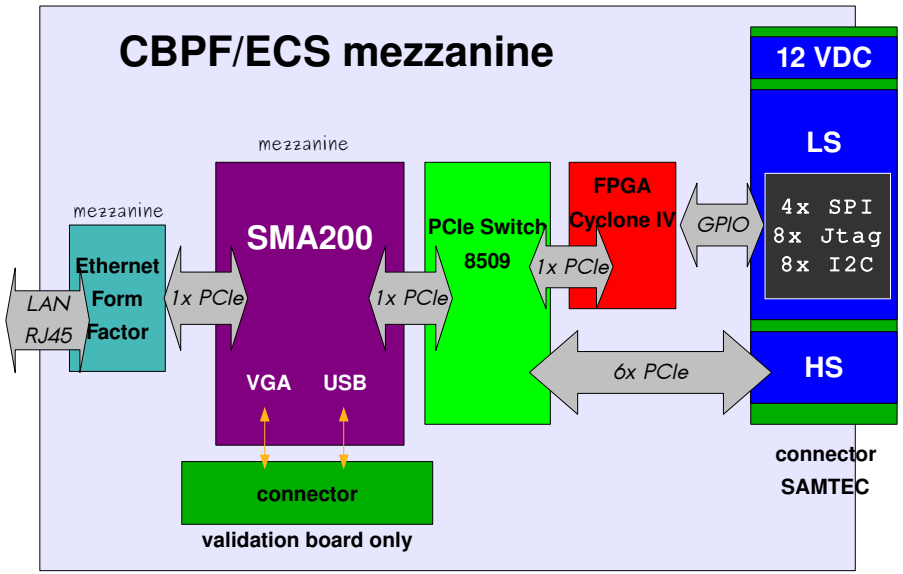
  Lausanne/Marseille for Testing
- other projects than TELL (?): 2012 production

  about 50 pieces (?)

The Design (as discussed with Guido and Jean-Pierre)

- CCPC with PCIe lanes: SMA200
- Ethernet 1Gbs LAN: Form Factor
- Switch drives:
  - → at least 4 PCIe lines
    HS block transfer
  - → 1 PCIe lane to FPGA
    translation to LS protocols
- 8 outputs I^2C
- 8 outputs JTAG no chain
- 4 outputs SPI

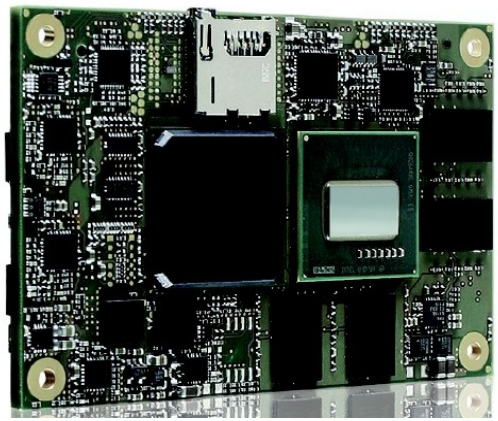
Actual design



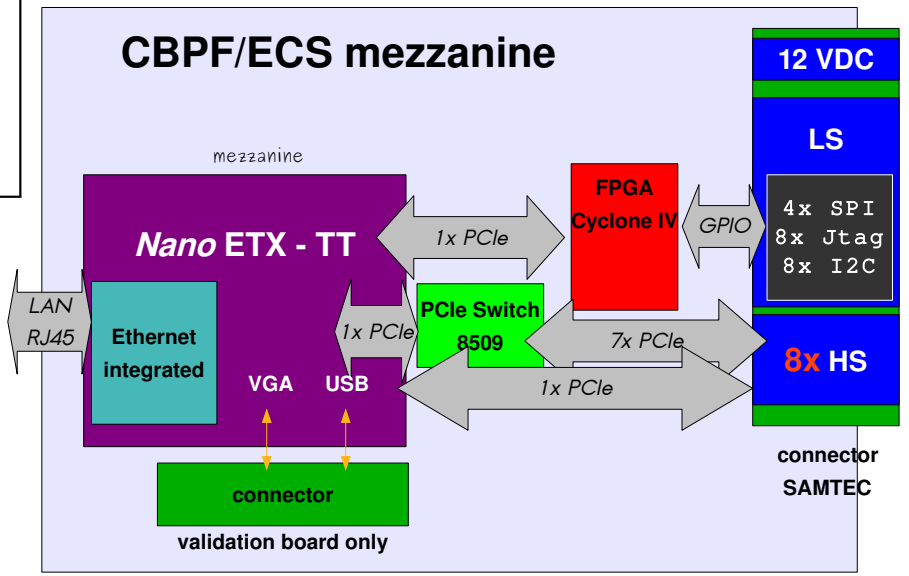
The Design (Jean-Pierre suggestion)

- CCPC with PCIe
- Ethernet 1Gbs LAN:

*nano***ETX-TT** express 3 lanes
Kontron Intel 1GHz 2GB DDR2
INTEGRATED CCPC ↔ Eth
5.76W full CPU *84x55mm*

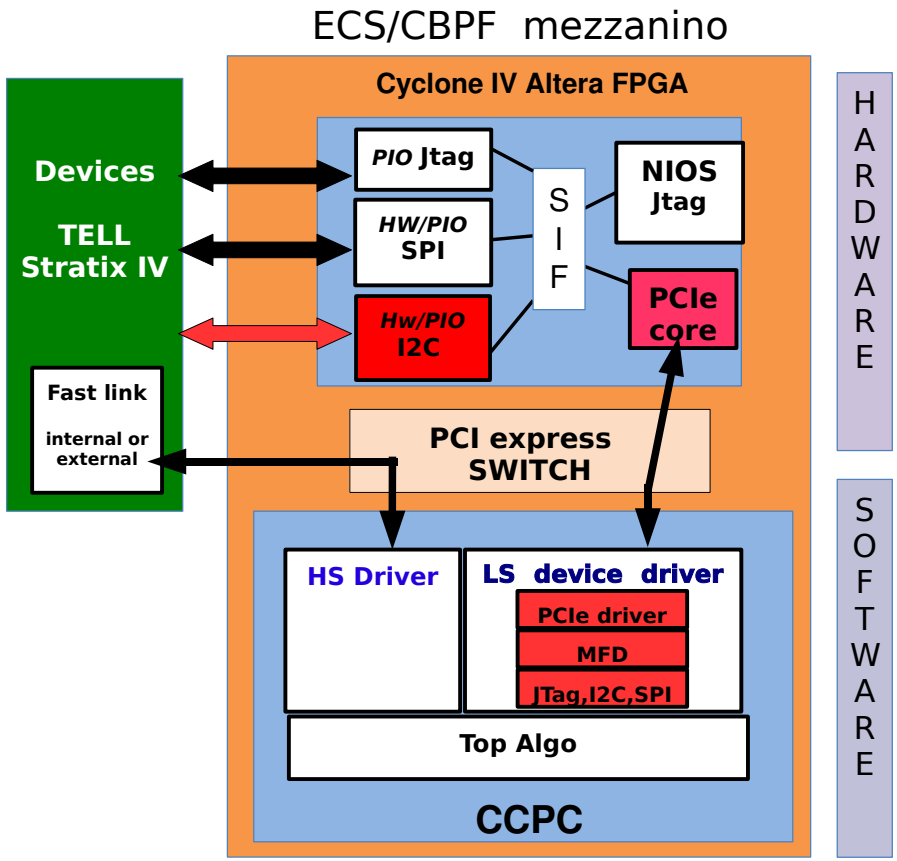


Upgraded design



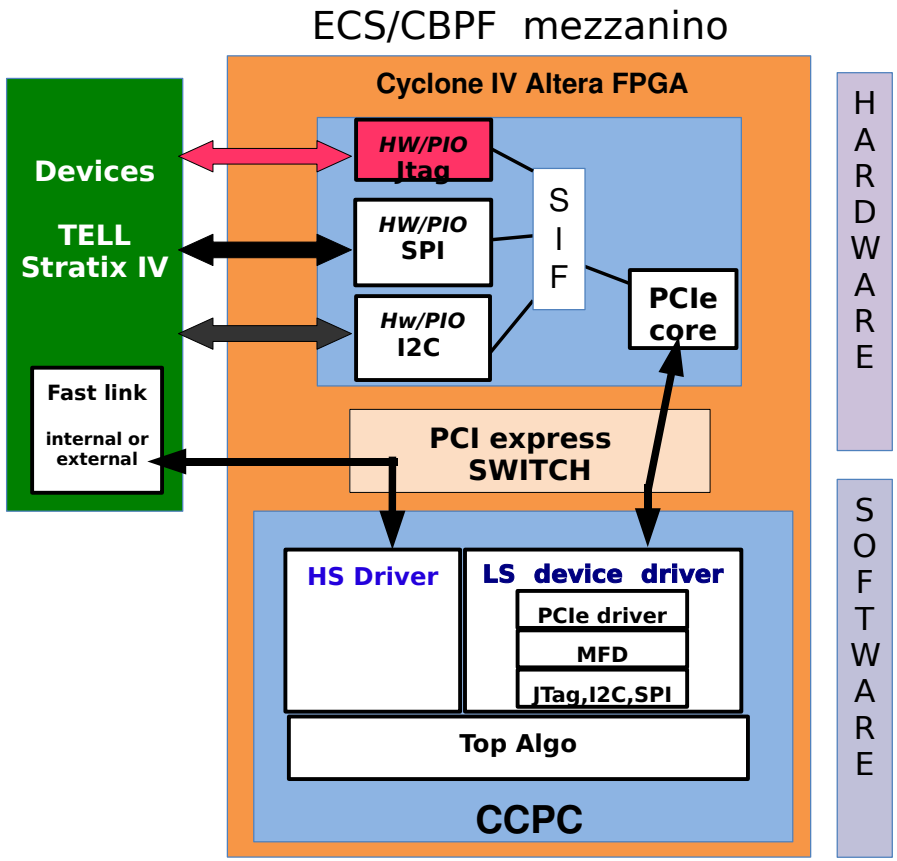
The HW & SW diagram

- The I^2C Chain is ready: for more details refer to Lessa, Niko and Beat as well as the previous talks



The HW & SW diagram

- The I^2C Chain is ready: for more details refer to Lessa, Niko and Beat as well as the previous talks
- The JTAG protocol on NIOS/JPlayer is in good shape but is is just for Altera!
- Verilog implementation of JTAG master in FPGA under investigation by Lessa: saving space in PCB and money wrt 74LVT8980 controller



The Schematic

Except the connection concerning the PCIe line

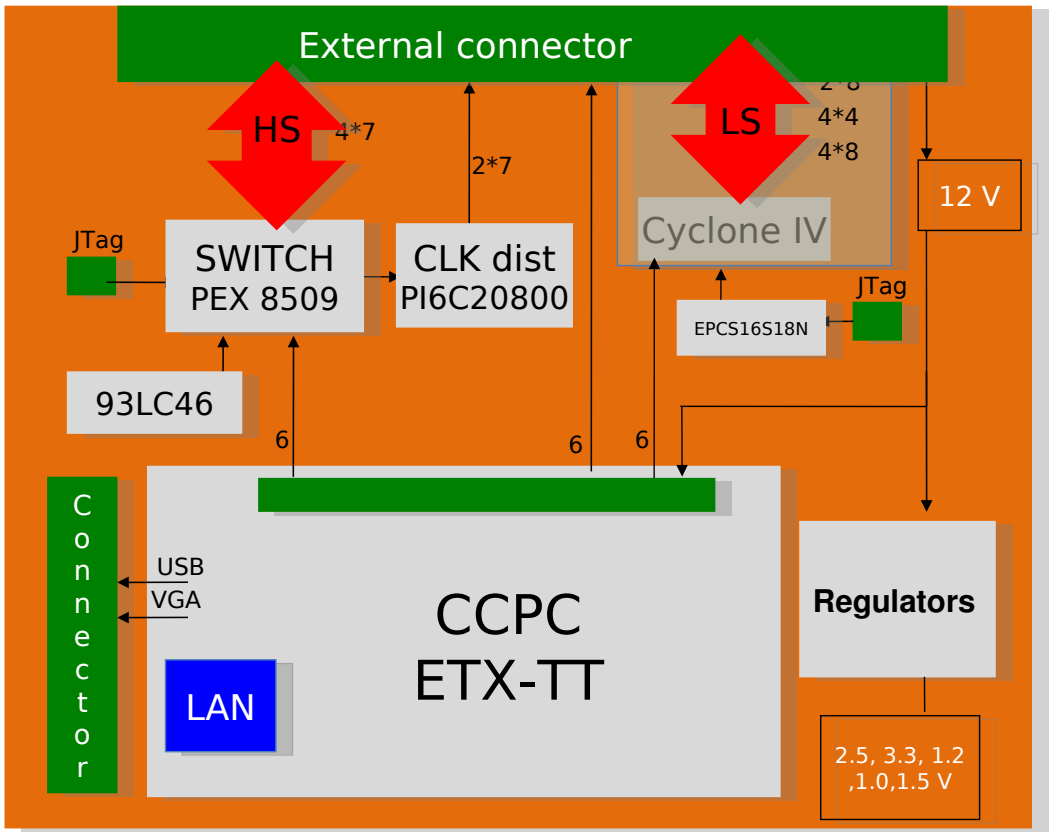
CCPC $\leftrightarrow$ Ethernet Form Factor

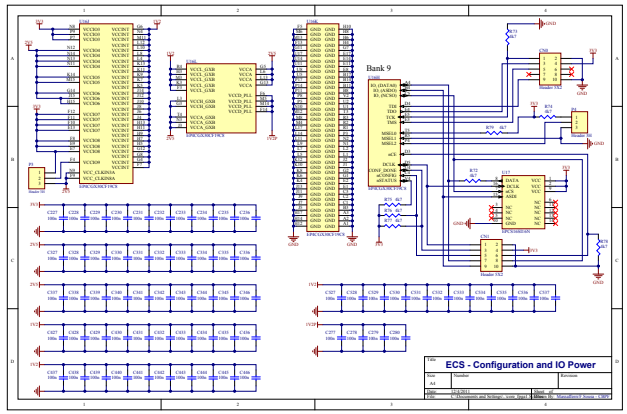
the whole schematic using SMA200 has been done

next slide: ETX-TT option

The Schematic

The Electrical schema @ALTIUM FPGA





The Schematic

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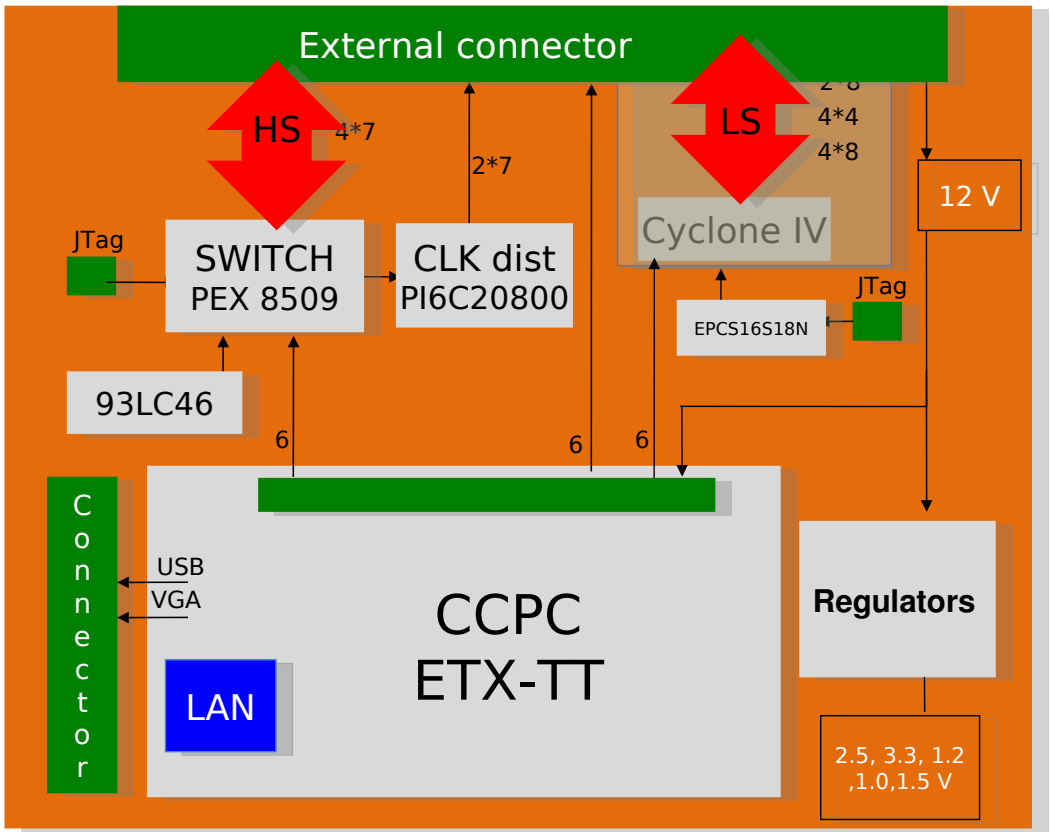

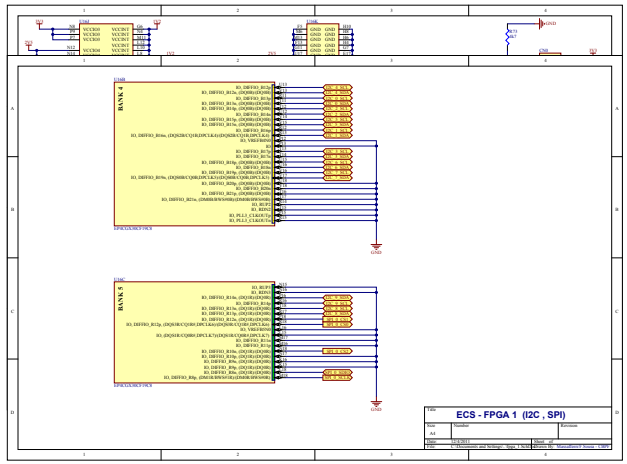

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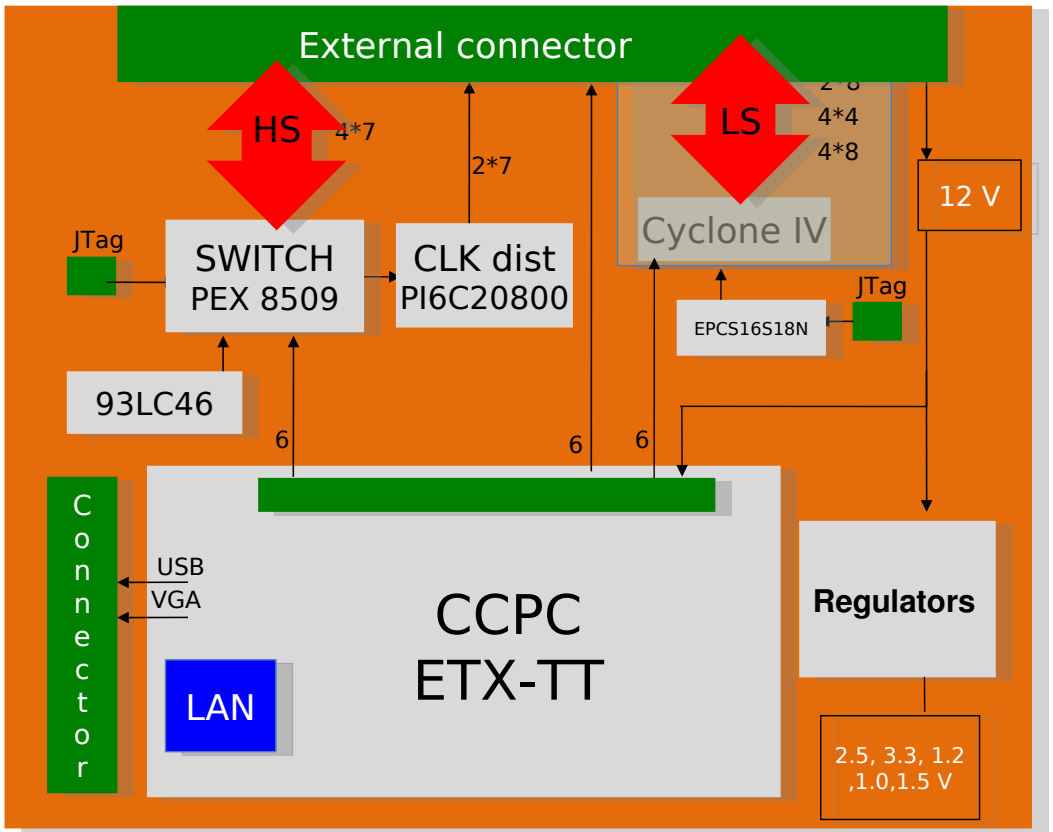

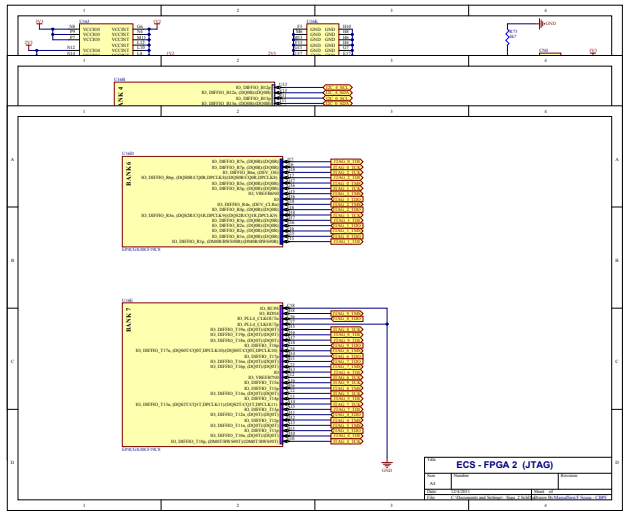

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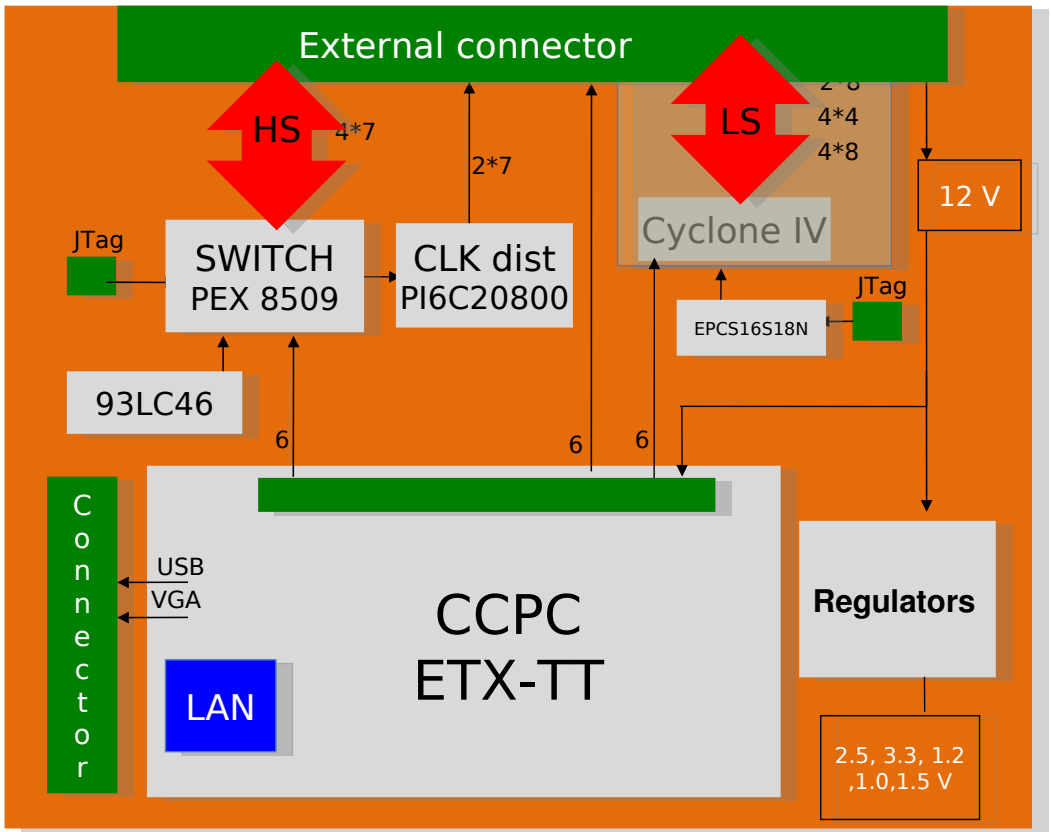
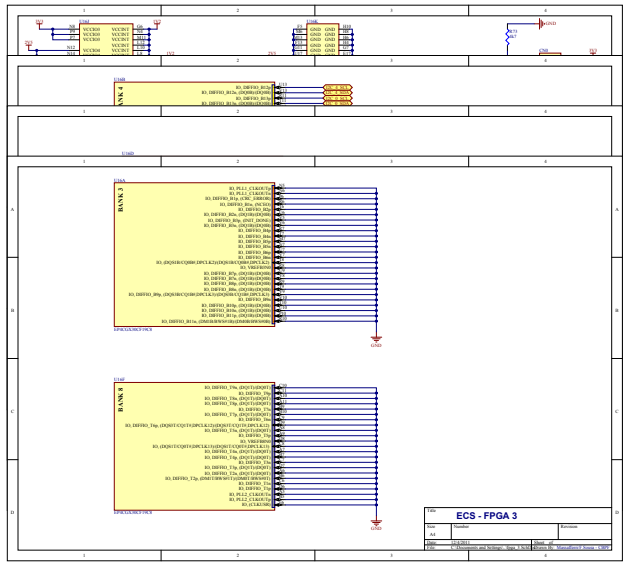
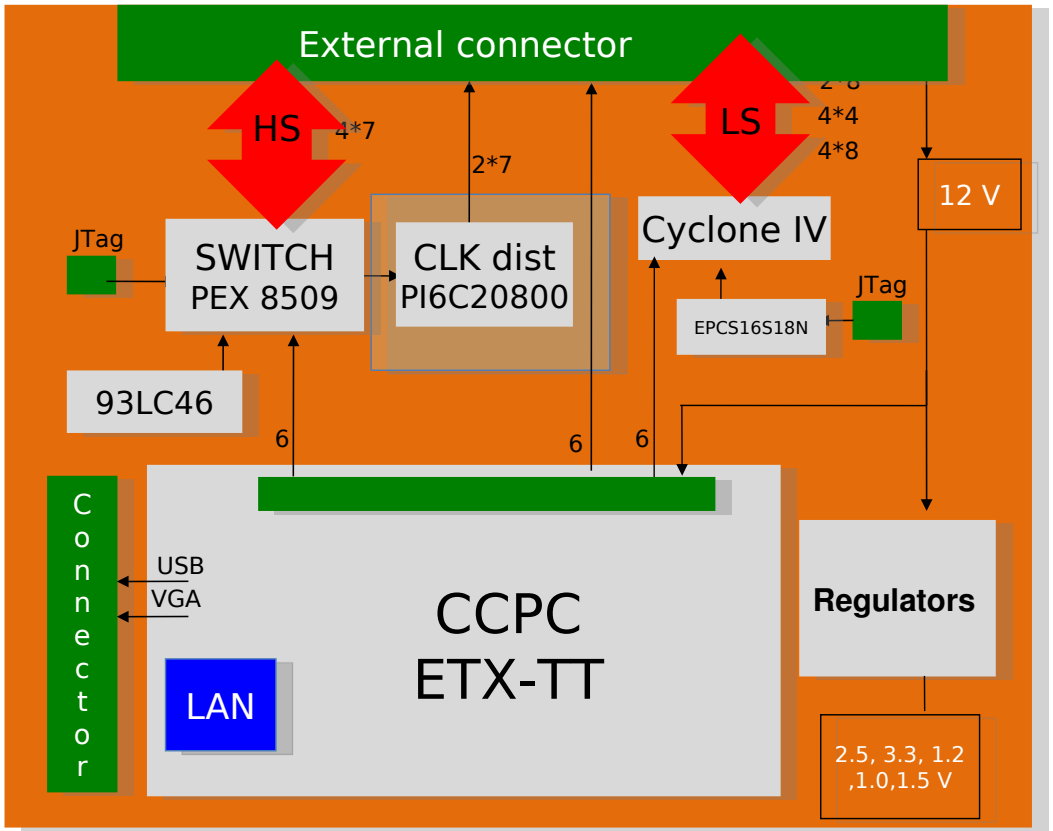
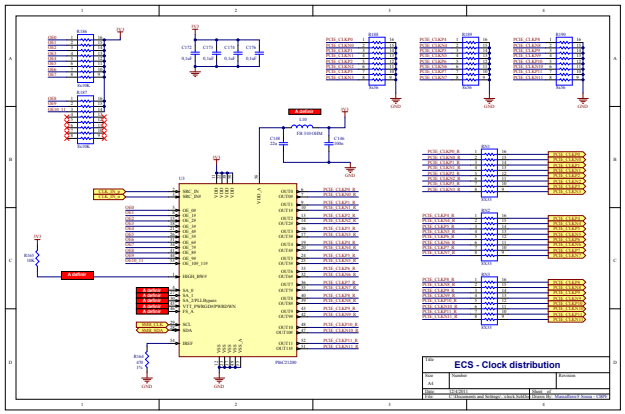




The Schematic

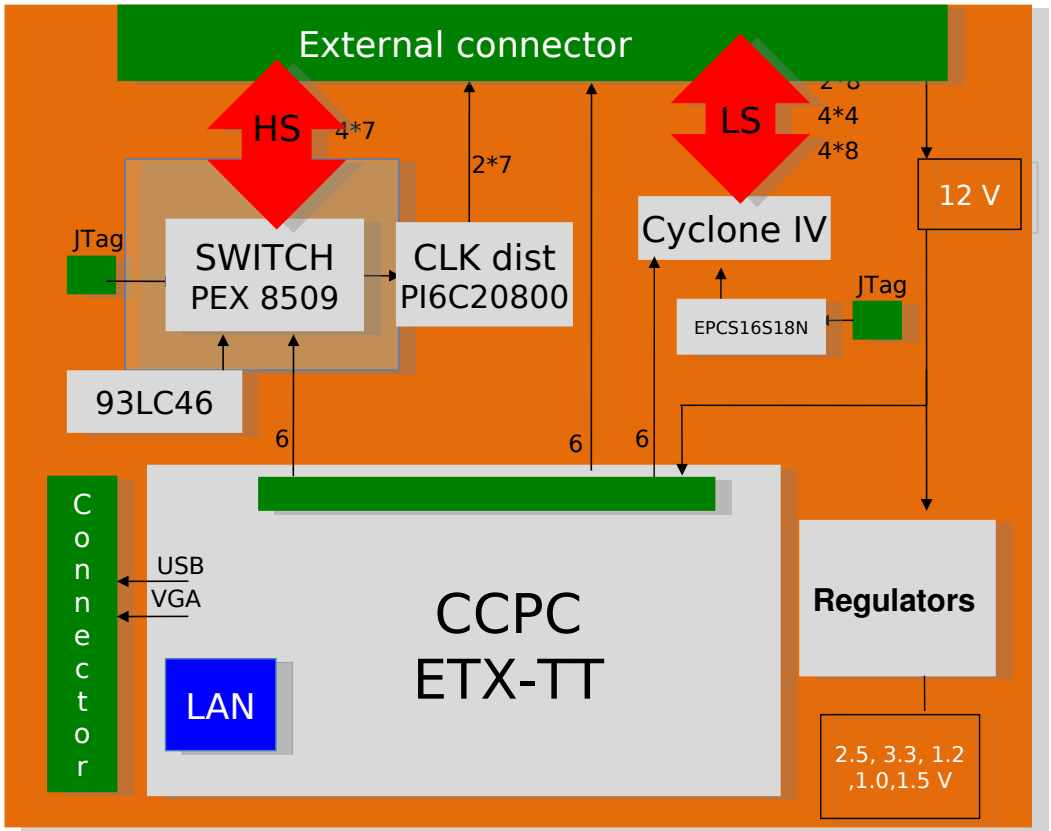
The Electrical schema @ALTIUM Clock Distribution

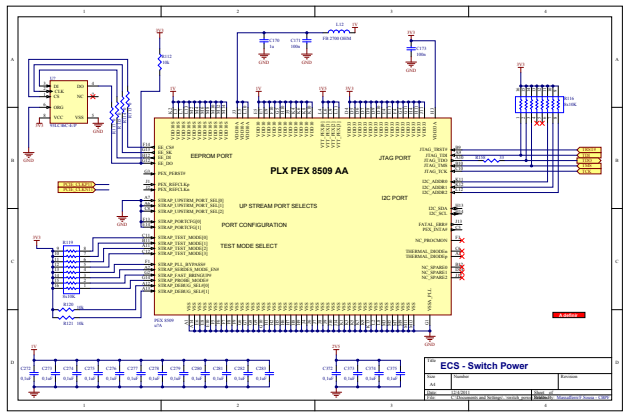




The Schematic

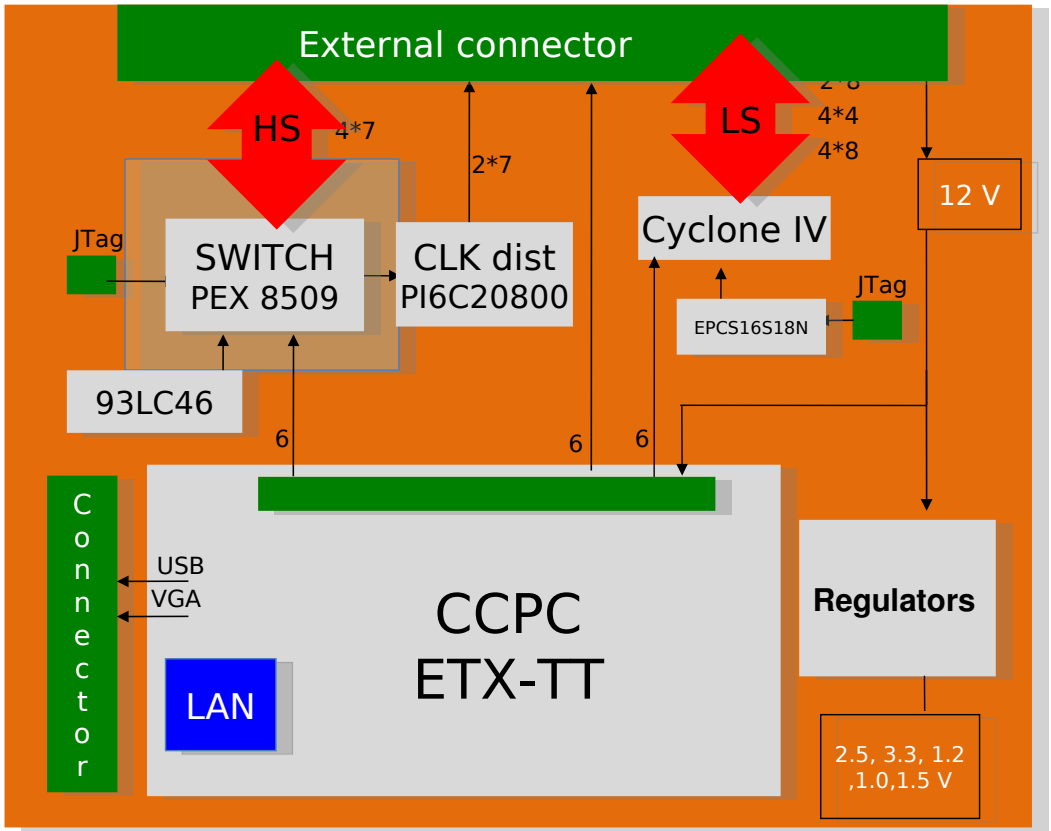
The Electrical schema @Altium Switch

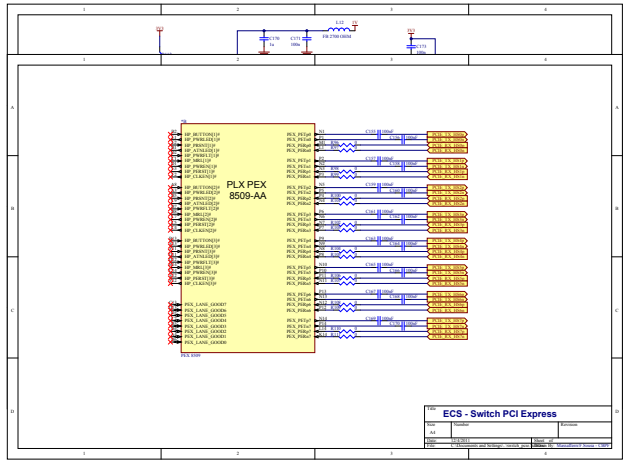




The Schematic

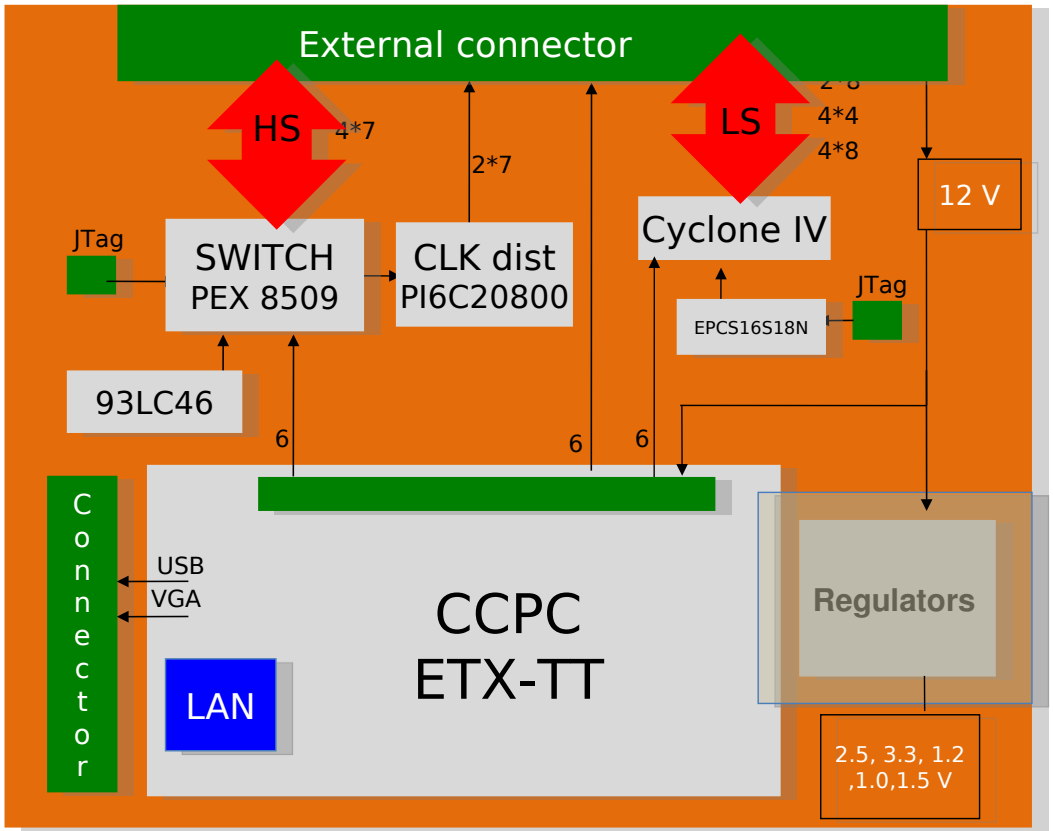
The Electrical schema @Altium Switch

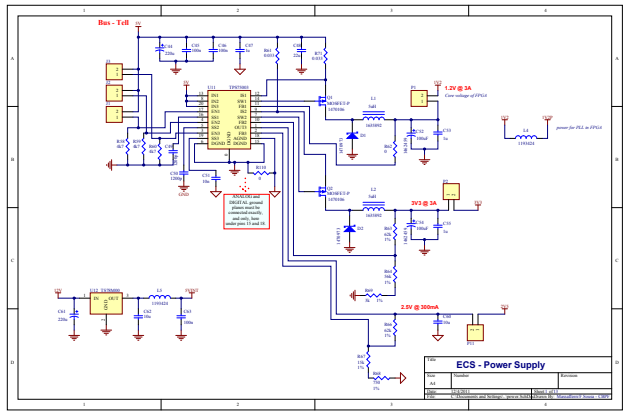




The Schematic

The Electrical schema @ALTIUM Power

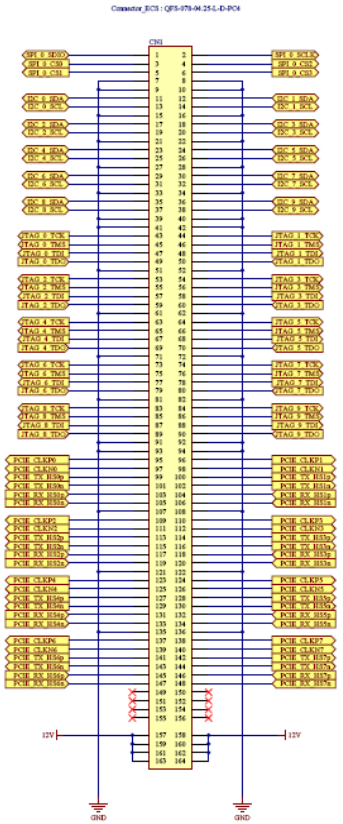




External Specs

Pinout

SAMTEC: **QFS-078-04.25-L-D-PC4**



The Geometry

- **2 VME-slots for TELL10** Guido

160 x 95 x (2*13.72) mm

- **ATCA for TELL40** Jean-Pierre

115 x 70 x 21.33 mm

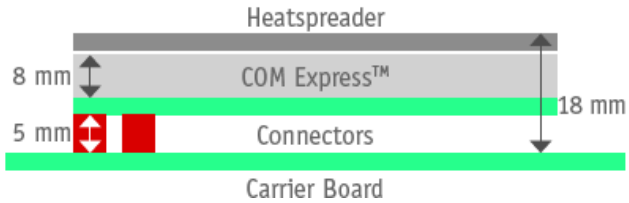
we can manage X & Y

even in the worst case

The HEIGHT is still an issue !

SMA200: 11mm

nano ETX: 18mm



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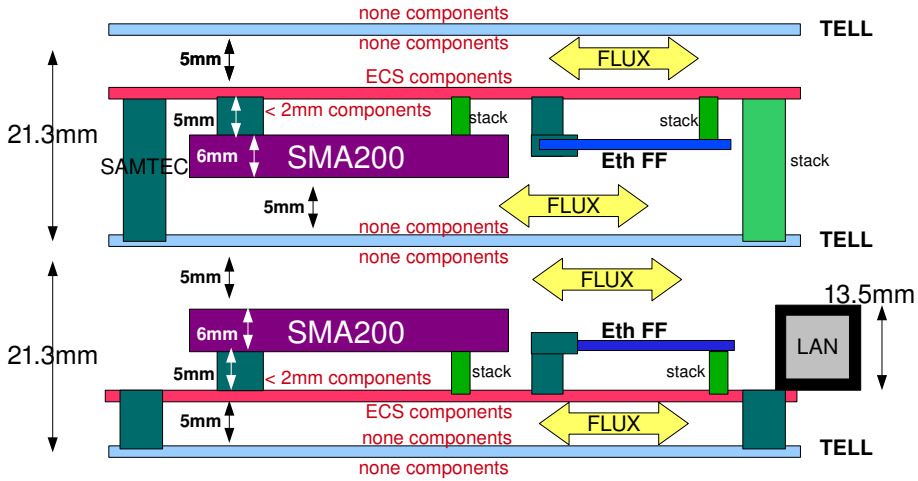

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The HEIGHT is still an issue !

I am looking for another SAMTEC **HS** connector
height $<$6mm or $>$17mm

Conclusion and Remarks

- The ECS-CBPF board is evolving on schedule.
- Low Speed Protocols: I^2C chain is ready @driver level. JTAG from JBC player has been substituted by development of controller inside FPGA
- The Schematic has been done
- CCPC+Ethernet seems to be the only place allowing new Technology before the final production of 2015. Following the suggestion of J.Pierre, I am proposing a new CCPC; ETX-TT
- Geometry: height is a concern in both options, SMA200 & ETX-TT. We will postpone this problem to the next Prototype.

Conclusion and Remarks

- SOON I will bring the 1^{st} Prototype to CERN for Testing
- PROJECTS OTHER than TELL are invited to benefit from the small production in 2012