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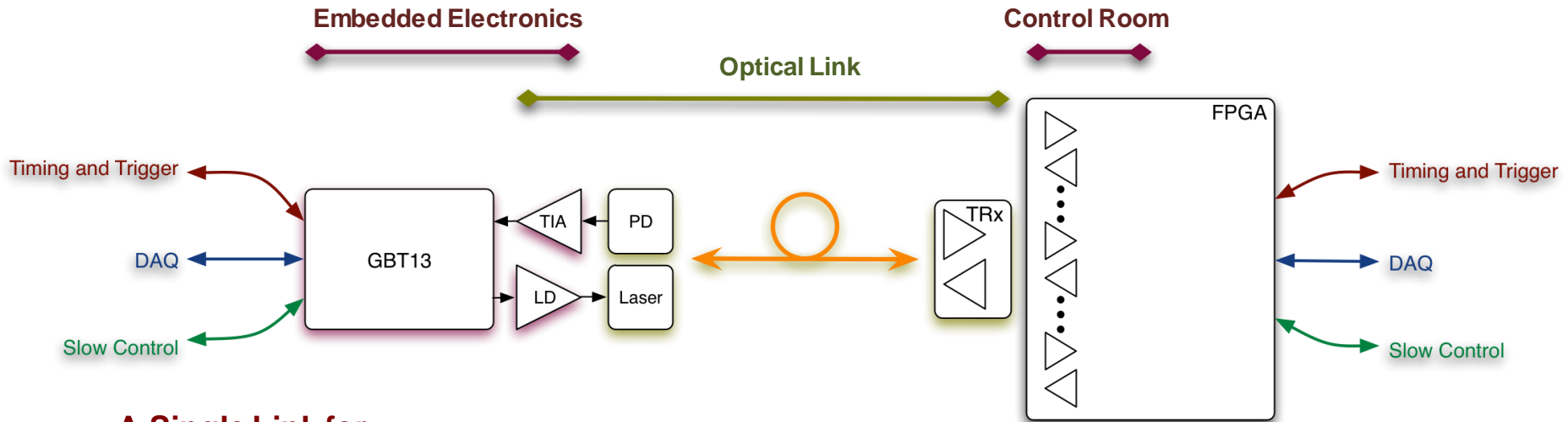
# GBT-SCA

# Slow Control Adapter ASIC

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P. Moreira, F. Sousa

LHCb Upgrade Electronics meeting  
15/12, 2011



## □ A Single Link for:

### □ Readout (DAQ)

- High speed unidirectional (up-link)
- Trigger data (up-link)

### □ Timing Trigger and Control (TTC)

- Clock reference and synchronous control (down-link)
- Trigger decisions and control (down-link)
- Low and fixed latency

### □ Experiment control (SC/DCS/ECS)

- Modest bandwidth (bidirectional link)

### □ Custom ASICs in the detectors:

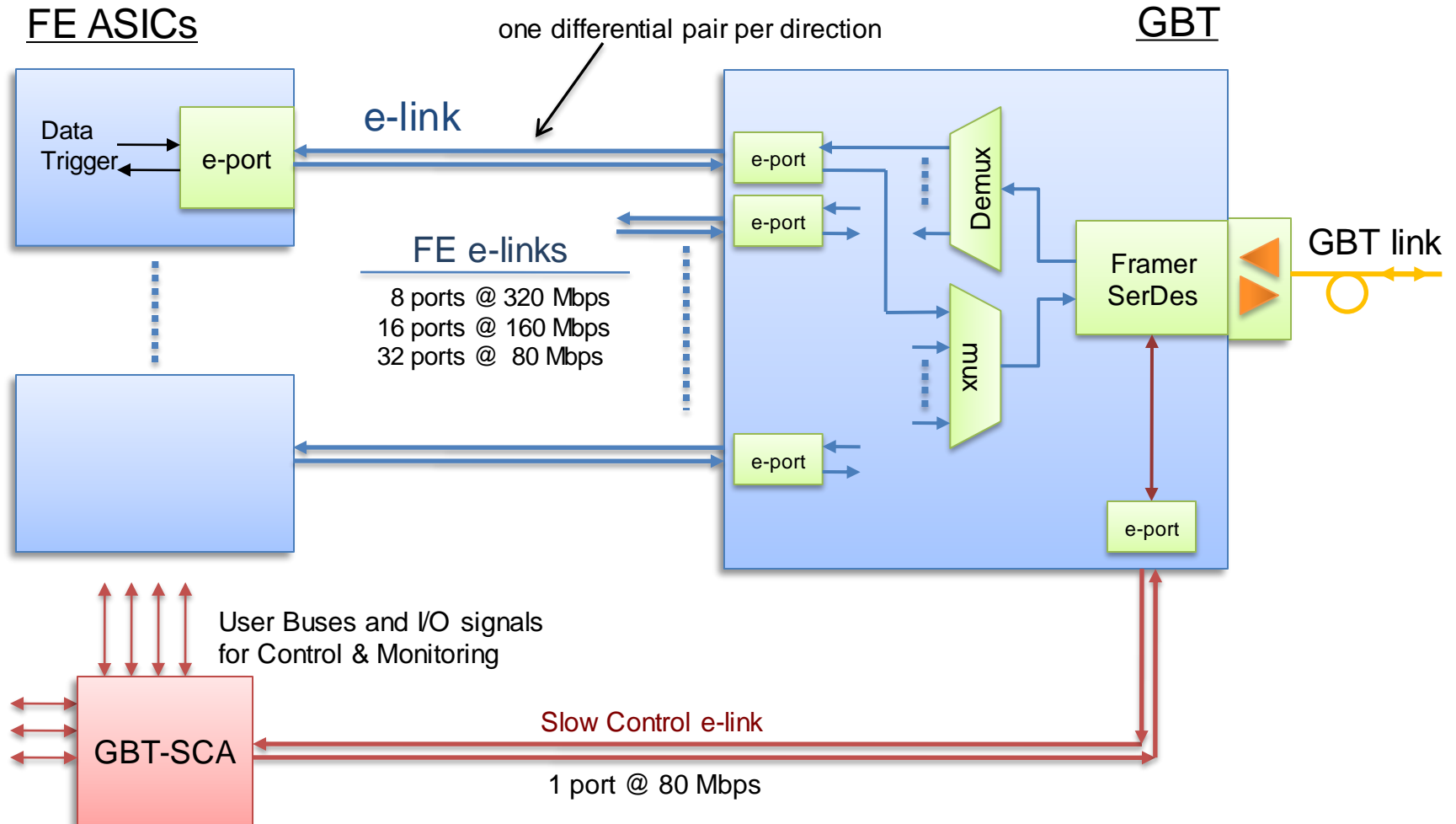
- Radiation Tolerant: Total dose & Single Event Upsets

### □ Commercial components in the control room

- FPGAs used to implement multi-way transceivers



# GBT Front End interconnects





# Design Team

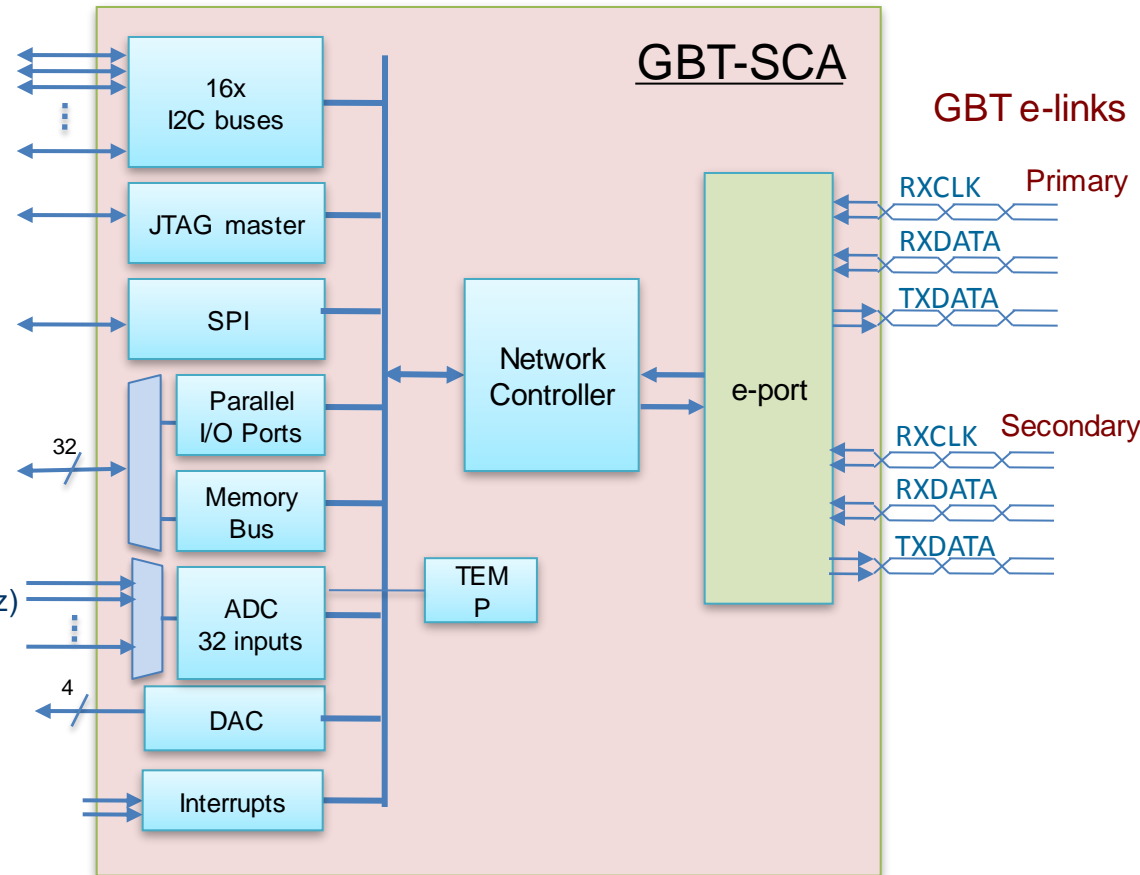
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- Core Digital Logic: *Alessandro Gabrielli*
- e-port interface: *Sandro Bonacini*
- ADC: *Filipe Pereira Alves De Sousa*
- DAC: *Xavier Llopart (Medipix-3 IP block)*
- Chip Assembly & AOB: *Kostas Kloukinas*



# The Slow Control Adapter ASIC

- ASIC dedicated to slow control functions.
- System Upgrades for SLHC detectors.
- Replacement for the CCU & DCU ASICs (CCU: Communication Control Unit DCU: Detector Control Unit in CMS).
- Flexible enough to match the needs of different Front-End systems.
- Key Features
  - Dual redundant e-Ports for GBTX e-links.
  - 16 I<sup>2</sup>C master controllers @ 100kbits/s or 1 Mbits/s.
  - 1 SPI master controller
  - 1 JTAG master controller
  - 32 multiplexed ADC channels 12-bit dual slope integrating ADC @ 3.5KHz)
  - 4 DAC channels
  - 32 Digital I/O lines individually programmable.
  - 8-bit memory bus
  - 4 Interrupt inputs
- Technology: CMOS 130nm using radiation tolerant techniques.





# Communication Architecture

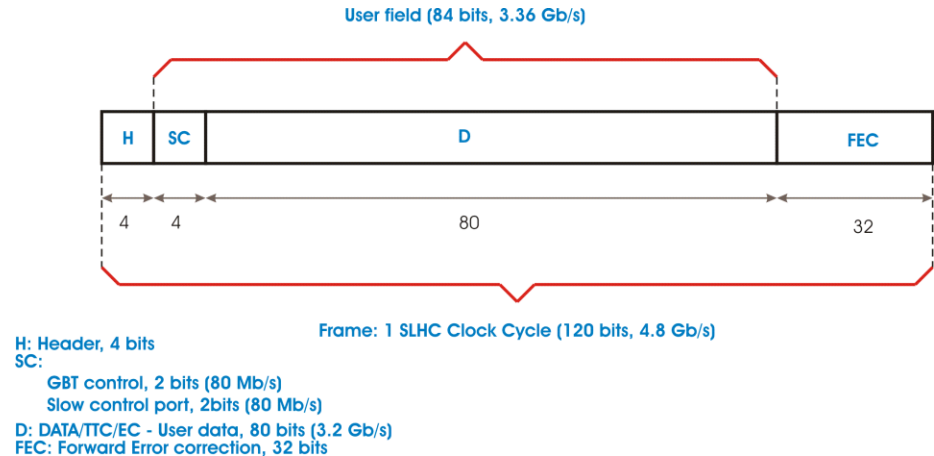
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- The Three Communication Layers of the SCA:
  - GBT-link Layer
    - Connects the GBT ASIC to the Control Room electronics via a point-to-point, bi-directional, 4.8Gbps, optical link using a special, SEU robust, transport protocol.
    - The transport protocol is totally transparent to the user data.
  - e-link Layer
    - Connects the GBT to the SCA ASIC via a point-to-point, bi-directional, 80Mbps, electrical link using a packet oriented transport protocol.
    - Data packets are encapsulated by the GBT-link protocol.
  - Channel Layer
    - Connects the SCA to the Front-End ASICs via multidrop, bi-directional, 100Kbps-1Mbps, electrical links, via the so called “Channel Blocks”.
    - SCA on-chip peripherals (ADC, DAC, PIAs, etc) are also Channel Blocks.
    - Channel Blocks are controlled via a command driven protocol.
    - The Channel Protocol Commands are encapsulated by the e-link protocol.



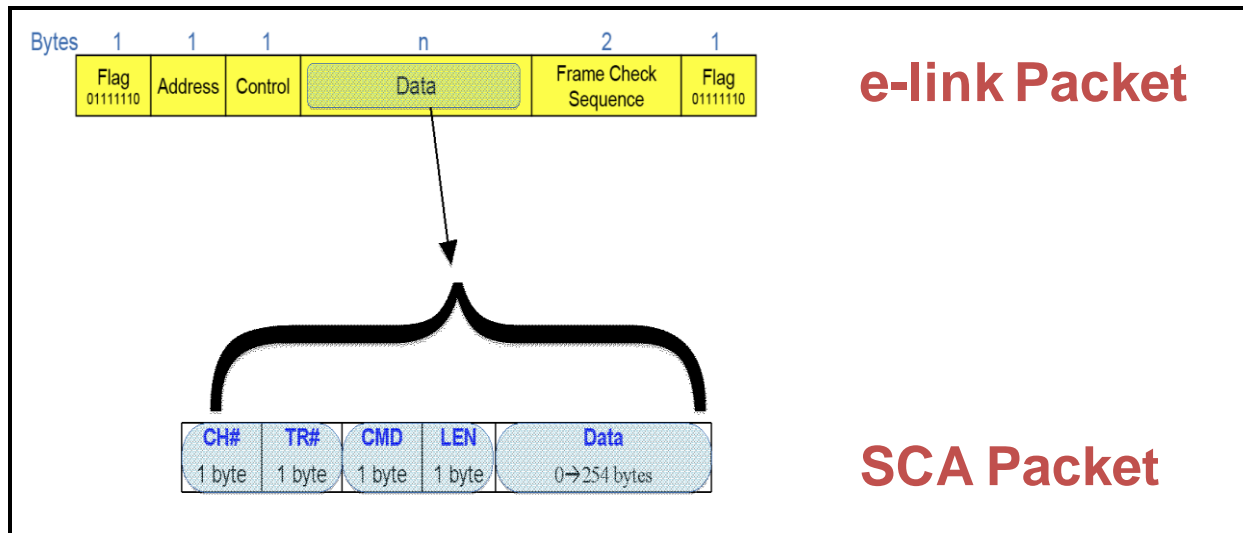
# GBT-link Packet Format

- Fixed packet length: 120bits
  - Packet transmission rate: 1/25ns
  - Data transmission rate: 4.8 Gbps
- Fixed bandwidth allocation:
  - Trigger path: 640 Mbps
  - Control path: 160 Mbps
    - 1 internal e-link (for GBT management)
    - **1 external e-link (for GBT-SCA chip)**
  - Data path: 2.56 Gbps
    - 8 e-links @ 320 Mbps
    - 16 e-links @ 160 Mbps
    - 32 e-links @ 80 Mbps
- Data flow:
  - Symmetrical, Bi-directional data transmission.
  - Transmission of GBT-packets is continuous.
  - Data from e-link ports are muxed/demuxed in the GBT-link stream.
  - GBT data path is unaware of the e-link transfer protocol.





# e-link & SCA Packet Formats



- **FLAG:** Frame delimiter character.
- **Address:** Packet destination address.
- **Control:** Indicates the type of the data packet.
- **FCS:** Frame Check Sequence for transmission error detection.
  
- **CH#:** (Channel ID) specifies the SCA Channel Block to be addressed – i.e. I2C, JTAG, NC, Monitor, etc. -,
- **TR#:** (Transaction ID) incremental identification number for each transmitted command.
- **CMD:** is a command code that specifies a given transaction. The operation can refer to a specific internal register of the channel – i.e. a configuration register – or a front-end ASIC destination address. In this case an address field follows the command.
- **LEN:** is a field that ranges from 0 to 255 that specifies the **DATA** field length. For read commands **LEN** is 0,
- **DATA:** is an optional variable length field upon **LEN** value.



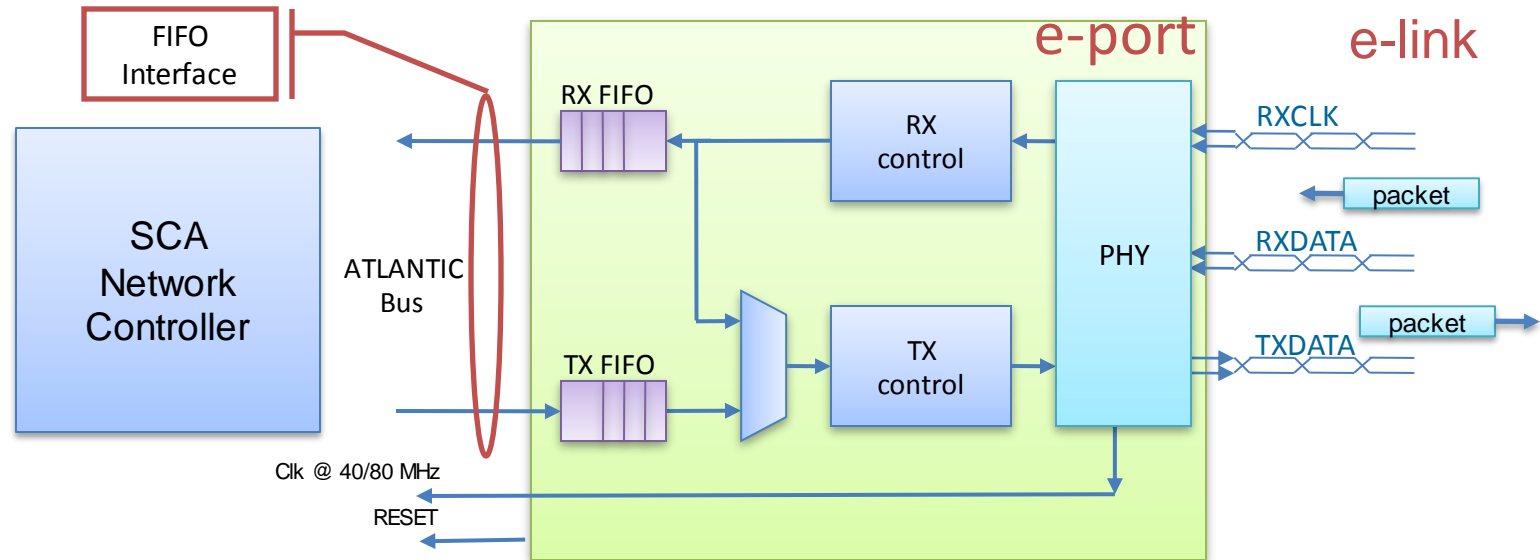


# Channel Block Commands

- Channels receive commands from the network controller and perform actions on the bus to which they connect as masters.
- These commands are contained in the data field of the packet.
  - The data content of a given packet is interpreted differently according to the channel to which it is addressed.
- Each channel type has a set of valid commands;
  - Channels receiving an invalid command do not execute any action and they report the error condition to the network controller.
- Upon reception of a command, a channel performs the required operation on its interface.
  - Depending on the particular command it can then return a reply to the network controller as a data block which will be transmitted to the control room electronics via the e-link.
- Example of I<sup>2</sup>C Channel Commands:

Command	CMD [hex]	Command and Reply Format
Single byte write normal mode	0x00	<b>C:</b> CH#+TR#+CMD+A7+DW <b>R:</b> none or CH#+TR#+ACK
Single byte read normal mode	0x01	<b>C:</b> CH#+TR#+CMD+A7 <b>R:</b> CH#+TR#+DR+ACK

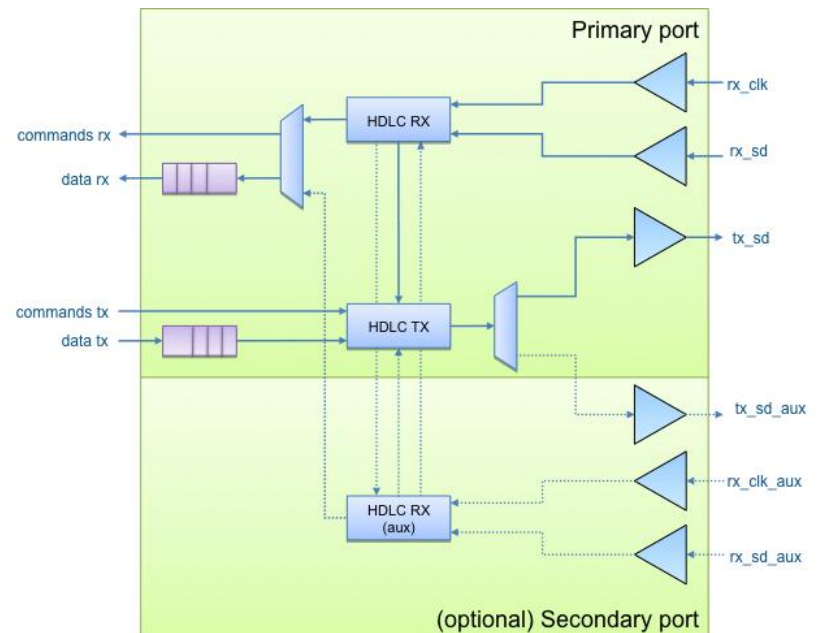
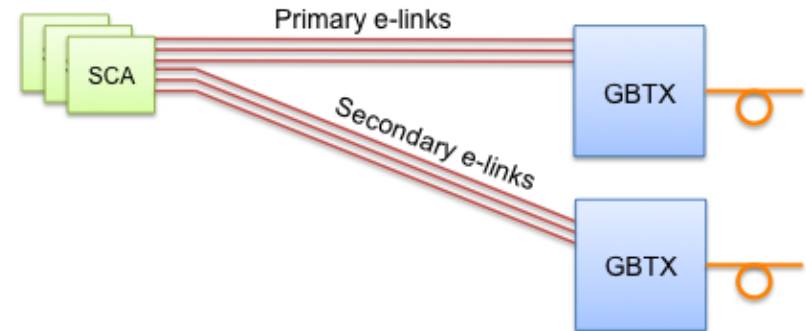
# e-link & e-port Block Diagram



- e-port implementation for the GBT-SCA
  - e-link interface: electrical, bi-directional chip-to-chip interconnect at 80Mbps.
    - Support for Manchester encoded data (at half data bandwidth) for AC coupled e-links.
  - HDLC (High Level Data Link Control) packet oriented communication protocol.
  - Special commands: CONNECT, RESET, TEST (loopback)
  - Acknowledge transactions using the HDLC protocol mechanism (packet numbering).
  - Altera (open core) ATLANTIC bus to interface with internal logic (Network Controller).

# Dual Redundant e-ports

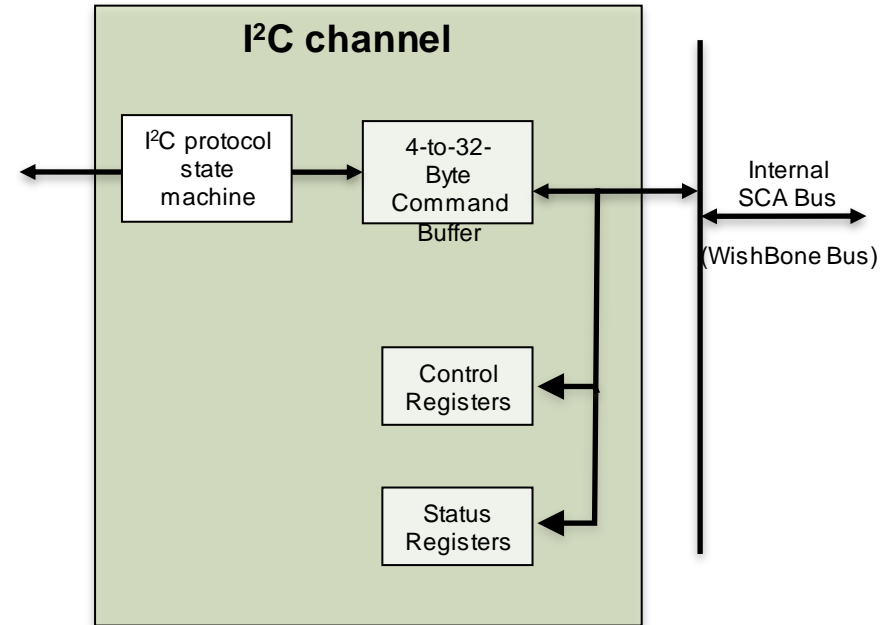
- A GBT-SCA chip can connect with two adjacent GBTX chips for redundancy.
- The GBT-SCA chip is equipped with a Primary and a Secondary e-port.
- Only one e-port is needed for operation.
- Only one e-port can be active at a time.
- Data from the inactive e-port is discarded.
- Switching between ports is command driven. (HDLC “CONNECT” command)
- Clock activity (or noise) on the “rx\_clk” input of the inactive port is discarded.
- Upon start up, the user application software should send a “CONNECT” command to activate the Primary e-port from the Primary e-link.
- To switch to the Secondary e-port a “CONNECT” command should be send through the Secondary e-link.





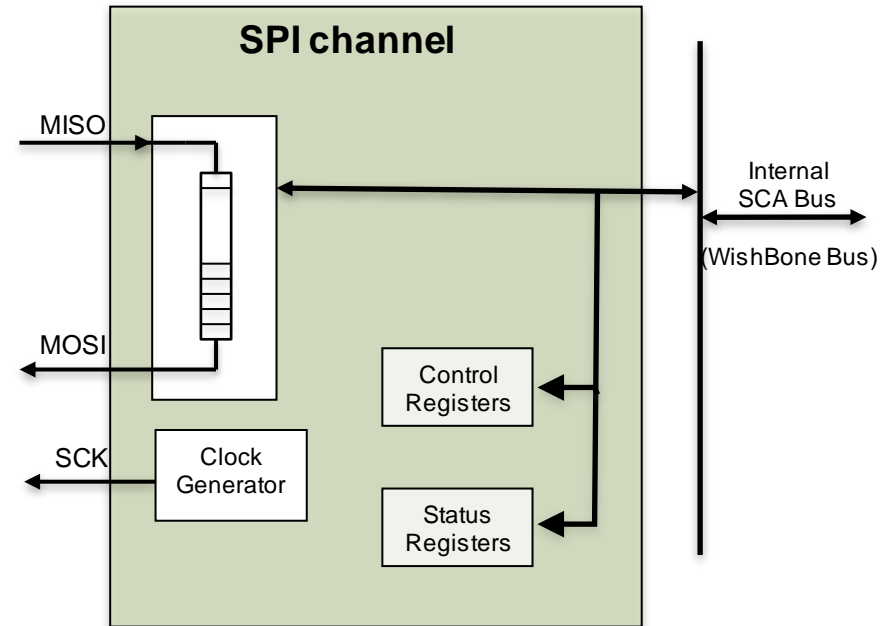
# The I<sup>2</sup>C port

- 16 independent I<sup>2</sup>C master channels
- Concurrent operation of all 16 channels
- Support is limited to single bus master topologies.
- 7-bit and 10-bit addressing modes.
- Single-byte and Multi-byte transfer modes.
- Read-Modify-Write mode that allows for AND, OR, XOR logic operations with a Mask register.
- Programmable transfer rate from 100Kbps to 1Mbps.
- Power Down mode per channel



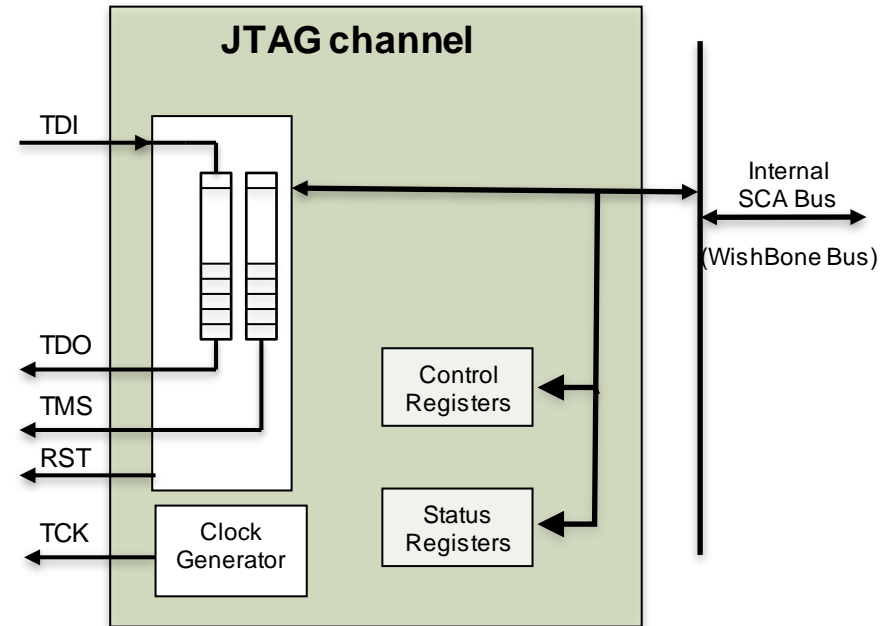
# The SPI port

- Synchronous byte oriented serial link.
- Full duplex mode
- Programmable transfer rate from 1Mbps to 10Mbps.
- RW commands composed of 8/16/32 bits
- Power Down mode



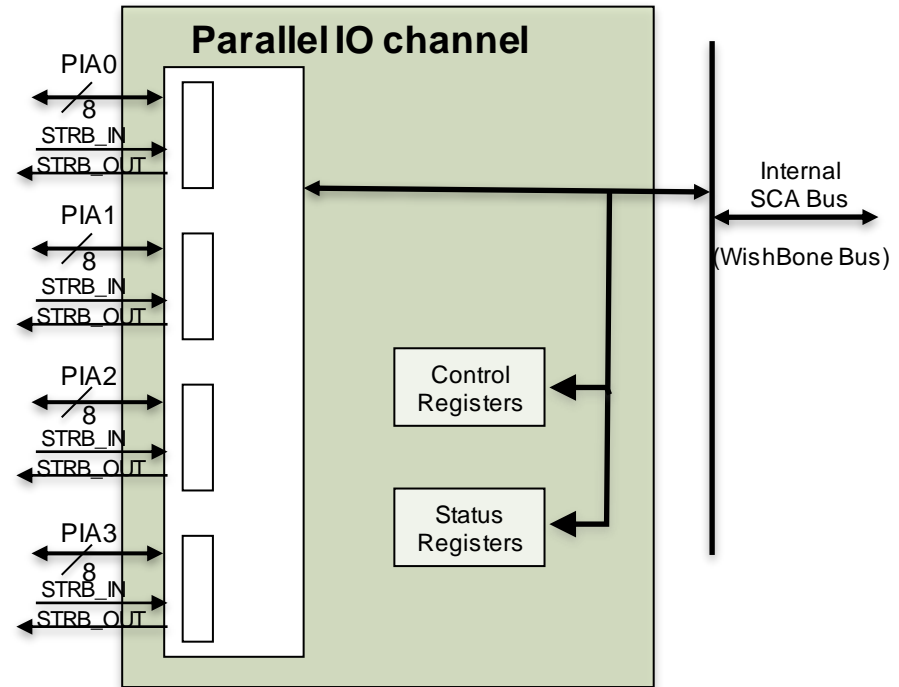
# The JTAG port

- Simplified implementation of a JTAG controller.
  - Two 128 bit shift registers to hold the TDO/TDI and TMS bit-streams.
  - Protocol implemented in software.
- Programmable transfer rate from 1Mbps to 10Mbps.
- RW commands composed of 256 bits in 128 pairs of (TMS/TDO)
- Power Down mode



# The Digital Parallel IO port

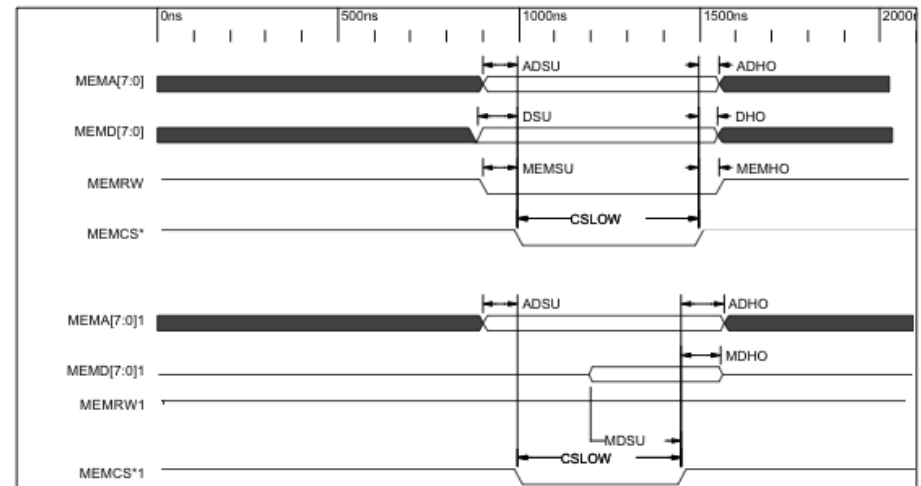
- Similar functionality to a Motorola PIA (Parallel Interface Adapter)
- 4 independent 8-bit wide ports with programmable data direction.
- Static IO operation or
- Strobe IO operation (using STRB\_IN, STRB\_OUT)
  - Interrupt driven transactions
- Power Down mode





# The Memory Port

- Simple memory-like interface
- Uses the same pins as the Parallel IO port
- 16 bit Data
- 16 bit Address
- Read/Write line
- Strobe line
- Commands:
  - Single (16-bit) Read
  - Single (16-bit) Write

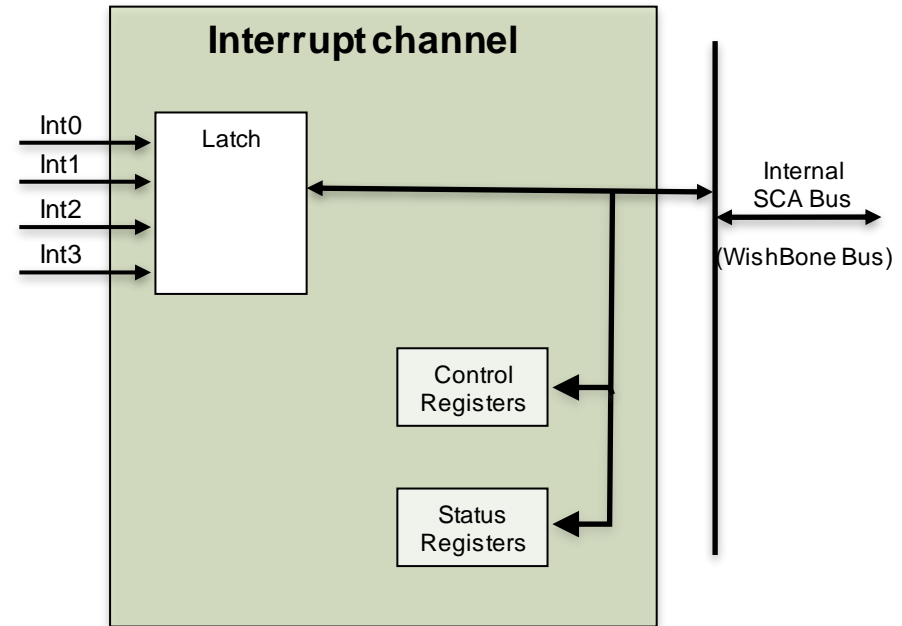


Note that this slide shows an 8-bit address/data bus.  
The actual hardware implementation is 16-bit address/data bus.



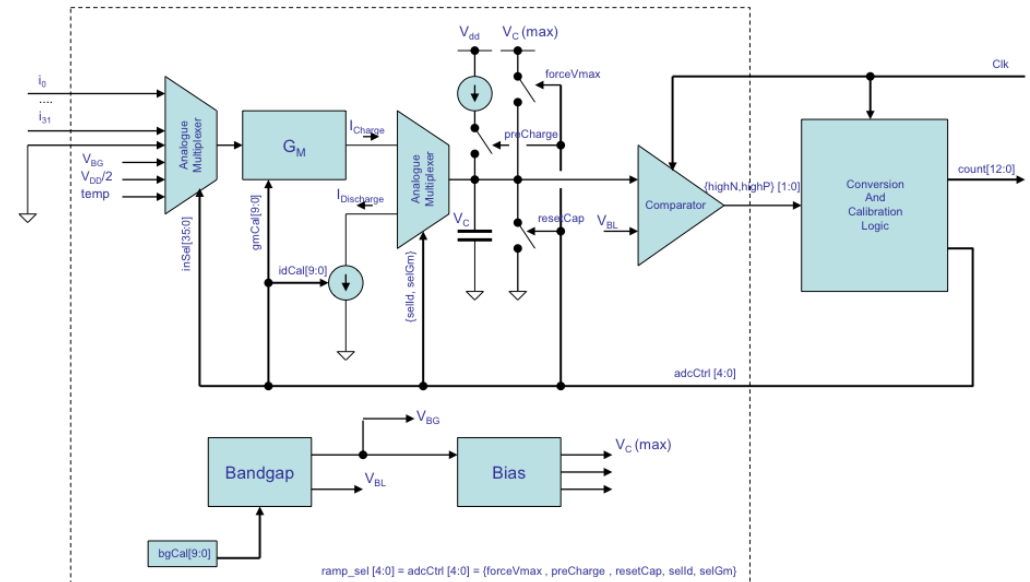
# The Interrupts

- 4 independent interrupt input signals
- Edge sensitive (High to Low transitions)
- Can be used to generate and transmit a special “interrupt event” packet to the remote control system.
- The interrupt inputs are edge sensitive.



- 12-bit ADC (LSB = 244  $\mu$ V)
- Dual-slope architecture
- Input range: GND <  $V_{in}$  < 1 V
- Single supply voltage: VDD = 1.2 V
- System clock frequency: 40 MHz
- Max. conversion rate  $\approx$  3.5 KHz
- Max conversion time  $\approx$  250  $\mu$ sec)
- Operating temperature: -30° C to +80° C
- 32 Multiplexed Input channels
- 1 channel occupied by an on chip Temp sensor
- All channels feature a switchable 10  $\mu$ A current source to support Pt sensors.
- Internal bandgap reference circuit.
- Power consumption  
350uA @ 1.2V (420uW analog part )
- Power Down mode

## Architecture

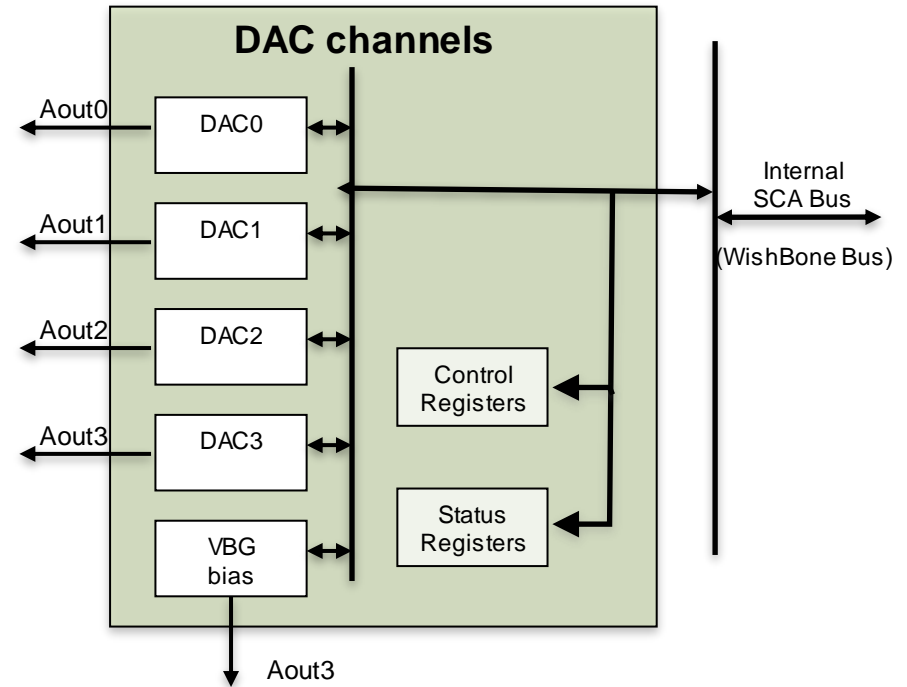


GBT-SCA-ADC

Design Review - 2010/III/10

8

- There are 4 independent DAC channels.
- Voltage output: 0V - 1.5V (preliminary specs)



## ■ Documentation:

- ❑ Short “Specifications” document (draft)
- ❑ Long “Users Manual” document (draft)

### GBT-SCA: Slow Control Adapter for the GBT system.

#### General Description

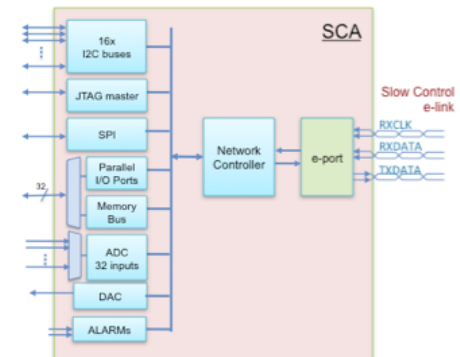
The GBT-SCA is an ASIC for control and monitoring of the embedded front-end electronics for the particle physics detectors. It is targeted for system upgrades for the SLHC detectors where can be considered as a replacement for the CCU & DCU ASICs. The GBT-SCA implements multiple protocol serial and parallel communication interfaces with the front-end ASICs as well as analog inputs and outputs for environment parameter monitoring. It connects electrically to a communication ASIC, the GBT, to form long distance optical networks. It is built in a CMOS 130nm process using radiation tolerant design techniques.

#### Features

- 1 e-Port for GBT
- 16 I<sup>2</sup>C master controllers @ 100kbits/s or 1 Mbits/s.
- 1 SPI master controller
- 1 JTAG master controller
- 32 Analog Inputs
- 1 Analog Output
- 32 Digital Inputs or Outputs individually programmable.
- 1 8-bit memory bus
- 4 Alarm inputs

#### Key Specifications

Supply Voltage: +1.2V  
 Power Dissipation: x00mW  
 Operating Temp.: -10°C ~ +50°C  
 ADC resolution: 12-bit @ 3.5KHz  
 DAC resolution:  
 Technology: CMOS 130nm  
Radiation Tolerant design.





# Status & Plans

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- Design Work Status
  - Digital Core Logic RTL design (**on going**)
    - All interfaces are designed.
    - Top level Simulation test bench is ready.
    - Functional verifications (data flow control & exception handling)
  - ADC IP block (**on going**)
    - IP integration
  - DAC IP block (**on going**)
    - IP integration
  - e-port IP block & SLVS IO pads (**Ready**)
  - Design implementation:
    - Triple Module Redundancy for SEU tolerance (**on going**)
    - Low power techniques (clock gating)
    - Floorplanning
    - Physical Verification
  - **Target Tape-out date: May, 2012**



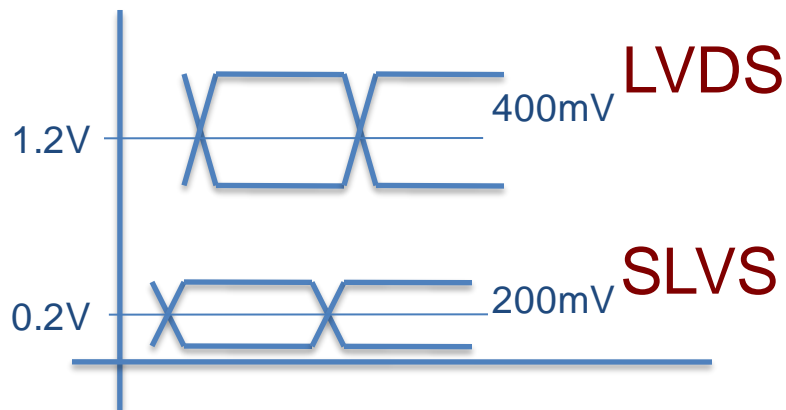
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THANK YOU



# Physical Layer (electrical)

- **SLVS (Scalable Low Voltage Standard)**
  - JEDEC standard: JESD8-13
  - Differential voltage based signaling protocol.
    - Voltage levels compatible with deep submicron processes.
    - Typical link length runs of 30cm over PCB at 1Gbps.
    - Low Power, Low EMI
  - Application in data links for Flat Panel displays in mobile devices.
    - Mobile Pixel Link, MPL-2 (National semi.)



## SLVS specifications

### brief

2 mA Differential max

Line impedance: 100 Ohm

Signal: +- 200 mV

Common mode ref voltage: 0.2V

# Resets on GBT-SCA

