LHCb Electronic upgrade Dec 15, 2011 CERN

Readout board form factor

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ATCA

Standard for application with:

- High throughput
- High level of integration
- High level of reliability

A standard specifying elementary blocks for:

- Mechanics
- Backplane for power supplies and point-to-point high speed links
- Control and Cooling

Used in:

- Telecommunication
- Data centre (networking)
- High energy physics (XFEL, Belle-2, ITER,...)

The natural choice for the LHCb readout board.

Controversy

- ATCA implementation breaks the rule "Re-use existing electronics and infrastructure as much as possible" since TELL1 crates (90 VME) will be replaced by ATCA crates.
- The same functionalities can be obtained using the current TELL1 crates since time and throttle signals can be distributed using optical cables:



ATCA / 9U VME comparison

- Architecture
- Board
- Crate and power supplies
- Infrastructure
- Cost
- Low level controls for a crate
- Reliability
- Possibility of evolution
- Test bench for early user
- Long term maintenance

Readout Architecture

Neutral with respect to the board form factor:



From F. Alessio, LHCb upgrade data processing mini workshop, 16 – 17 Nov, 2011

Board

ATCA

- 322×280 mm×mm
- 250 Watt (FPGAs full)
- 48 V / 5.2 A

▶ 9U VME

- 400×367 mm×mm

- Larger PCB by 8 cm in *h* and *w*
- Additional electric/optic converter for TFC signals

Crate and power supply

- ATCA crate from Schroff
 - 14 slots
 - 200, ..., 400W per slot

- 90 VME crate from Wiener
 - 20 slots
 - 100 W per slot

- Only 10 boards per crate

- Need: 48 V / 73 A
- PS: 48 V / 100 A (350W)

- Need: 48 V / 52 A
- PS: 3.3V/200A, 5V/100A, 48V/12A
- Replace power supply
 5 modules 48V/12A
 3.295 k€

Infrastructure modifications

ATCA

- Crate height 13U
- Modify the rack
- Vertical air flow
- Rack power dissipation 7 kW

90 VME

- Crate height 11U
- Vertical air flow
- Rack power dissipation 5 kW

NOTE:

- LEP rack power dissipation \leq 10kW
- General cooling should be enough

Crude cost estimated

ATCA

- 15 to 17 crates (1)
- 5.3 k€ per crate

90 VME

- 19 to 21 crates (1)
- 3.3 k€ per power supply
- 1.6 k€ / crate for optical transceivers and fibres
- ?? due to larger PCB

- ∑crates = 80 - 90 k€

– Σcrates = 97 – 103 k€

Similar cost for the two solutions

(1) include partitioning but depends on the ratio of TFC+ECS board with respect to TELL40 boards, The number of GBT links, the number of GBT and 10 GbE links per AMC, the load of 10 GbE links, ...

Low level control for crate

ATCA

- IPMI controller
- Ethernet (distributed)
- Switch ON/OFF crate
- Monitor voltage, current, temperature and fan speed
- Reset individual CCPC
- Switch ON/OFF board
- Off-the-shelf software from Annecy

90 VME

- OPC server
- CAN bus (daisy chain)
- Switch ON/OFF crate
- Monitor voltage, current and fan speed
- Reset individual CCPC (?)

Reliability

ACTA

- Redundant power supply
- Less fragile connections
- Excellent mechanics pour insert/extract a board
- Distributed architecture for the low level control

▶ 9U VME

Possibility of evolution

ATCA

rely on the interconnection matrix between boards via point-to-point high speed serial links embedded in the backplane and to the FPGAs computing power

Allow to build unforeseen applications which might help us in the future:

- New LLT for VELO tracking
- Compute tracking primitive to help the tracking algorithm running in the farm

90 VME

Test bench for early user

Independent of the readout board form factor. Require a table, power supply, big fan, PC and a clock generator.



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Long term maintenance

ATCA

 Contract for maintenance has to be setup by the CERN electronics pool

▶ 9U VME

- Maintenance of power supplies are under contract via the CERN electronics pools
- Contract expires in 2018 but will be renewed.

Proposal

- ATCA is better adapted to the readout board requirements.
- Propose ATCA as a baseline and 9U VME as a backup. The first prototype merges all together envisaged technologies:
 - Develop a readout board compliant ACTA standard
 - Buy and ATCA crate
 - Validate TFC distribution and the low level crate control

End 2012, when the prototype is fully debug, review this choice:

- We can modify rather quickly the board form factor when designing the preserie version.
- Better understanding on the dimension of the readout system
- See Evolution of CERN / POOL, Atlas, ...
- This approach allow to tests envisaged technologies up to the end. It minimizes the risk since early users will program FPGAs and are not sensitize to the board form factor.