CCPC-ECS (brief status)

&

A Tester for the OT FE Electronics

André Massafferri & Antonio Pellegrino

Rio de Janeiro, 15-12-2011

- CCPC-ECS
  - ✓ brief status
  - ✓ First prototype; block diagram & Pinout
- Introduction
  - ✓ Why a FE Tester
  - ✓ tester functionalities
- Toward a new FE Tester
  - ❖ design
  - ❖ time scale
  - ❖ open questions

CCPC-ECS Status

- **concept**: generic mezzanine to connect any **device** to **control room**

  PCIe, I2C, JTag, SPI → **CCPC** → 1Gbs Eth

- **R&D and mass production**: **CBPF-Rio**

- **focus** on TELL40:
  - > OnBoard implementation due vertical limitation (ATCA)
  - > integration discussed in last october in Marseille

    PCIe, JTag (& maybe SPI) very useful

    I2C not needed due intrinsical control system in ATCA

- **Validation board**: Automatic Testing system for HW & SW

- **documentation**: technical note & specs & Talk
  - > available for next Electronics meeting

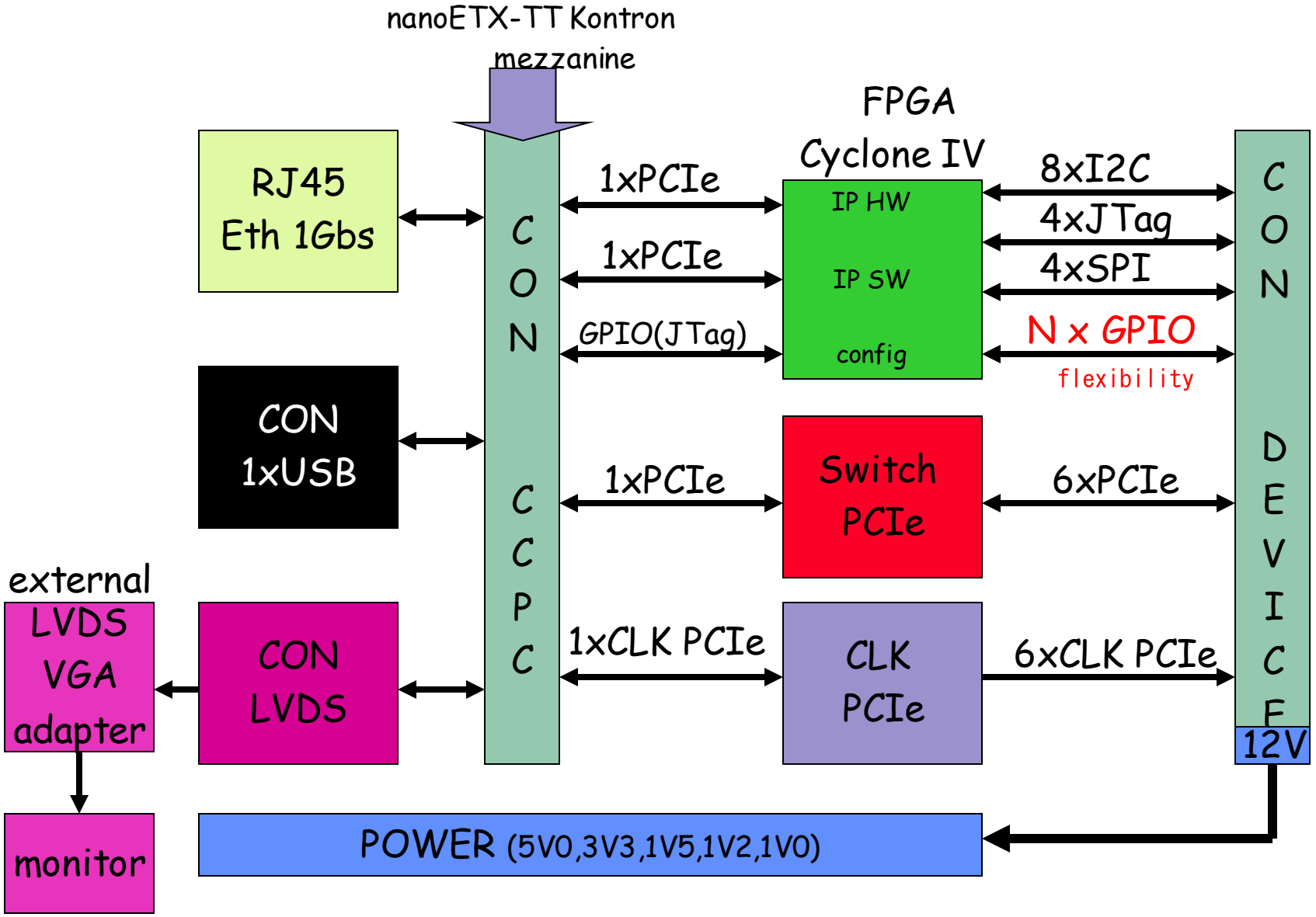
CCPC-ECS Status (cont'd)

- Software low-level on Linux:
  - > access registers of any Altera FPGA via PCIe *OK*
  - > load any Altera FPGA via JTag *OK*
  - > I2C control to any device (Temp,Biasing ...) *OK*
  - > SPI communication *to be done*
  - > PCIe ECS interface *our next Benchmark*

- Low Speed protocols implemented in Cyclone IV FPGA
  PCIe ←→ Cyclone IV ←→ I2C, JTag, SPI
  I/O flexibility
  - > Firmwares (except SPI) *OK*

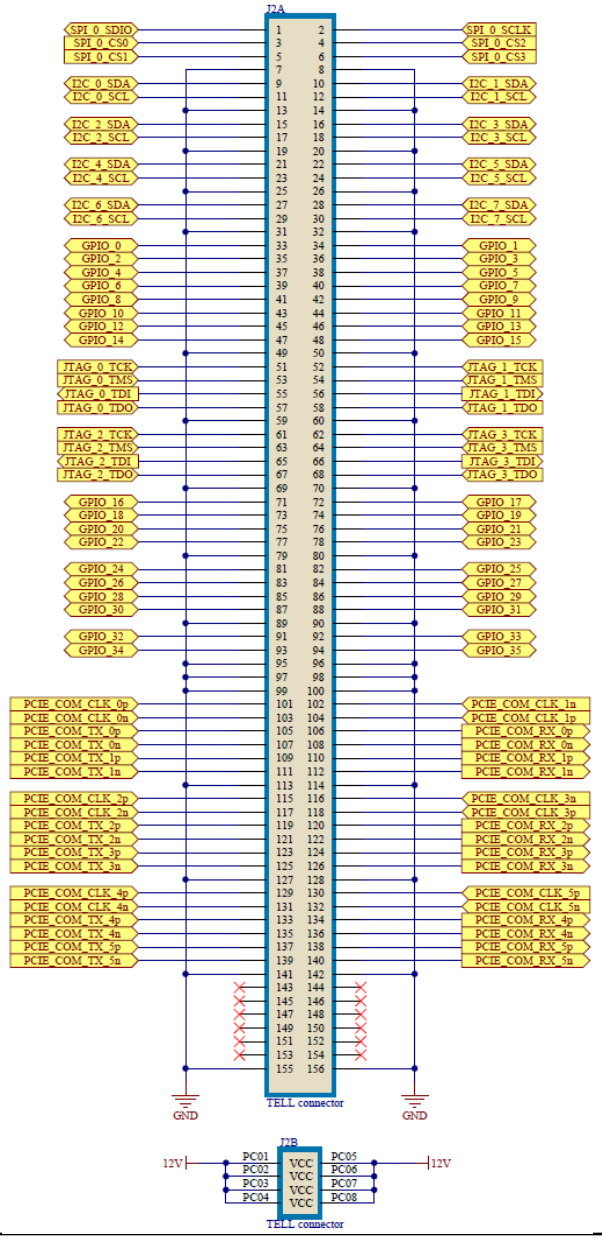
- Prototypes: CCPC-ECS & Validation boards
  - > both in production → ready Feb/2012
  - > five 2nd versions → mid 2012
    (Brasil, CERN, Marseille*, Lausanne, ...?)

First Prototype Block Diagram



First Prototype Pinout

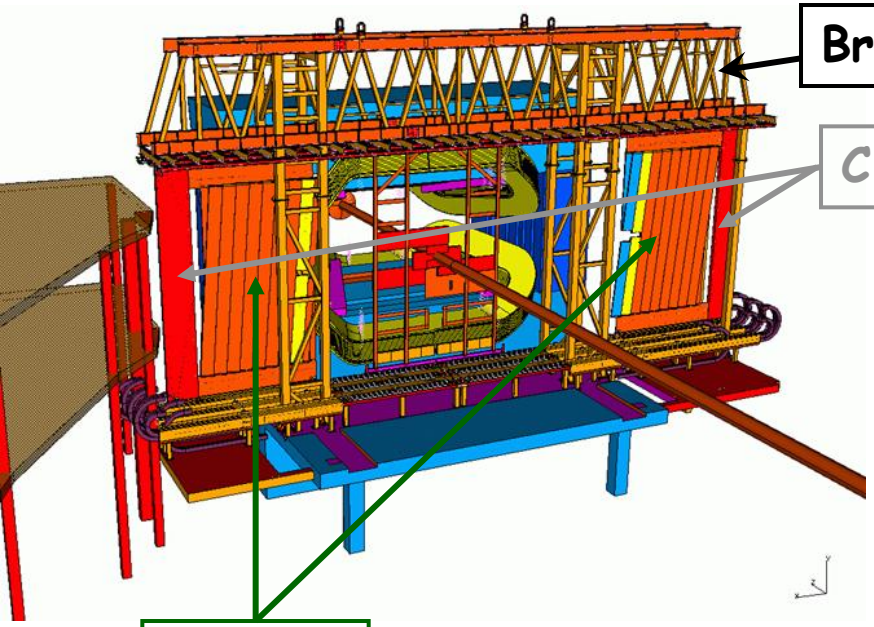
SAMTEC: QMS-078-04.25-L-D-PC4 (device)
QFS-078-04.25-L-D-PC4 (ECS)



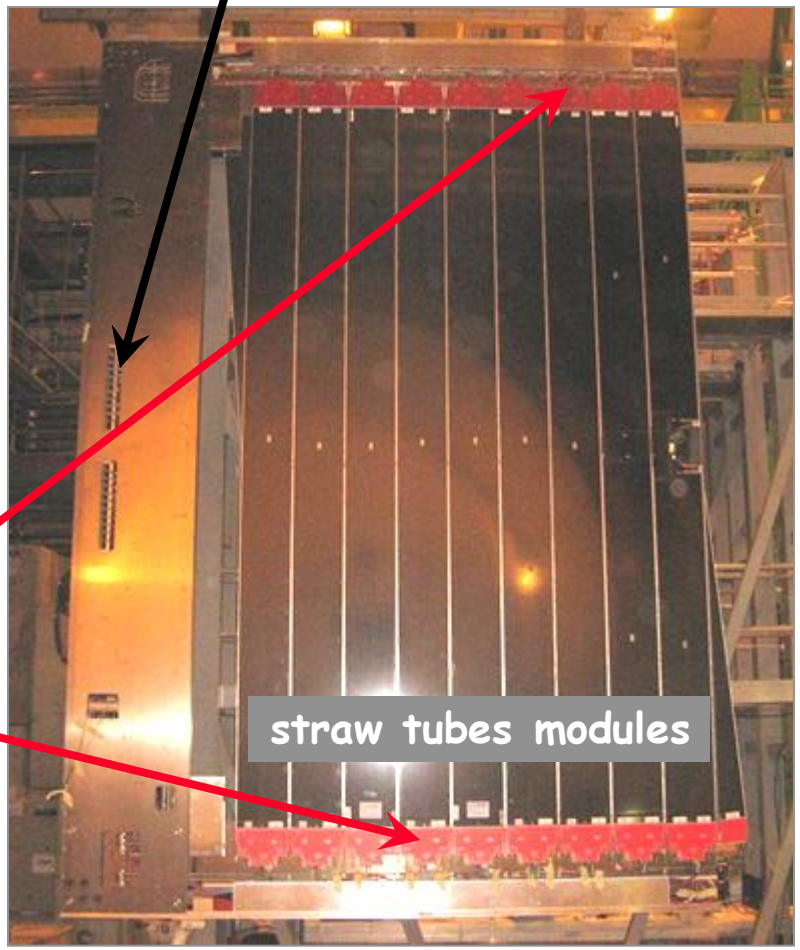
Switching topic

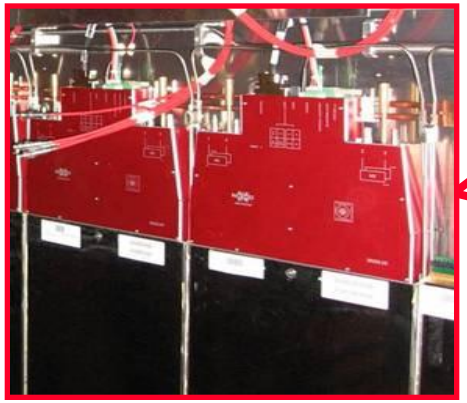
A Test Bench for the upgraded OT FE Electronics mass production

OT FEE Overview



Distribution of LV,HV, ECS/TFC, etc.





2×2×9 FE Boxes

FE Electronics (the present one)

Front end box (full size):

128 channels

4 × (32 ch) HV Boards

16 ASDBLR chips

4 OTIS TDC chips

1 GOL chip: 1.6 Gbit/s

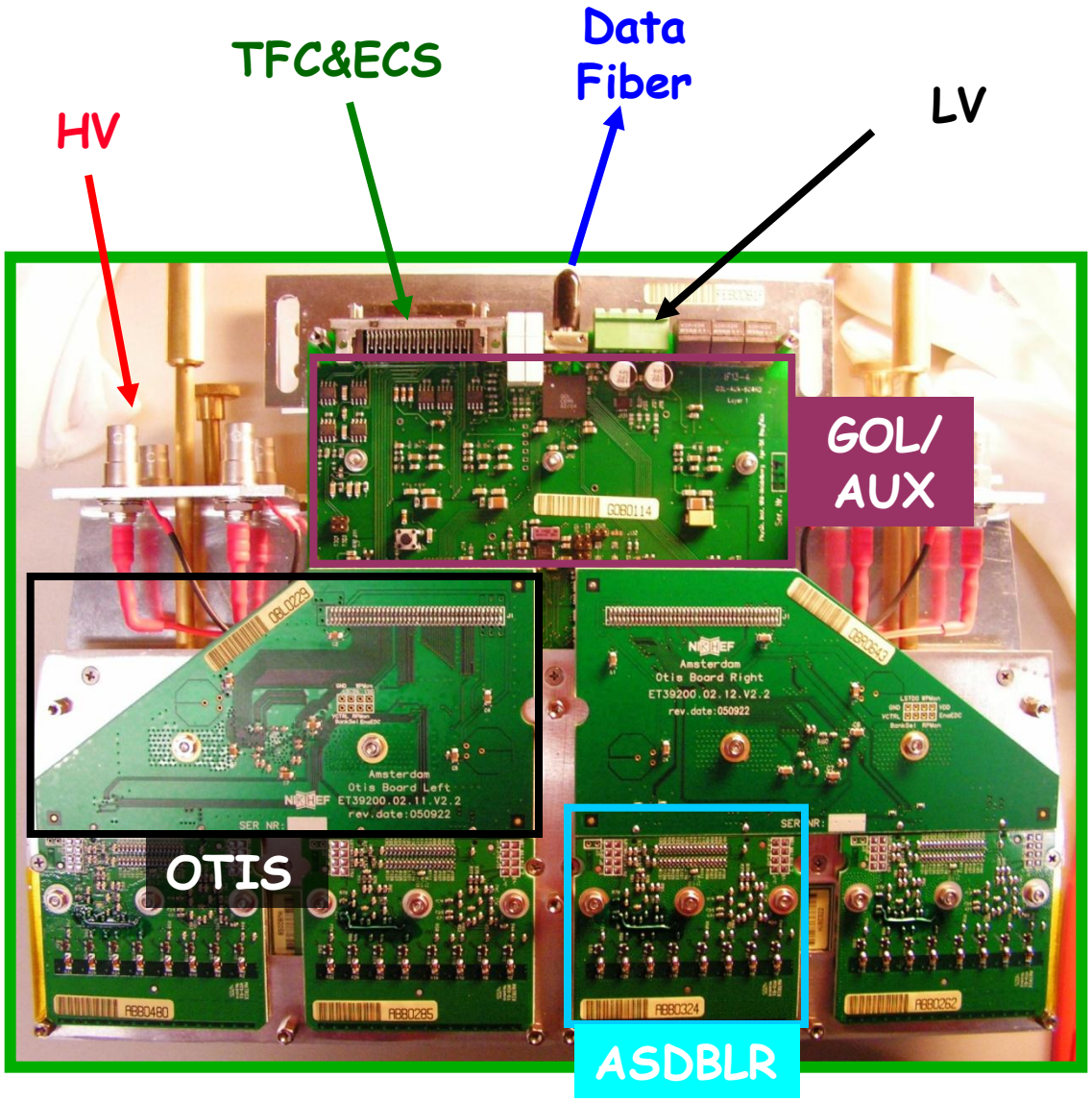
MASS PRODUCTION:

500 GOL/AUX Boards

2.000 OTIS TDC Boards

4.000 ASDBLR Boards

2.000 HV Boards



Why a FE Tester?

A fully automatized FE Tester was mandatory given the large size of the production

MASS PRODUCTION:

500 GOL/AUX Boards

2.000 OTIS TDC Boards

4.000 ASDBLR Boards

2.000 HV Boards

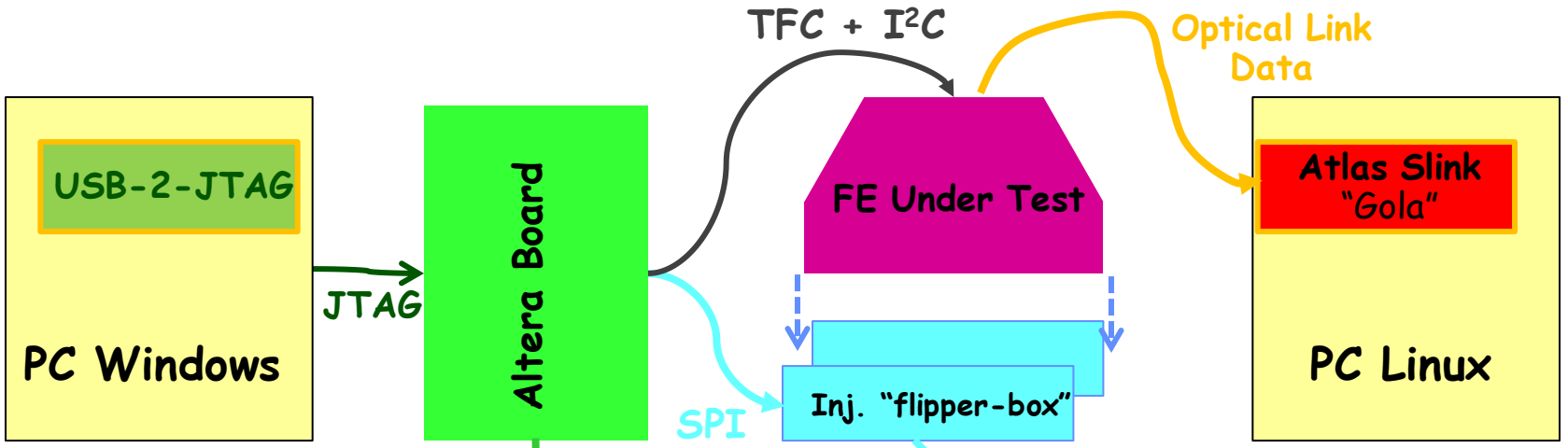
Although we tested individually all boards inside a FE Box, a final global test proved invaluable:

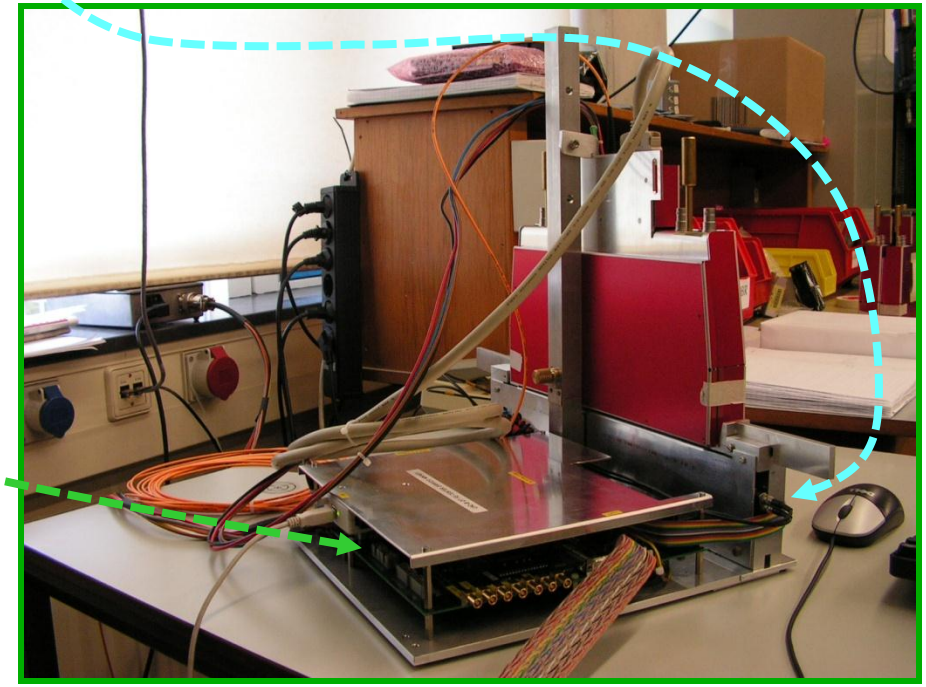
- FE assembly defects ⇒ ~1/3 of FE Box re-assembled
- synchronicity between 4 OTIS in one FE Box could be checked

We did NOT use ODIN and Tell1, but generated TFC internally and read data asynchronously (see next slides):

- simple setup, ready ahead of time (2 extra Nikhef FTE for 1 year)
- but could not check synchronicity (Bxid, L0id, etc.)

FE Test Setup

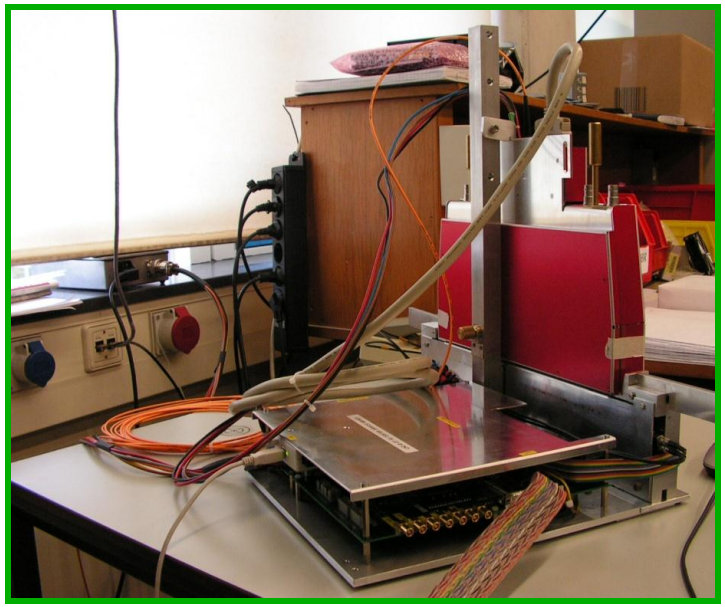


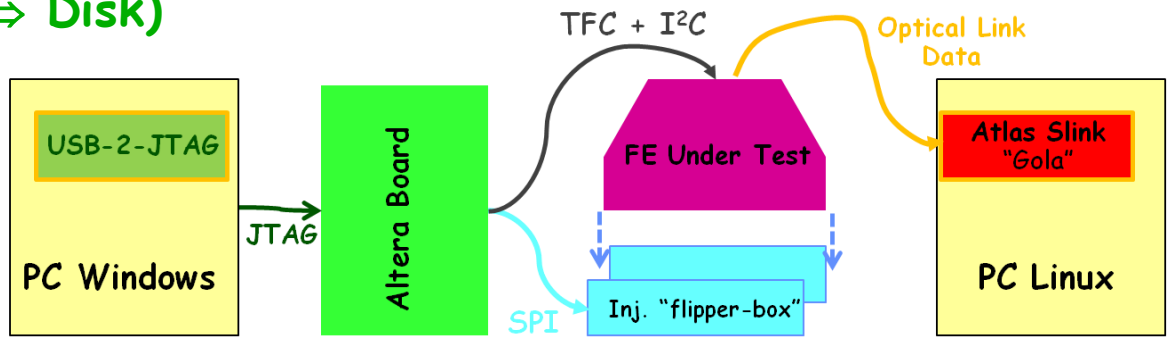


FE Tester Functions

Test of global functionality of fully assembled FE-Boxes:

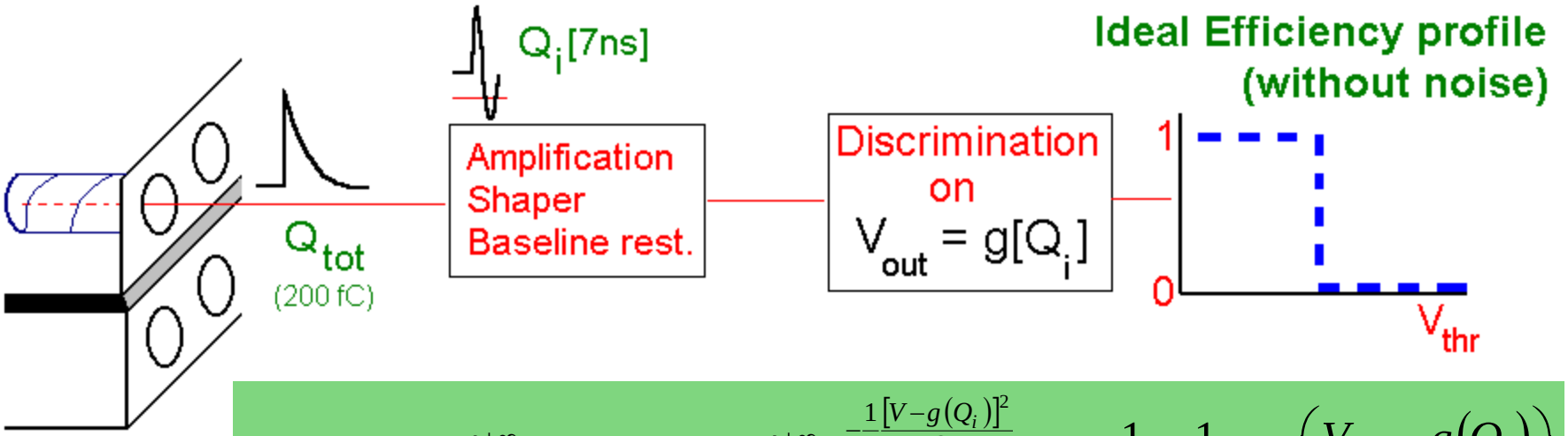
- Analog input signal injection (mimicking straw-like signal)
- Internal Generation of ECS & TFC
- Data Acquisition (Fiber ⇒ Disk)



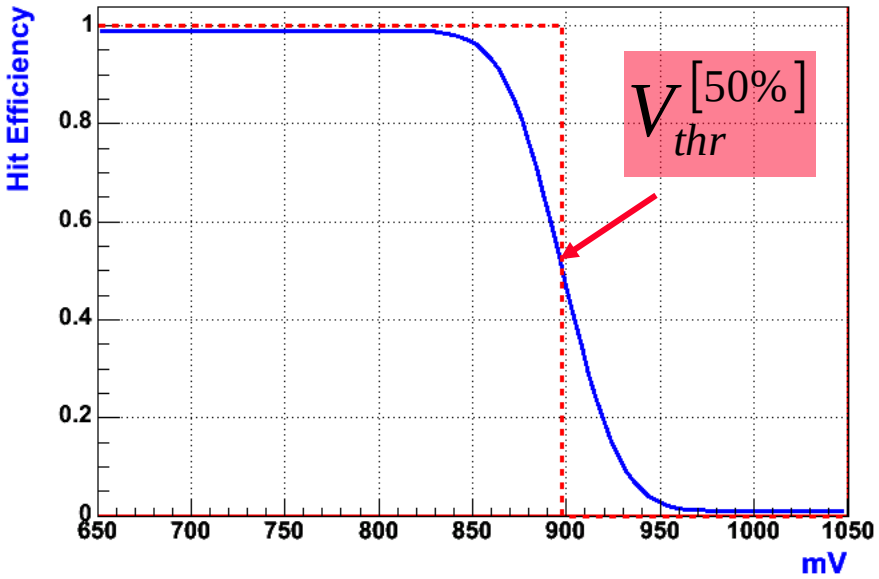


- Threshold Scan
- Input signal amplitude scan
- ASDBLR Testpulse (hi/lo even/odd)
- Input signal delay Scan
- LO delay scan
- …

Threshold Characteristics



$$P[Q_i, V_{thr}] = \int_{V_{thr}}^{+\infty} f(V)dV = N\int_{V_{thr}}^{+\infty} e^{-\frac{1}{2}\frac{[V-g(Q_i)]^2}{\sigma_{ENC}^2}} dV = \frac{1}{2} - \frac{1}{2} Erf\left(\frac{V_{thr} - g(Q_i)}{\sqrt{2}\,\sigma_{ENC}}\right)$$

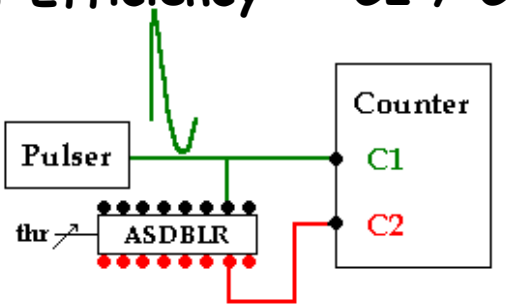


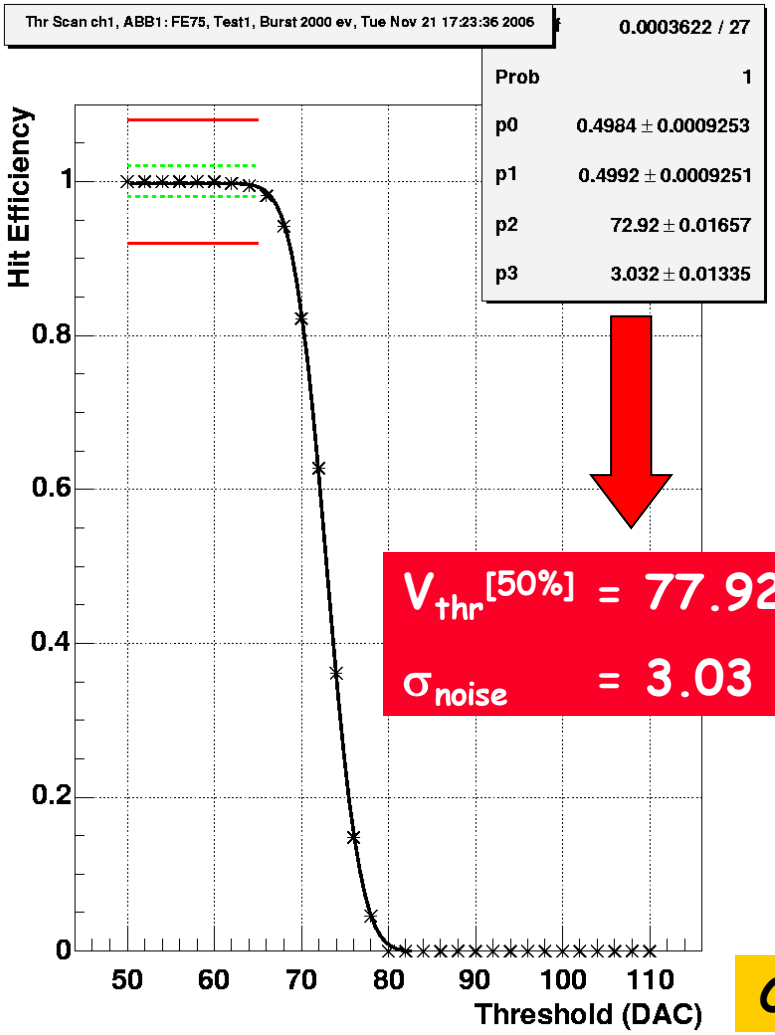
For a Gaussian Noise, fit efficiency curve with "Erf" and use 50% point as the best estimator

Threshold Characteristics (cont'd)

Measure hit efficiency profile for each channel, fit Erf to data and determine $V_{thr}^{[50\%]}$ and σ_{noise}

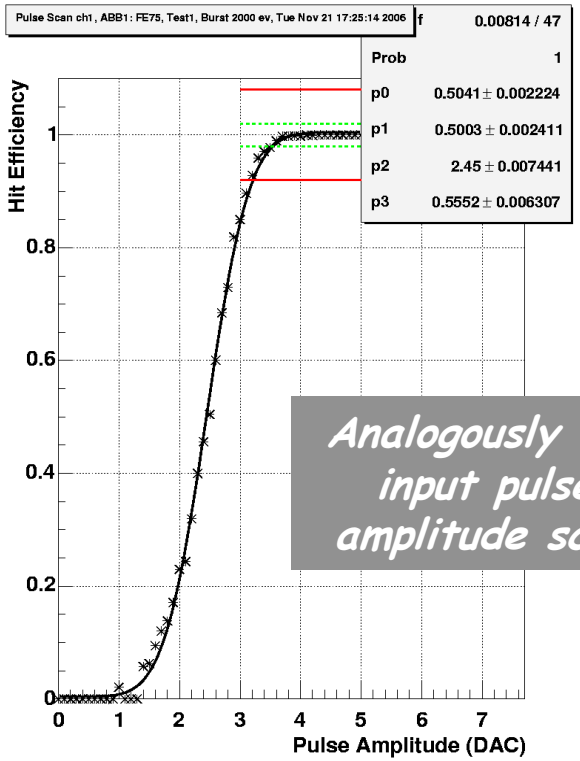
Hit Efficiency = C2 / C1





$V_{thr}^{[50\%]}$ = 77.92 DAC

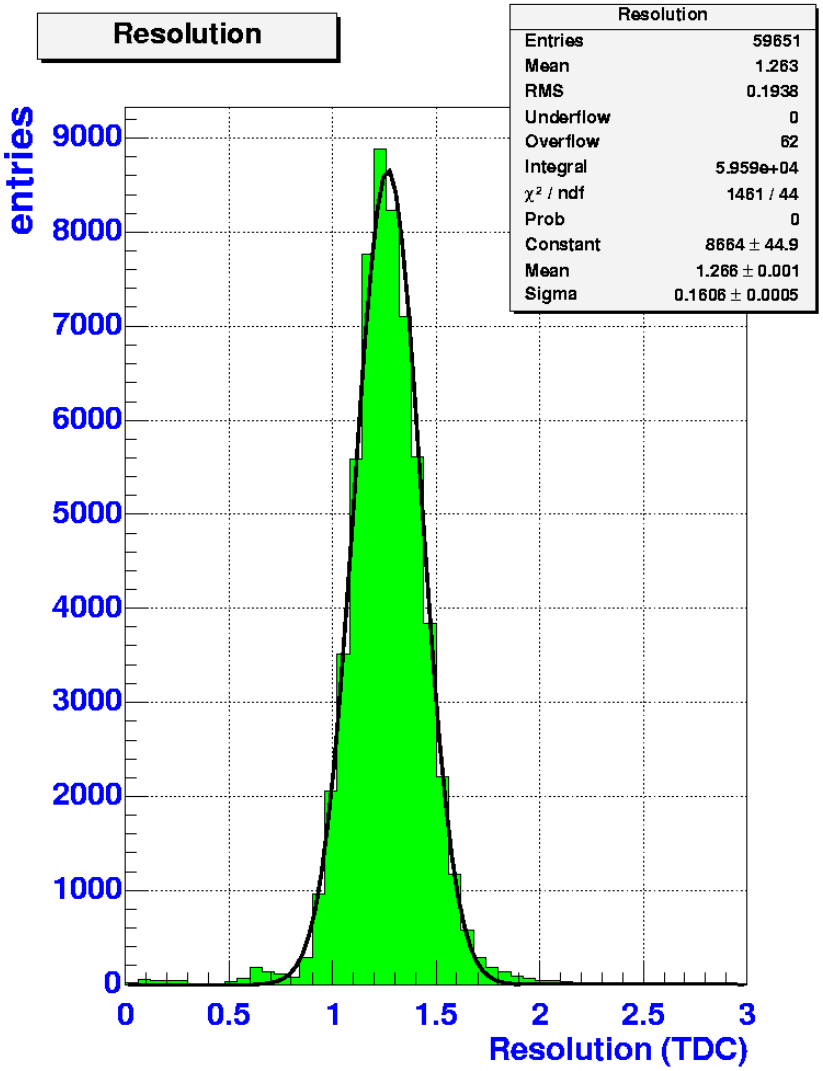
σ_{noise} = 3.03 DAC



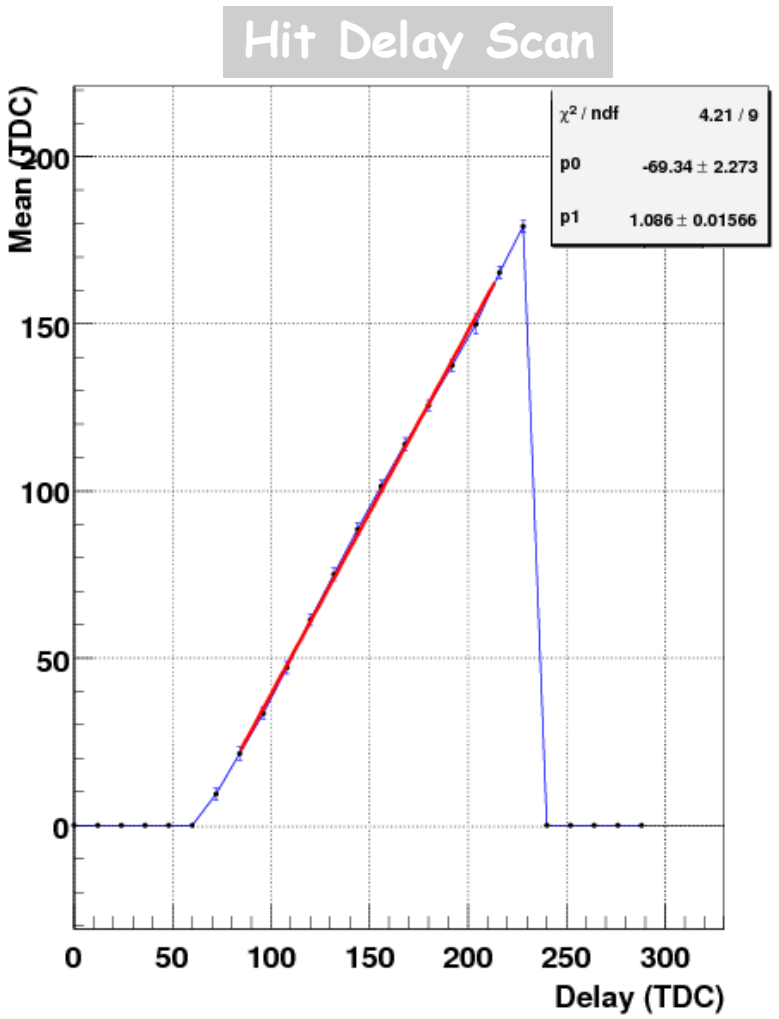
Analogously for input pulse amplitude scan

Channel-to-channel uniformity within ~50 mV!

Timing Tests



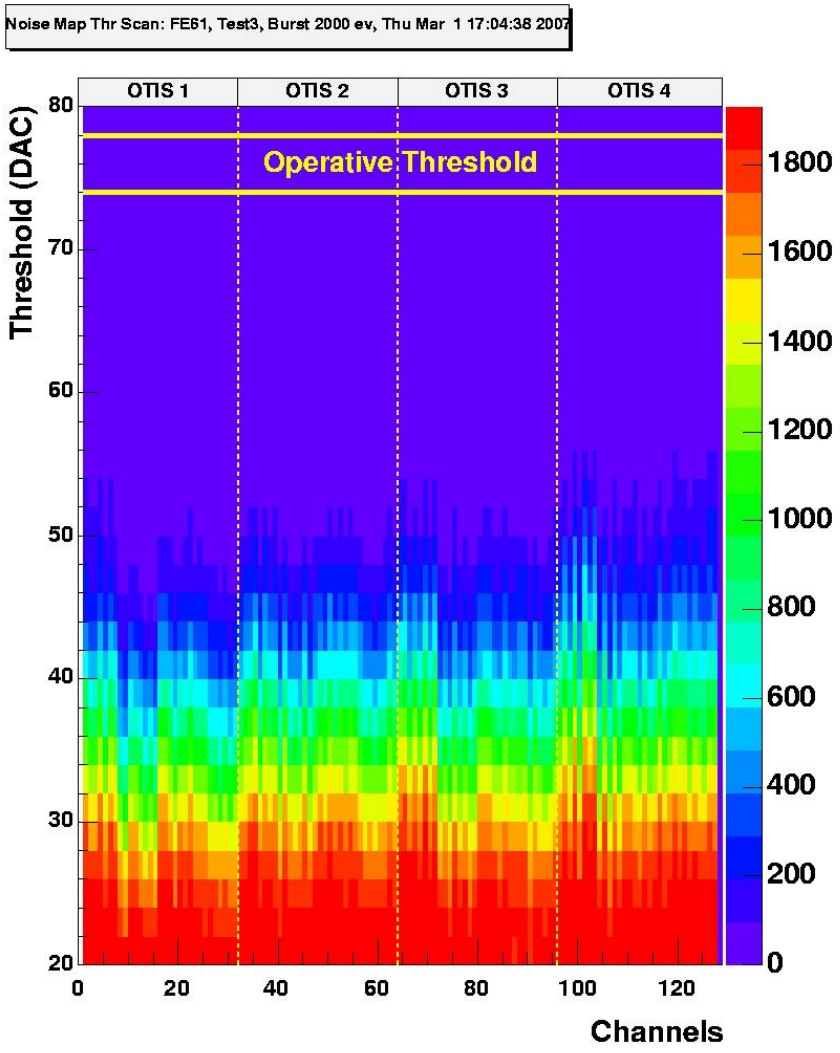
About 1.2 TDC channels (~0.5 ns)
Includes Test-Setup resolution etc.



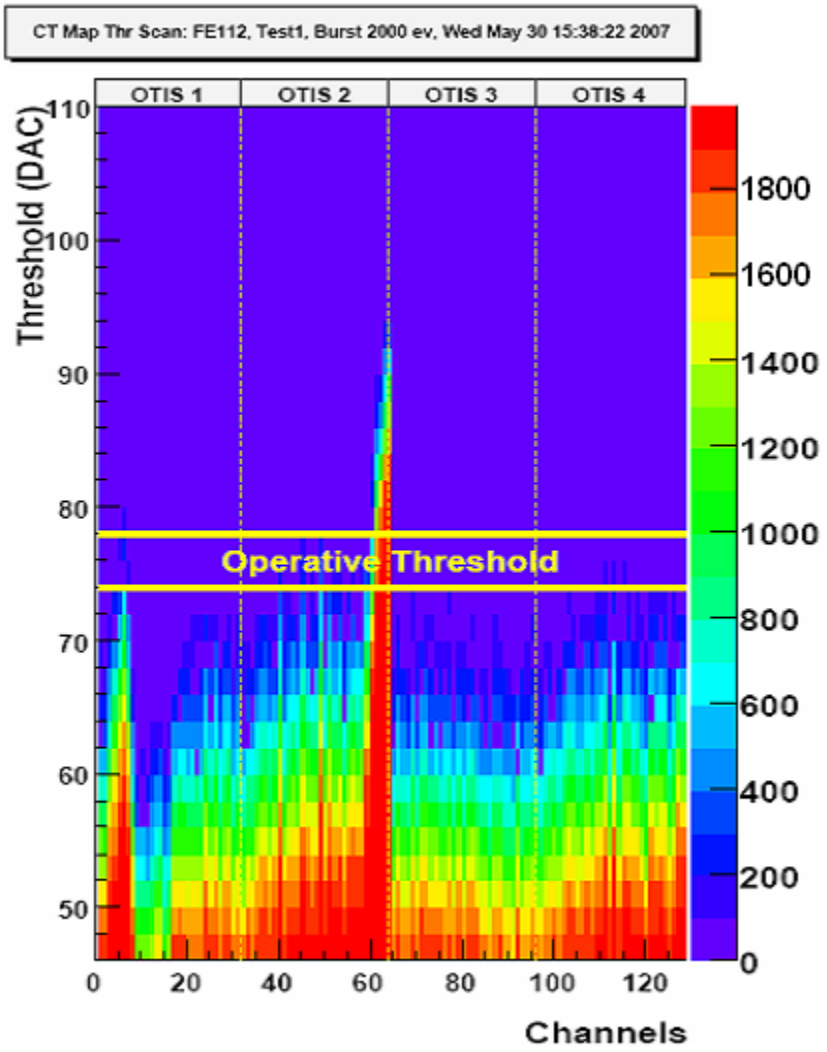
Fit straight line to data and reject if poor linearity (large $\chi^{2)}$

Noise Tests

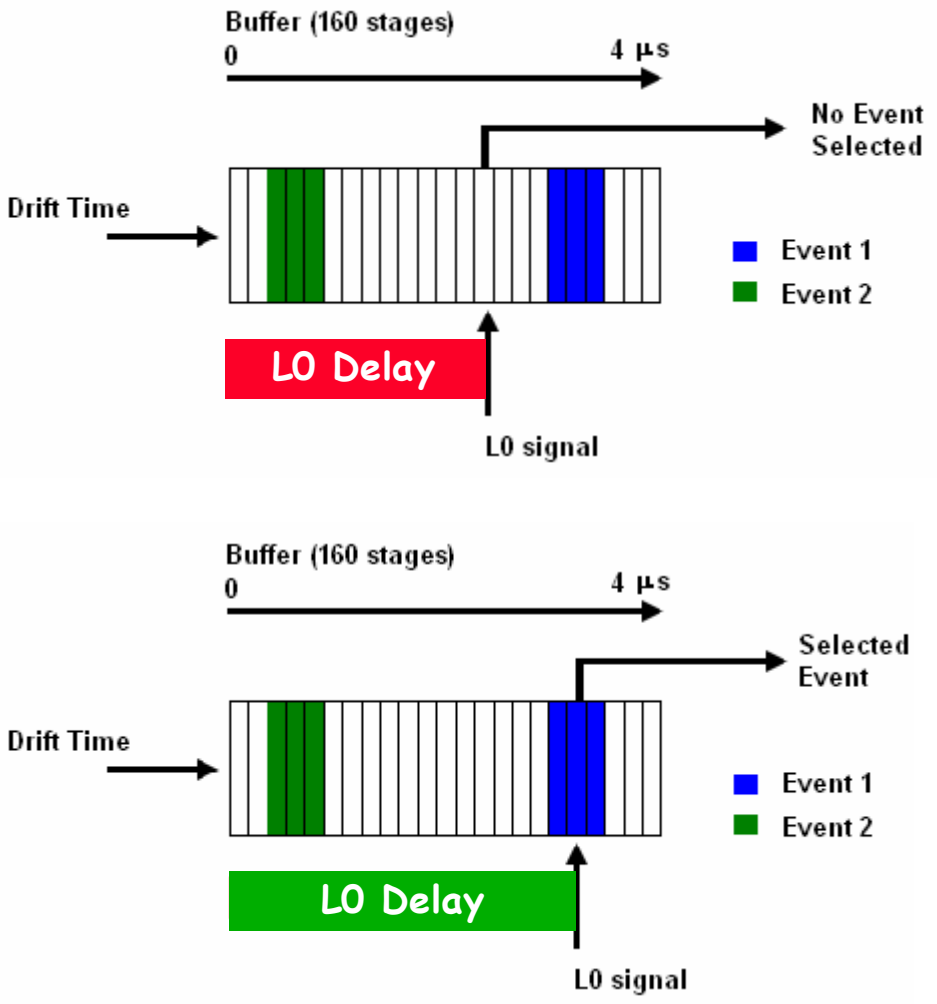
OK

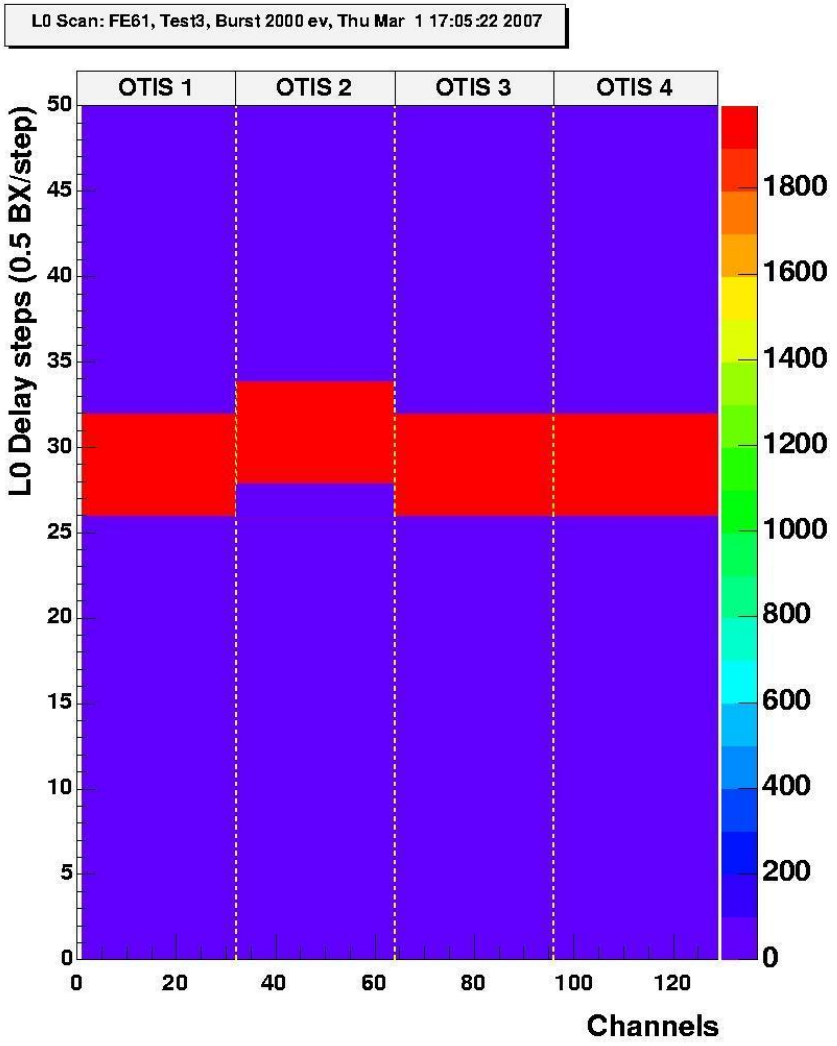


Noisy channels



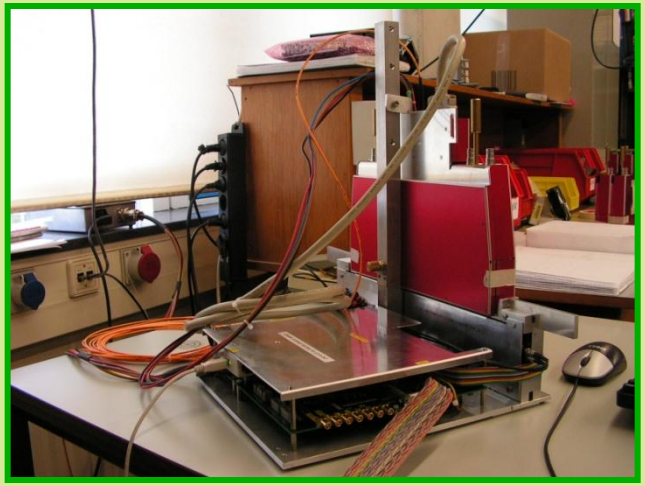
L0 Delay Checks





In summary: Test Sequence

- **Threshold characteristics :**
  - Amplitude Scan with input signal $\Rightarrow V_{thr}^{50\%}$, noise, cross-talk, etc.
  - Thr Scan with input signal $\Rightarrow V_{thr}^{50\%}$, noise, cross-talk, etc.
  - Thr Scan with Testpulse (lo/hi) $\Rightarrow V_{thr}^{50\%}$, noise, cross-talk, etc.
- **Noise :**
  - Thr Scan without input signal
- **Timing :**
  - TDC spectra of all channels
  - Input delay scan over the full time range
- **LO scan :**
  - LO Delay Scan in steps of ½ BX
- **Analysis**
  - Control histograms automatically generated for all tests, fitting, etc.



All test results available via the Web

What we learned

- quality of production excellent thanks to systematic and meticulous testing
- should have (did not!?) tested also high data-load with random triggers
  - check synchronicity (mainly Bxid)

- we used up >90% of our spares (mainly in commissioning in 2009 and 2010)
  - buuuut… repaired all defect FE Boxes!!
  - ✓ without retaining functional FE Testers, we'd be dead by now!
  - ✓ FE Tester not only important in production, for whole life cycle!

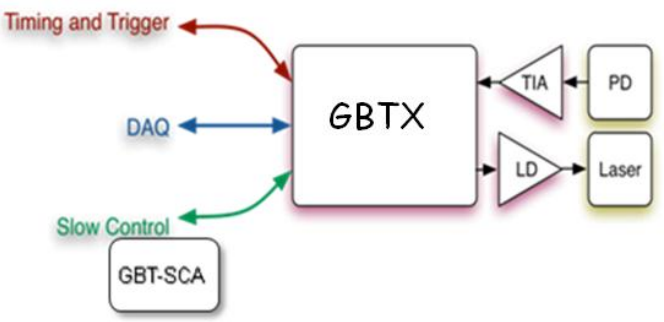
- FE Box transport needs care!?
  - Not much use testing, if lousy transport after test!?
  - corollary: needs FE Tester also at CERN

GOOD!

NOT GOOD!

Goal of the project

What tester do we need for the upgraded OT FE?



- a tester who can receive the GBTx data
- a tester using GBT/GBT-SCA for TFC/ECS
- a tester capable of writing "raw" data to disk
  - Real time? What bandwidth? Well, let's say at least "bursts" of O(10,000) consecutive events (a "step" in a threshold/delay scan!)
  - histogramming in FPGA? Yes, please!
  - data analysis in FPGA? No, thanks!
- a tester who can be itself controlled via TCP/IP GbE
  - mainly to configure a "step" run (e.g. 33 threshold steps of 10k evts)
  - extra controls needed (e.g. SPI) ? Probably not…

When do we need it?

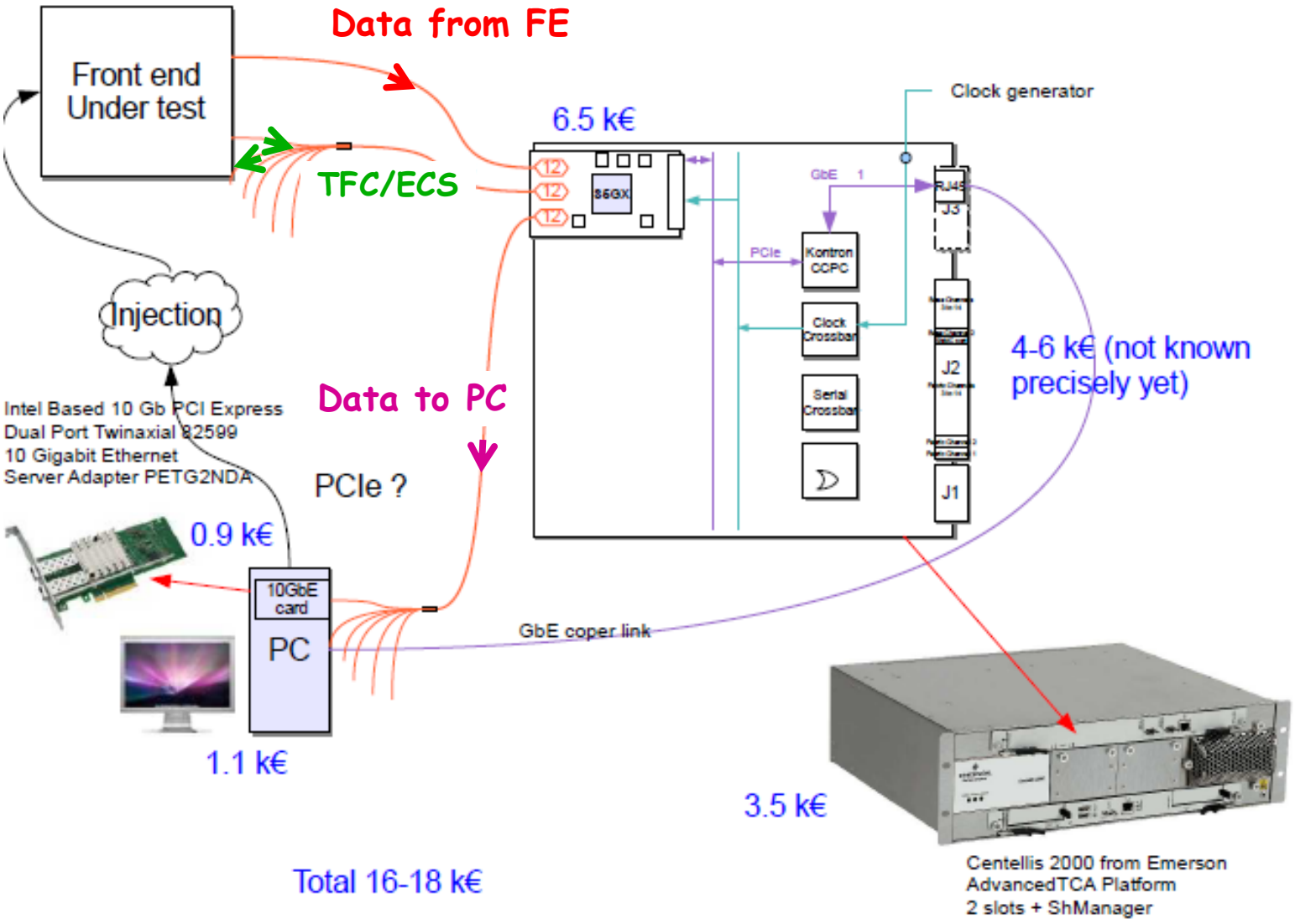
Basic blocks 2nd half next year, 1st prototype in 2013, 3 instances by 2014

CBPF/Nikhef cooperation (aimed at OT), support by Marseille & LHCb Online

Question: commonalities with other test benches??

The Perfect Answer!

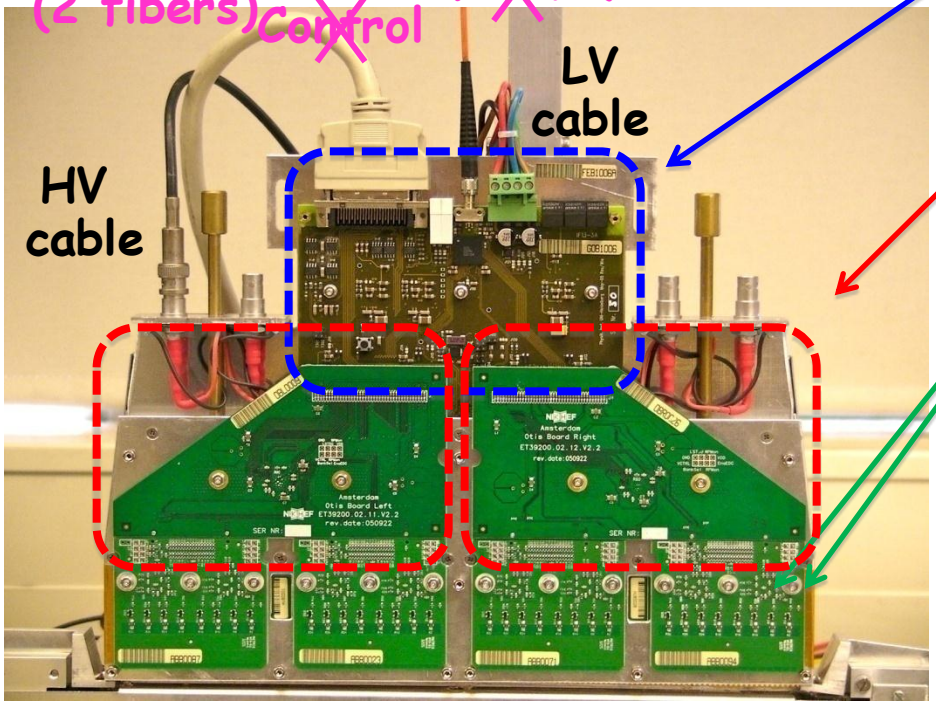
Based on proposal by J-P Cachemiche & A. Massafferri



Overview of OT 40MHz Upgrade

We have 432 of these objects (FE Boxes in OT)

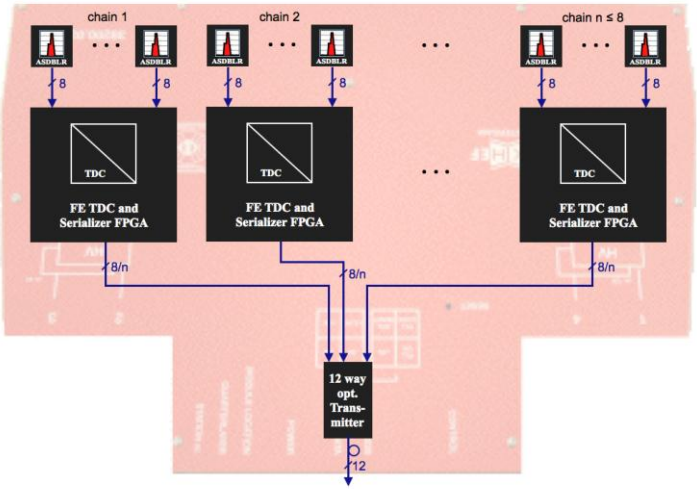
- 36 per C-Frame (12 C-Frames)



GOL/AUX Board (and ASIC) needs replacement

OTIS Boards (and ASIC) need replacement

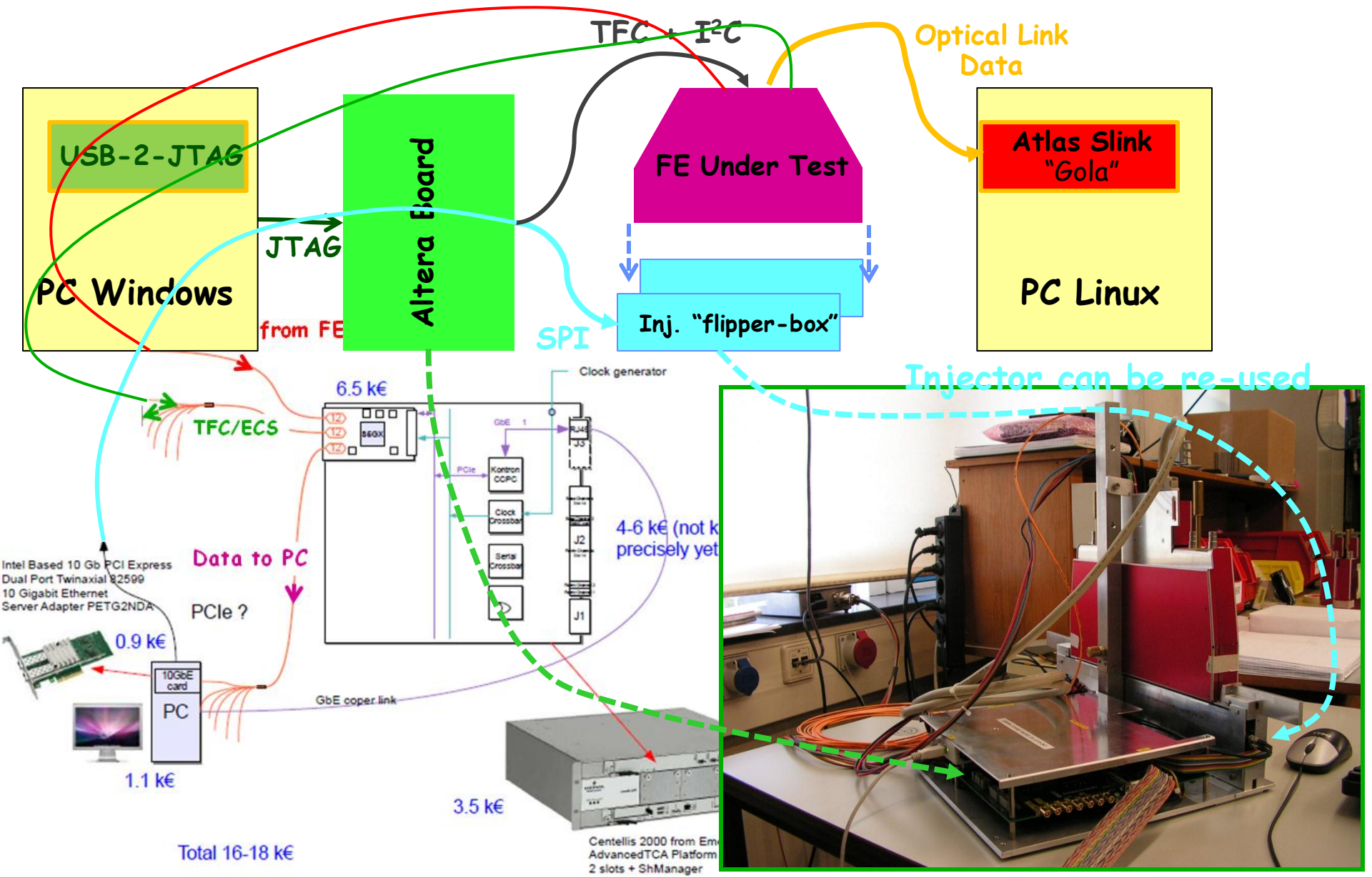
HV and ASDBLR Boards may remain unchanged



So, Tester <u>physical interfaces</u> to/from FE Box are:

- 12-fibers ribbon (data: 4 or 8 GBTx)
- 2 fibers (bi-directional TFC/ECS)

Modified FE Test Bench



Optical Interfaces

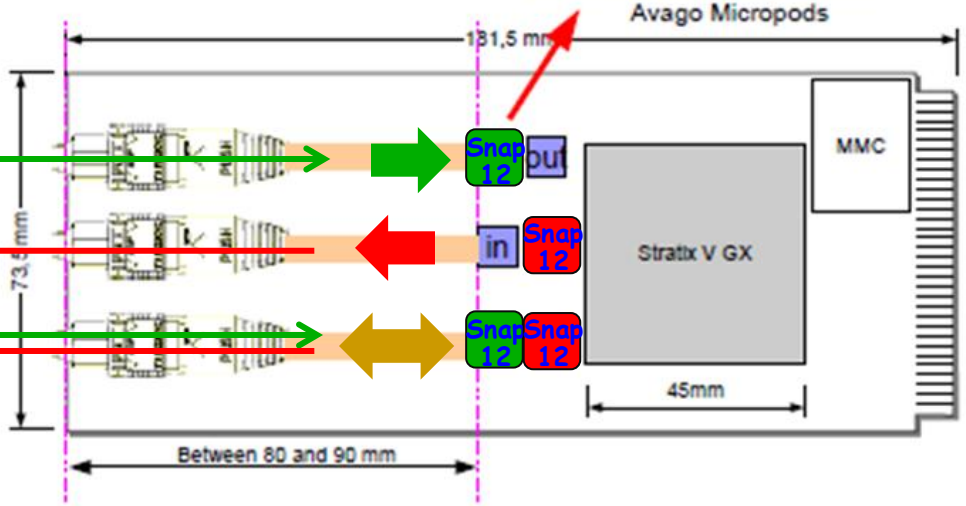
Use input/output configurability of the 3×12 optical links to/from Stratix V

12× Data from FE

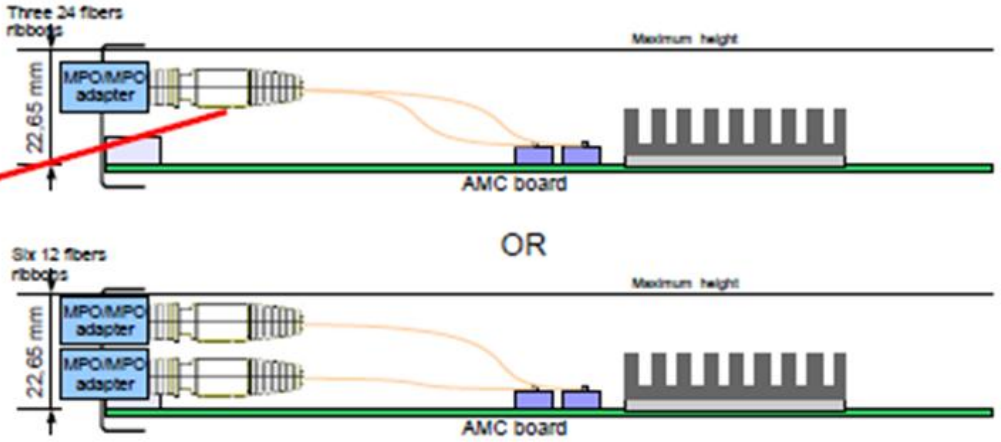
12× Data out to PC

6× bidirectional TFC/ECS

Avago Micropods



MPO/ Prizm patchcord



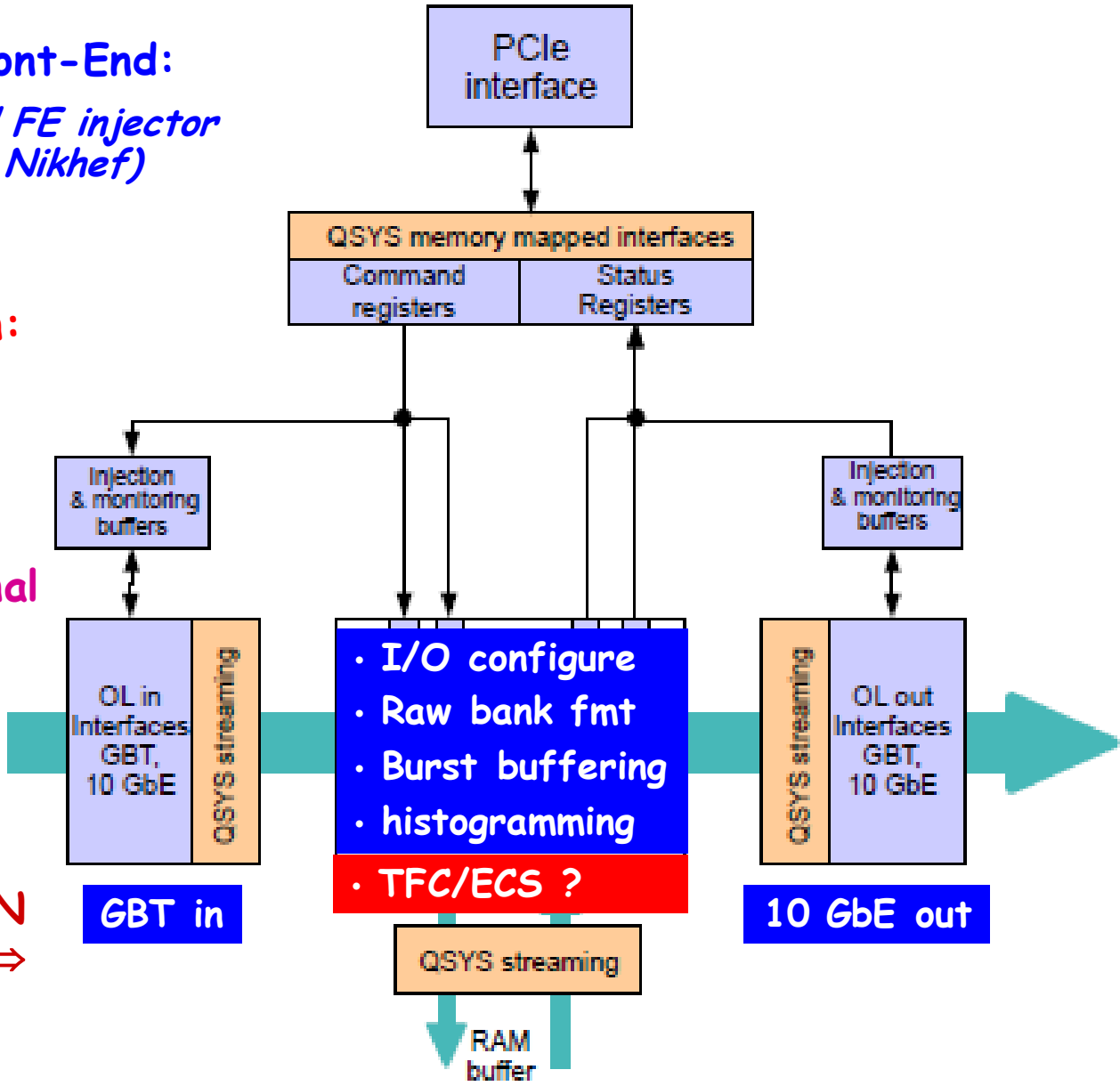
FPGA Firmware interfaces

E.g. for data from Front-End:

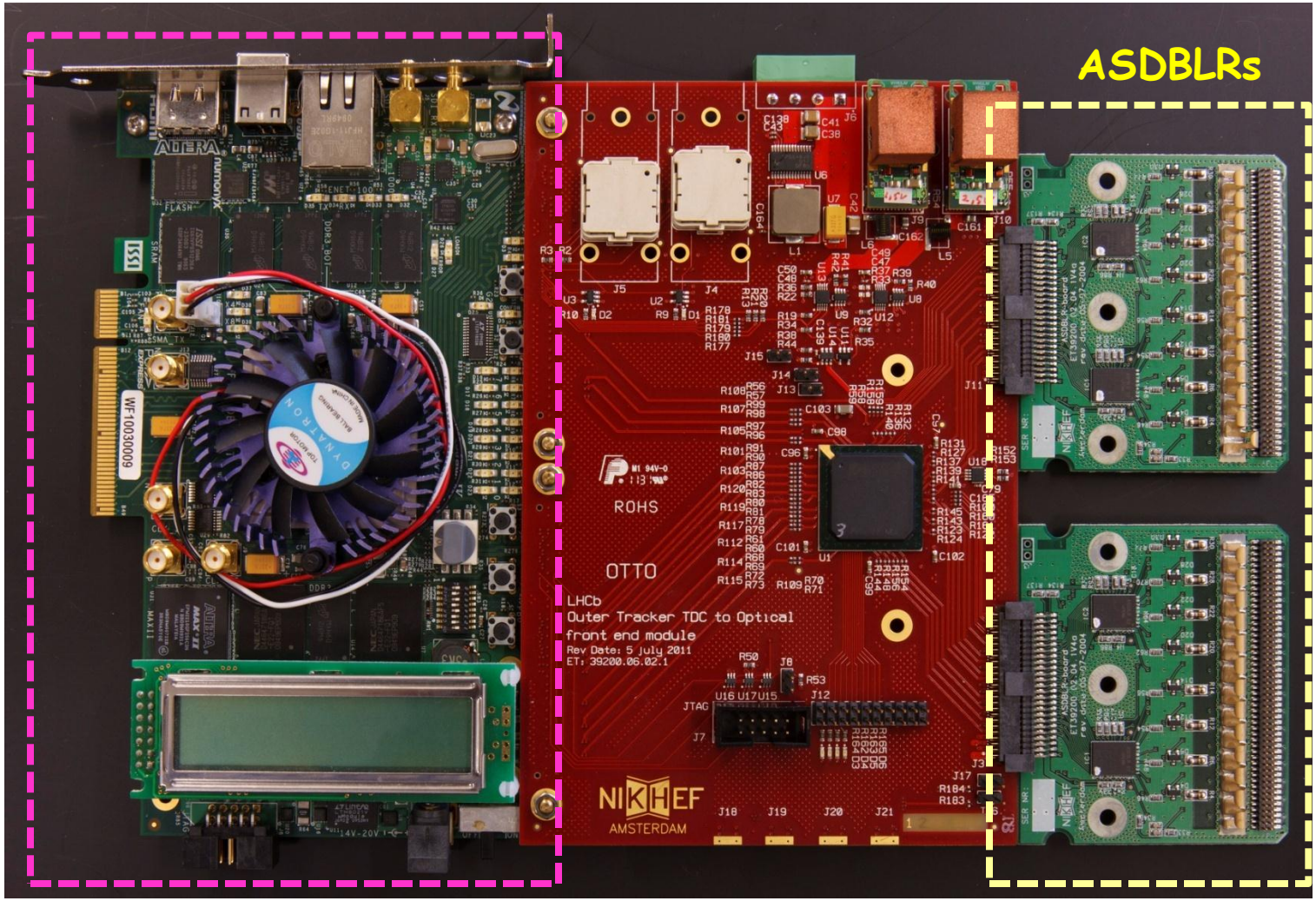
This part of User code (and FE injector control?) by us (CBPF + Nikhef)

However needs clarification:

- will there be a TFC/ECS firmware fitting in the same Stratix V?
- capable of working (e.g. STEP runs) without external hardware?
- will there be basic software (C API? PVSS?) to drive the TFC/ECS?
- When? Who?
  - CBPF student at CERN (L. Lessa) could help ⇒ OT pilot test-case ?



Where we are now

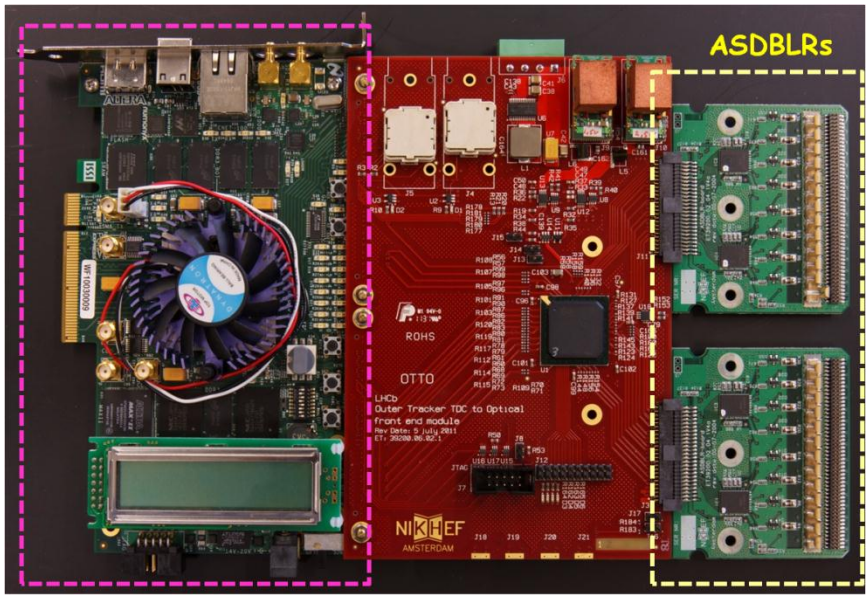


Stratix IV (readout and GBT emulator)

How do we read & control?

At present testing through:

- ASDBLR connected to Actel TDC
- all data and control lines from/to Actel via HSMC connector to Stratix IV
- Actel registers (I2C) controlled by Stratix IV via 1GbE
  - UDP Nikhef-made + encoding/decoding software on Linux
- all data read by Stratix IV via 1GbE (UDP Nikhef-made)



Stratix IV (readout and GBT emulator)

Ok for a while, until 1st prototype Actel TDC service board debugged, then FE test bench needed

When do we need it?

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