ANALOG MEMORY VS TDC FOR ECAL UPGRADE II ELECTRONICS

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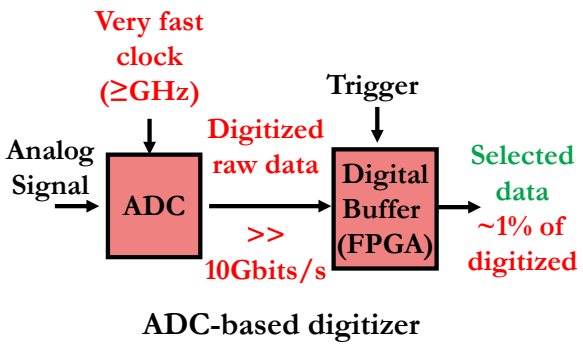
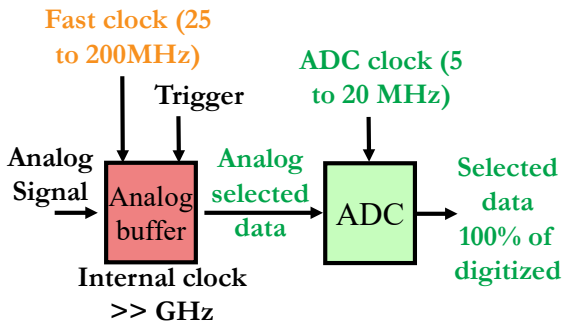
INTRODUCTION

- **Time stamping** will permit the **localization of vertices** with a few mm precision, thus helping dealing with the pile-up foreseen at HL-LHC.
- **Time to Digital Converters (TDCs)** are the usual candidates for time stamping of fast signals.
- But the progress in **ultra-fast digitizers** (including high-end oscilloscopes) demonstrated that ps timing accuracy can be reached simply by **sampling the detector signal at high rate** and extracting time information by **interpolation of the leading edge samples.**
- Another advantage of recording the waveform resides in cases where the shape of the signal carries **extra information** in addition to direct measurements (time, amplitude, etc…).
- But getting the full **signal waveform** has a non-negligible cost, especially at high rates (a few tens of k€ per channel for a high-end oscilloscope).
  - Fast analog memories (SCAs) permit high speed sampling at low cost.
  - But their counting rate is limited by their readout time.



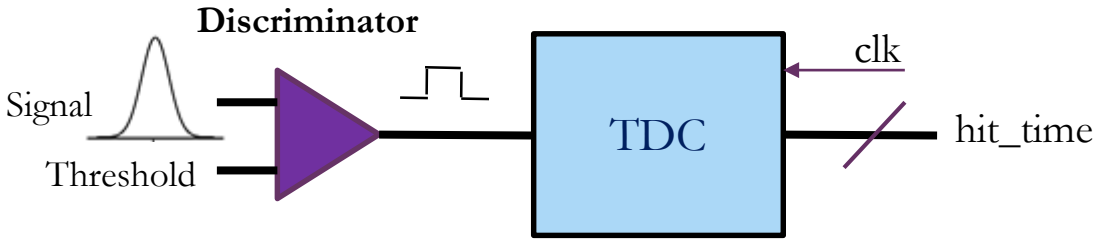
ADC-based digitizer



SCA-based digitizer

METHODS FOR TIME MEASUREMENT: TDCS (1)

- **Time to Digital Converters** (TDCs) are commonly used for time measurement in physics experiments.
- They are designed either in the form of **dedicated ASICs** or integrated inside **high-end FPGAs**.
- Here, the information is concentrated into a simple digital integer value, thus reducing drastically the quantity of information, which is adequate for large scale measurements.



- But TDCs **do not provide information on waveform**, except under the derivate form of time over threshold (**TOT**) for those able to measure both edges of the signal. But in this case, the precision on the amplitude or charge is poor (especially due to the asymmetry of the signal edges).
- The TDC has a strictly digital input => **a discriminator** has to be present to transform the **analog signal into digital**. It introduces **additional jitter and residues of time walk**

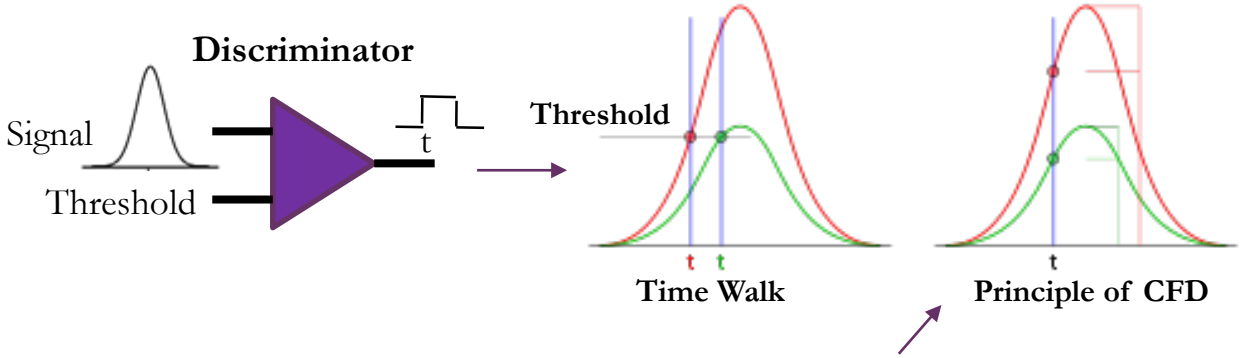
=> the overall timing resolution is degraded to **the quadratic sum of the discrimination and TDC contributions**, making it difficult to go below a few 10's of ps rms for large dynamic ranges.

A FEW WORDS ABOUT DISCRIMINATION

A discriminator translates an analog signal into a digital pulse.

When sending a signal to a discriminator, the time instant "t" of the output level toggling will depend on the amplitude of the signal

=> **"Time Walk"** effect



To avoid this effect, one has to use a Constant Fraction Discriminator (CFD)

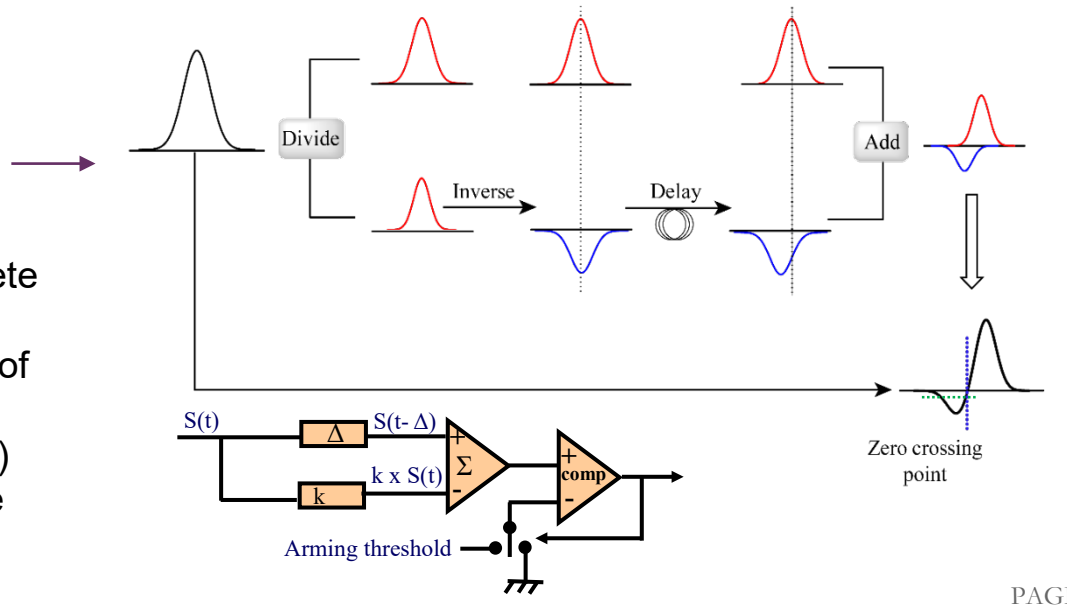
- But this implies that **you need to know the value of the peak** to apply the threshold !
- Ok for a firmware or software when the signal has been digitized but **not in a TDC** …

How to make a CFD in an analog way in front of a TDC:

- but never perfect (there is always a residue of time walk)
- Requires many components for discrete implementation
- hard to integrate in an ASIC because of the delay line (needs inductances)

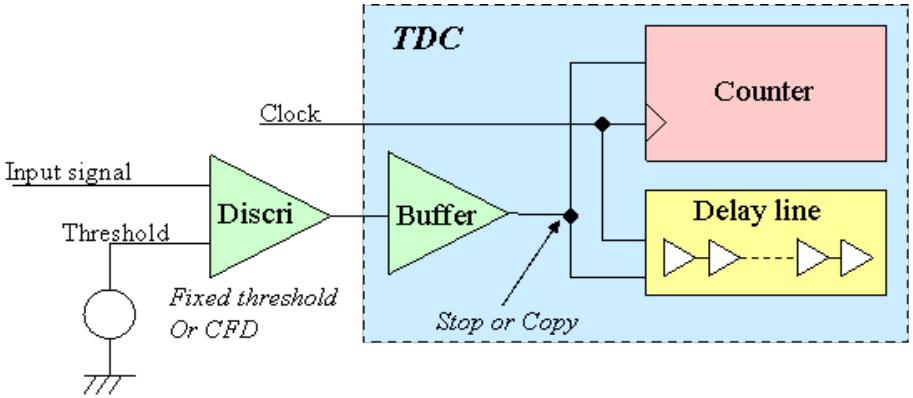
=> other options are used (RC filter)

but they tend to degrade the performance



METHODS FOR TIME MEASUREMENT: TDCS (2)

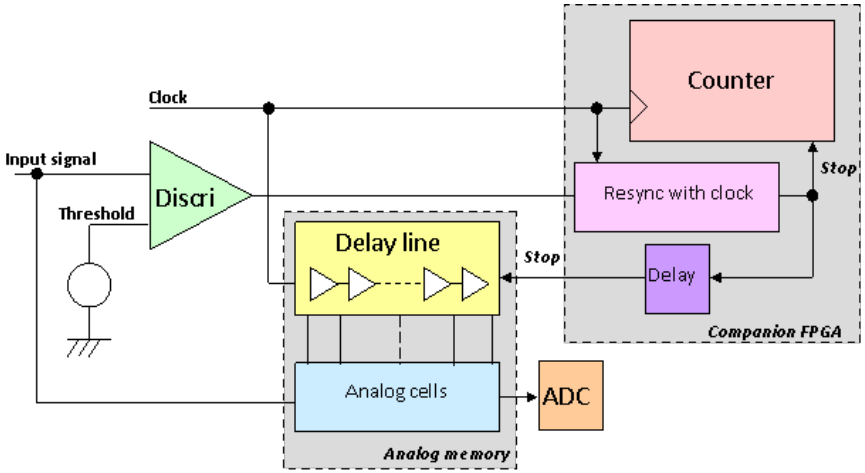
- The pure digital TDCs are usually based on the association of a **coarse time counter** running on the main clock and of **Delay Lines** (DLs) interpolating the clock.
- In order to improve the resolution, the DLs can be **smartly interleaved**, introducing a third stage for the fine measurement (PicoTDC).



- Resolution is given by **the Delay Line or interpolator step** but it is usually limited by stability of calibration or environmental effects.
- Each channel is **self-triggering**. This permits reaching high counting rates (>> MHz).
- In the case of large experiments, in order to limit the dataflow, dedicated **buffers** are usually present at the TDC output for **selecting hits** based on an external trigger system like in the large particle physics experiments where the first level general trigger sorts the events.

FAST DIGITIZERS: ANALOG MEMORIES…

- Time measurement can also be based on **a mix of fast analog memories using Switched Capacitor Arrays (SCAs) and FPGAs**. This is a smart solution for **replacing ADCs**, especially in terms of power, space and money budgets.
- **The discriminator is not anymore in the critical timing path**. Time information is given by association of the Timestamp Counter (few ns step), of the DLL locked on the clock to define region of interest (100 to a few 100's picoseconds minimum step), and finally of the samples of the waveform: their interpolation will give a precision of **a few picoseconds rms**.

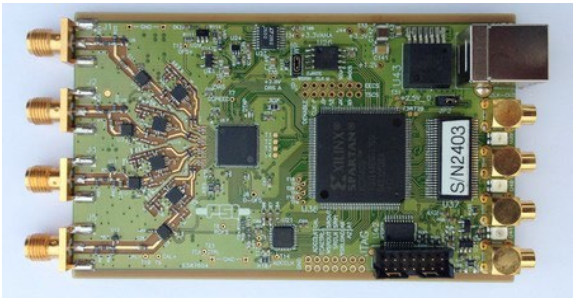


- This requires a precise **calibration of the Time Integral Non-Linearity** (like for ADCs). A very good time resolution can be reached even on small analog signals (a few tens of mV).
- The main drawback of the SCAs is their **readout dead-time** (a few tens to ~100 µs depending on the number of samples read), which becomes a limitation at high rates. Moreover, the channels are **usually commonly triggered and readout like in an oscilloscope**.

EXAMPLES OF SCA-BASED FAST DIGITIZERS

4-channel Evaluation Module

DRS4 ASIC and modules
(S.Ritt, PSI)



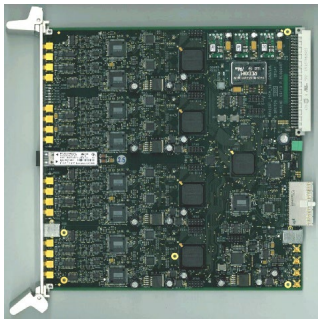
CAEN version
(V1742)

Currently used for test beams

WaveCatcher modules

8-channel Module

16+2-channel Module



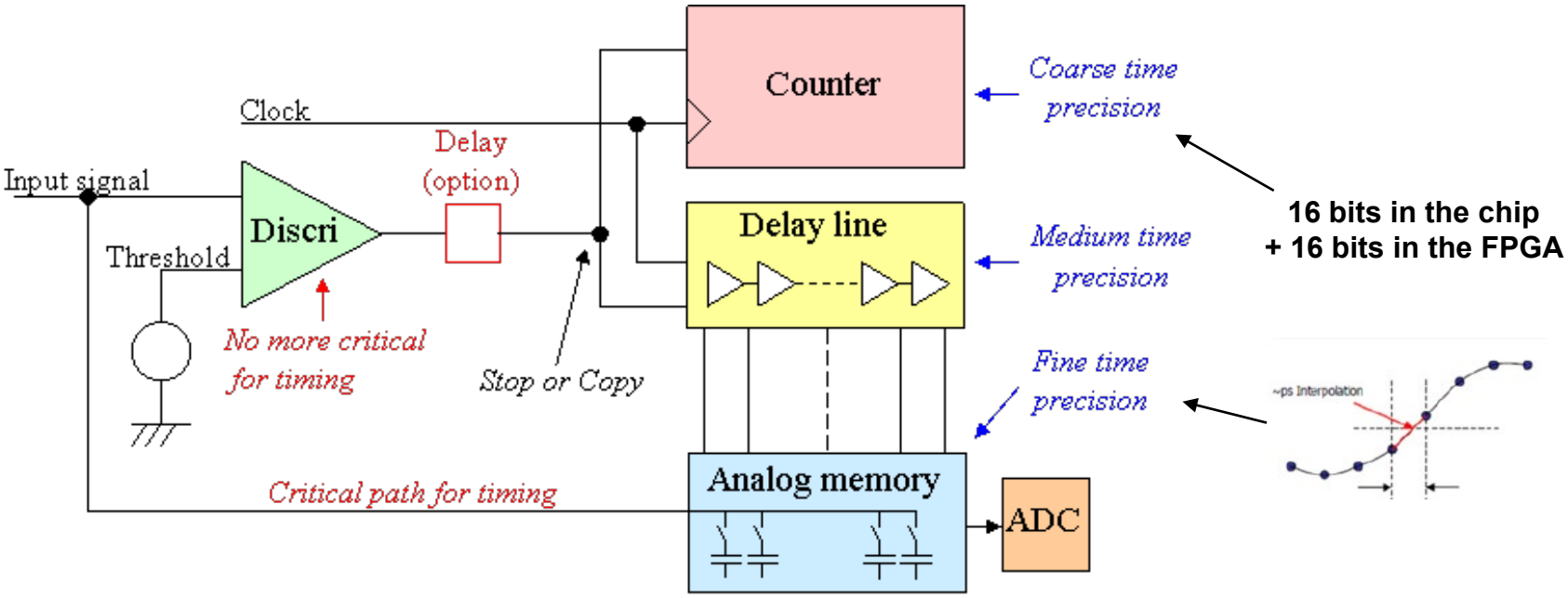
16+2-channel board

64-channel mini-crate

CAEN version
(V1743)

THE « WAVEFORM TDC » STRUCTURE

- Mix of DLL-based TDC and of analog-memory based Waveform Digitizer
- **All channels are self-triggering**
- The TDC gives the time of the samples and the samples give the final time precision after **CFD interpolation** => **resolution of a few ps rms**
- Digitized waveform gives **access to signal shape**…
- Conversely to TDC, discriminator is used only for triggering, **not for timing**

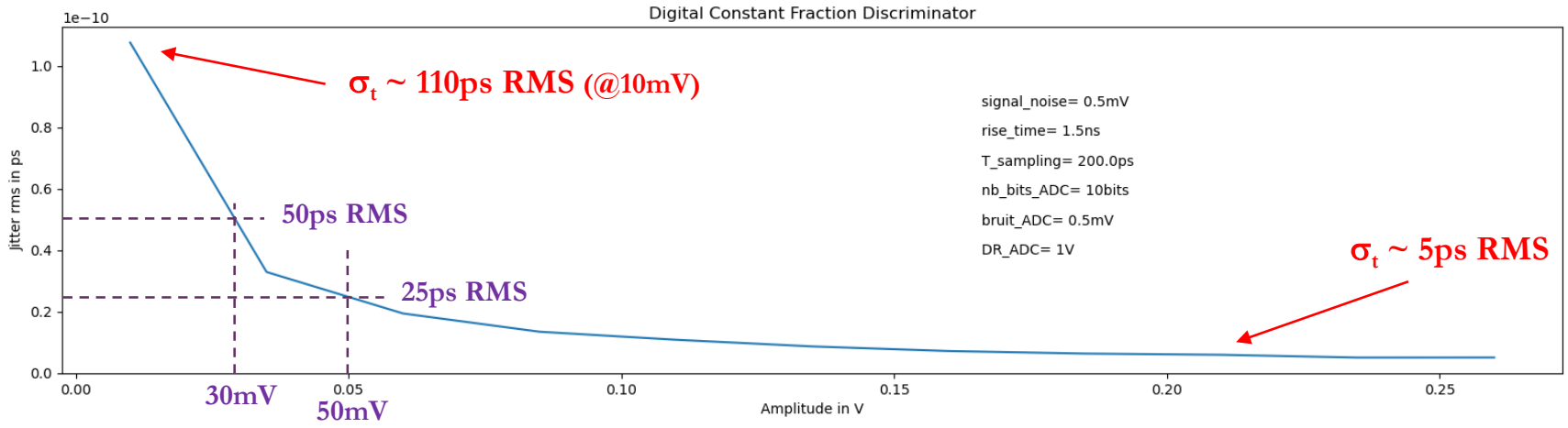


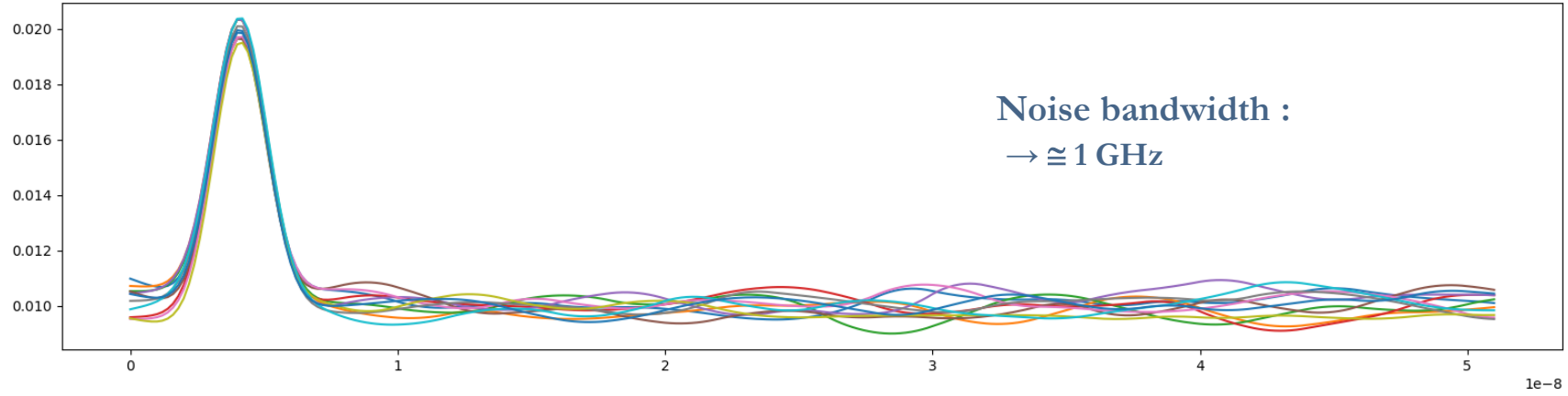
SIMULATIONS OF DIGITAL CFD (1)

Timing jitter versus signal amplitude :

rise time = 1.5ns ; σ_{noise}= 500µV_{RMS} ; σ_{SCA}= 500µV_{RMS}

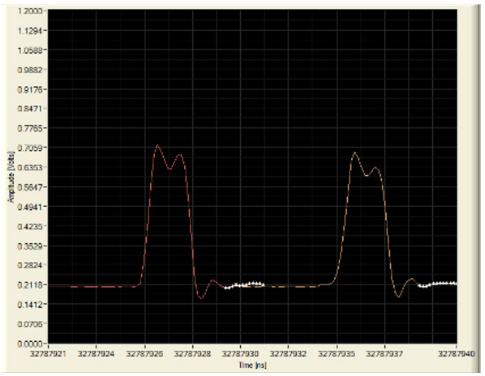
Here we use a **dynamic range of 100**, as required for ECAL:
=> Vin ranges from 10mV to 1V

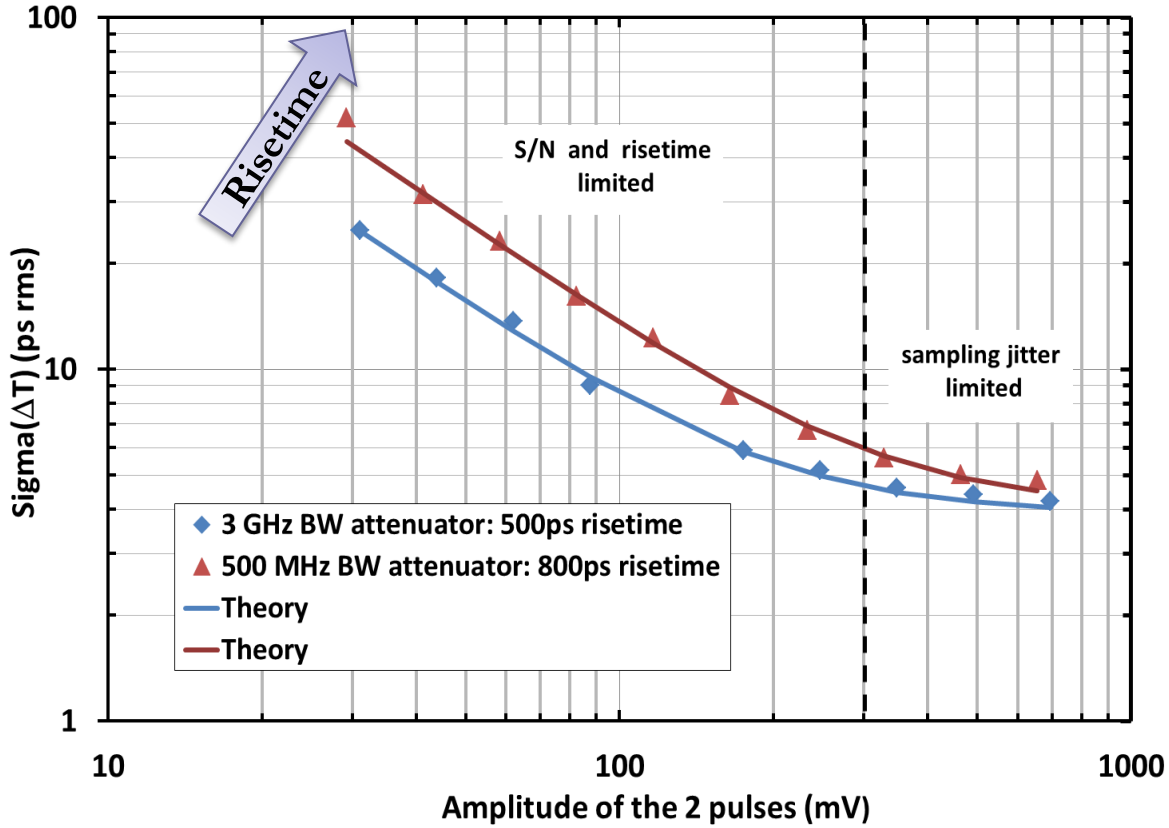




REAL MEASUREMENTS WITH DIGITAL CFD

Measurements performed with a **SAMPIC** (**Waveform TDC**) module: two pulses with 1-nS FWHM - 15 ns delay, digital CFD algorithm





Measurements consistent with the theoretical formula:

$$\sigma(\Delta t) = \sqrt{2} \times \sqrt{{\sigma_j}^2 + \alpha \times \left(\frac{\sigma_n}{Slope}\right)^2}$$

Assuming: :

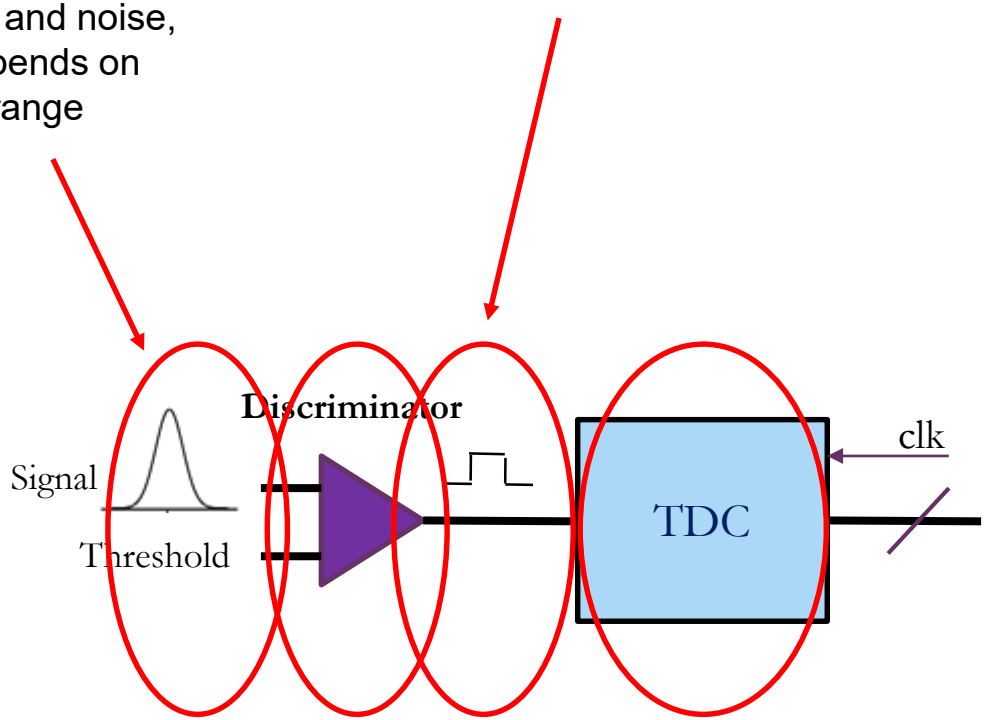
* Voltage noise σ_n = 1.1 mV RMS
* Sampling jitter σ_j = 2.8 ps RMS
* α = 2/3 (theory for perfect CFD)

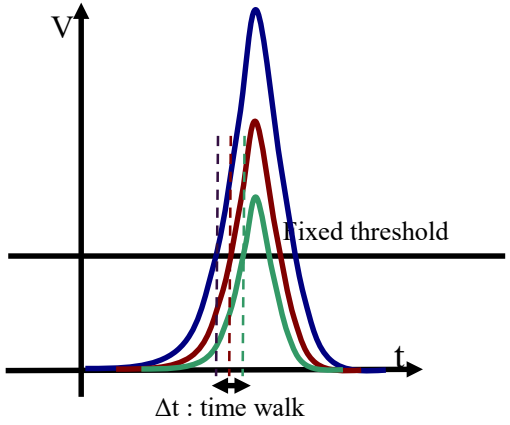
arXiv:1606.05541v1

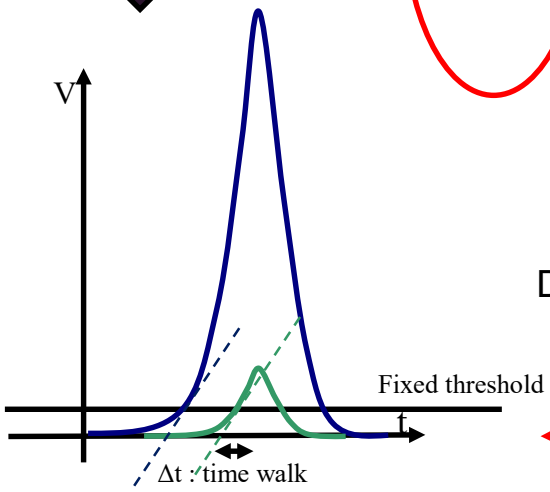
JITTER CONTRIBUTIONS IN A TDC CHAIN

Jitter from comparison signal vs threshold: depends on signal slope and noise, threshold depends on dynamic range

Effect of time walk: depends on signal dynamic range.
Can be partly corrected thanks to amplitude or charge measurement







TDC jitter (depends on time LSB, time INL residue, ...)

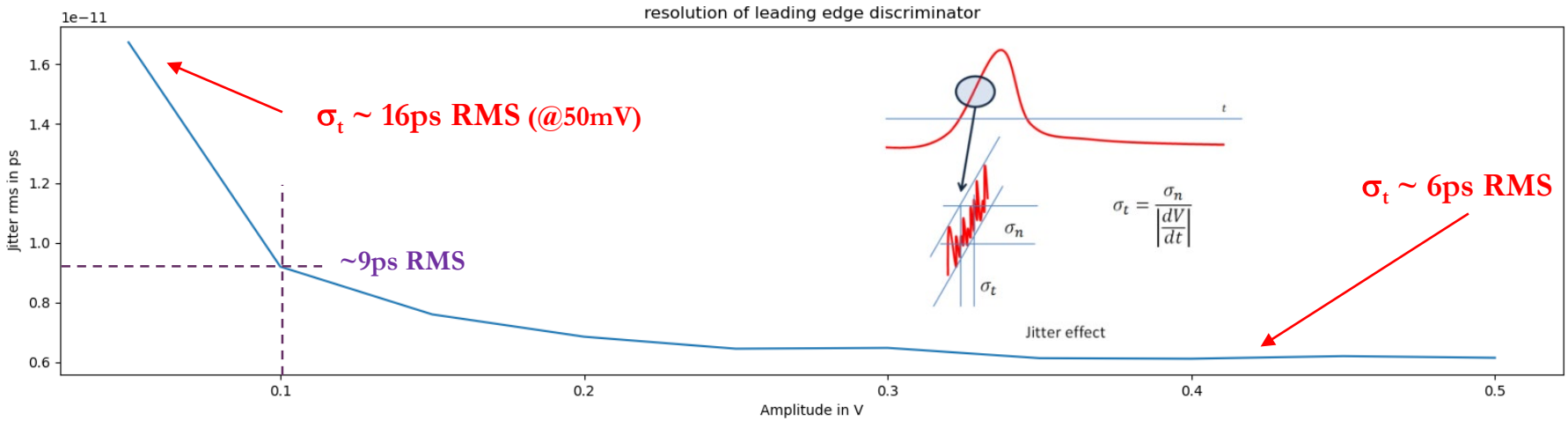
Discriminator's own jitter

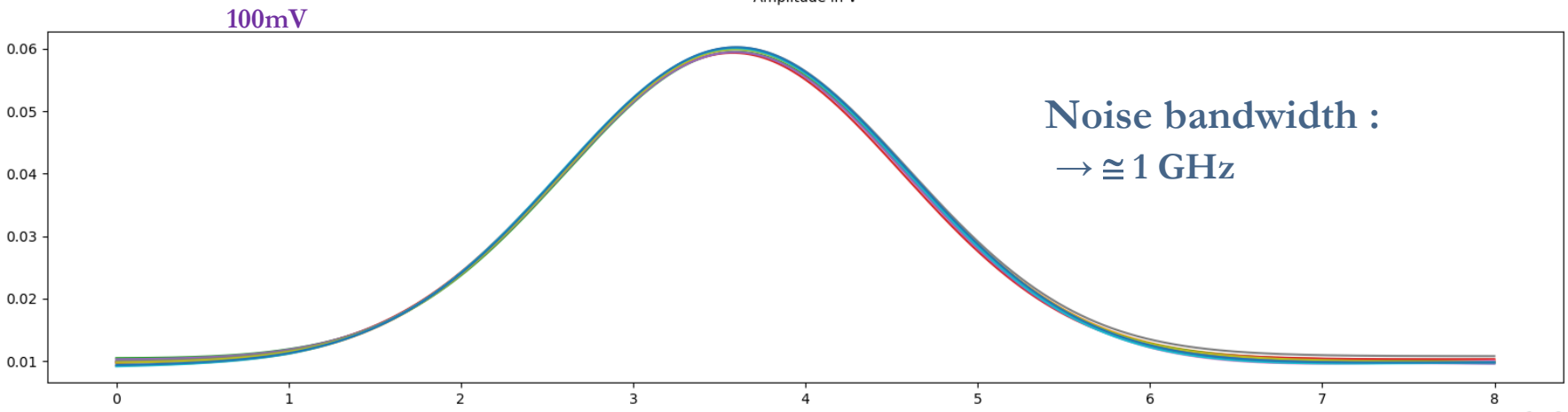
The key element is the slope at threshold crossing …

SIMULATIONS OF SOLE LEADING-EDGE DISCRIMINATOR (1)

Timing jitter versus signal amplitude : rise time = 1.5ns ; σ_{noise}= 500µV RMS

If the dynamic range was **of only 20**:
Vin ranges from 50mV to 1V
=> discriminator threshold is set at 25mV (half the minimum signal)

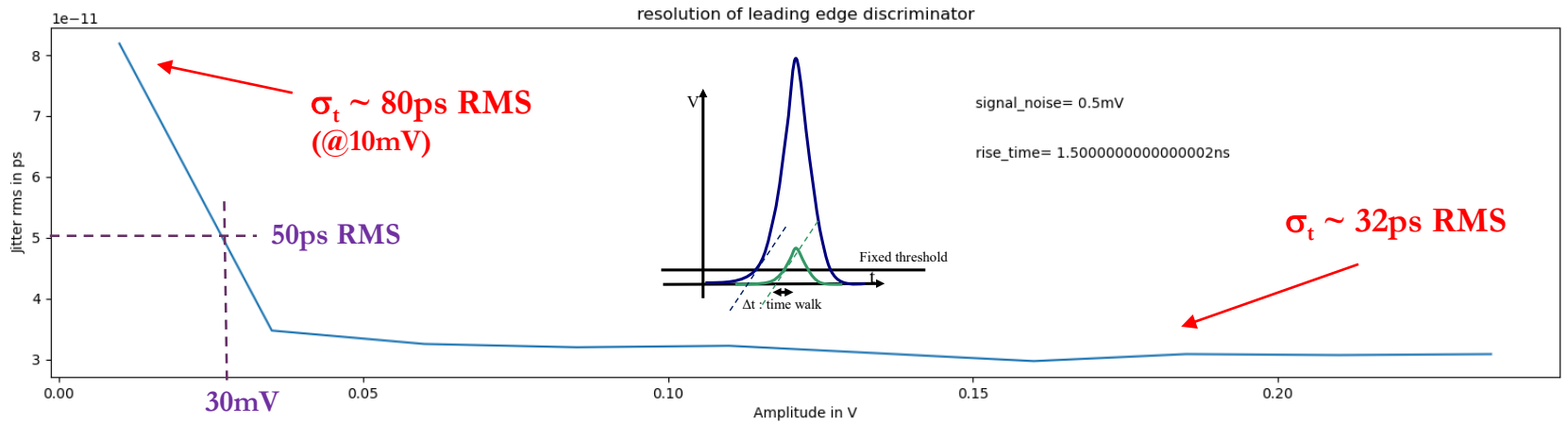


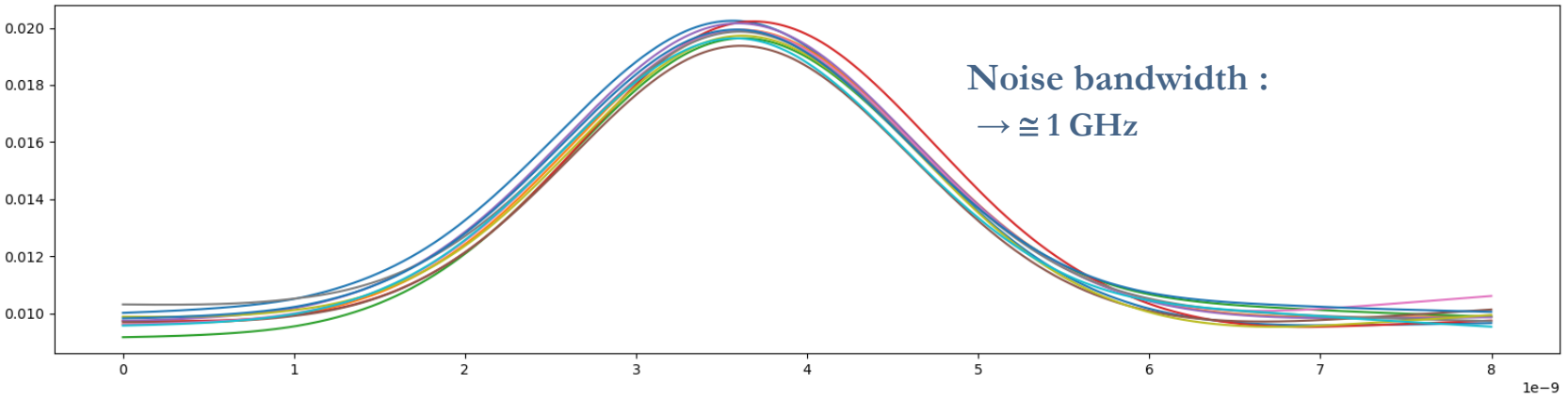


SIMULATIONS OF SOLE LEADING-EDGE DISCRIMINATOR (2)

Timing jitter versus signal amplitude : rise time = 1.5ns ; σ_{noise}= 500µVRMS

But **with a dynamic range of 100**:
Vin ranges from 10mV to 1V
=> discriminator threshold is set at 5mV (half the minimum signal)



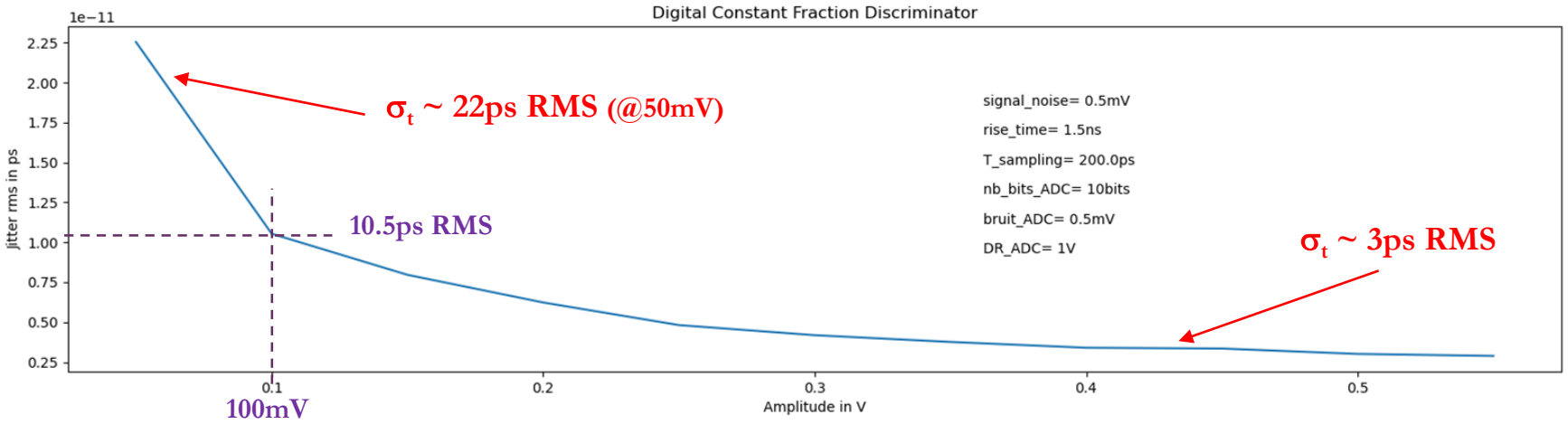


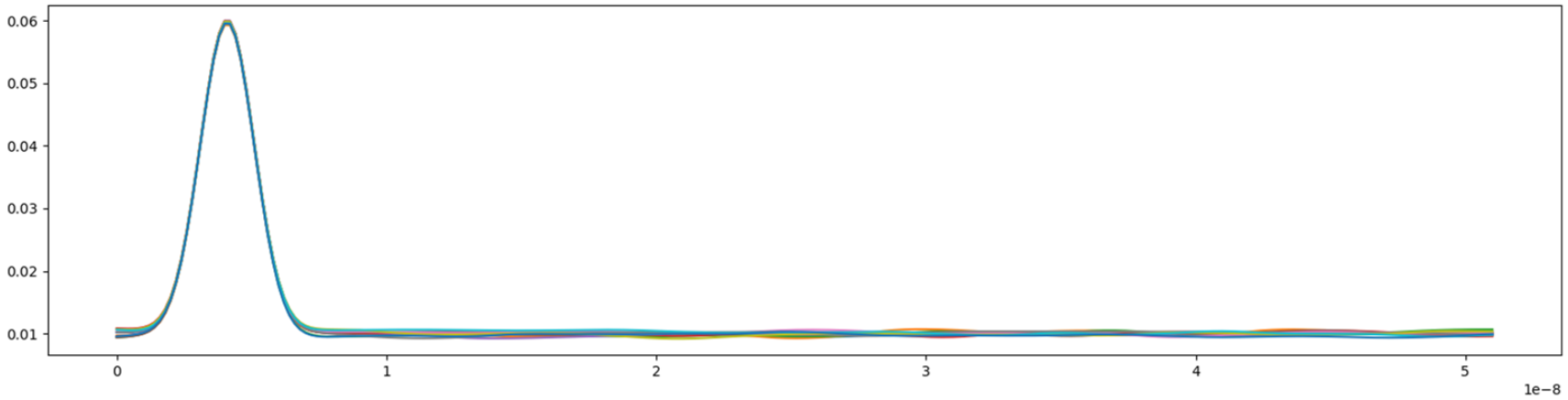
SIMULATIONS OF DIGITAL CFD (2)

Timing jitter versus signal amplitude :

rise time = 1.5ns ; σ_{noise}= 500µVRMS ; σ_{SCA}= 500µVRMS

Just to compare, here we use a reduced dynamic range of 20
=> Vin ranges from 50mV to 1V





SUMMARY ABOUT DISCRIMINATOR + TDC CHAINS

- The **discriminator + TDC chain** is well adapted for small or medium dynamic ranges, not for large ones
  - **Very sensitive to input noise**: the contribution of the sole discriminator is already higher than the electronics target (< 20ps rms) even for large signals if input noise is > 350 µV rms.
  - **Very sensitive to Time Walk correction,** especially with asymmetric edges (much slower falling edge which introduces jitter in TOT)
    - In the case of ECAL, we have the separate energy measurement which could help in this field (but its correction requires a cross calibration of energy and time) => hard to predict precisely

- **These problems have clearly been seen on ATLAS HGTD and CMS HGCAL**, even with smaller dynamic ranges than the one required for UII ECAL
  - They seem to induce noticeable limitations to the targeted time resolution

- The **other contributions** still and always have to be added (in quadrature):
  - The **discriminator noise** => low
  - The **TDC's own time resolution** => depends on the chosen solution (FPGA or ASIC), and of the complexity of its calibration

BACK TO SPIDER

- Conversely, **analog memories like SPIDER** permit covering **all types of ranges** with a resolution **much less sensitive to input noise and to other signal specificities**:
  - Their **own noise** adds up but is visible only for **small signals**
  - Their **own jitter** (low if well designed) becomes dominant only for **large signals**
  - **Calibration is simple** and all calibrations signals are **internally generated**
  - Time extraction algorithm could be adapted to **signal shape evolution** due to aging and irradiation
  - Obviously challenging but “safe” and robust solution, also compatible with dedicated timing layer option.