SPIDER “Swift Pipelined DigitizER”

for Timing Path Measurement

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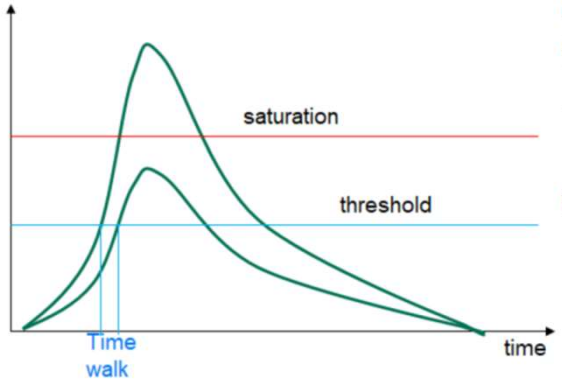
Plan

- ✓Requirements on timing path
- ✓How to achieve the specifications
- ✓SPIDER “Swift Pipelined Digitizer” asic
  - Concept
  - Architecture
  - Performances
- ✓Status of SPIDER development

Requirements on timing path

- Goal resolution down to $20ps_{RMS}$ to distinguish interactions
- Goal dynamic range E_T=[50MeV-5GeV]
- Assume maximum channel occupancy of ~10% (~4MHz), under study/sir
- Make it possible to deal with a few consecutive events (8?)



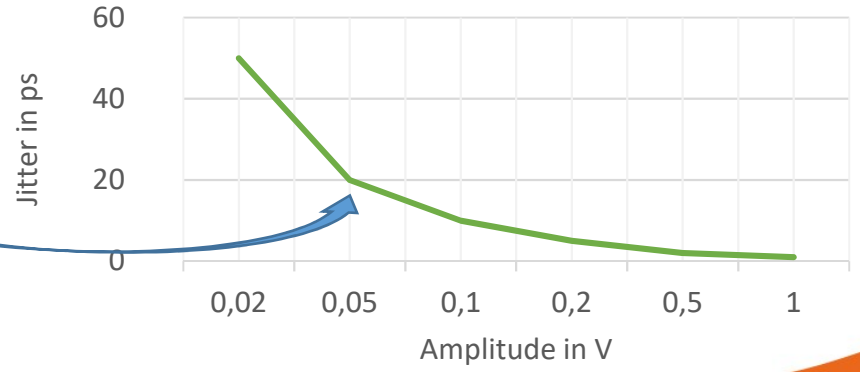
Challenging resolution : slowest edge of 5ns (for SpaCalW) with 1mV noise
→ jitter of 250ps

Theorical time resolution : $\delta_t = \frac{t_{rise\_time}}{SNR}$

For $\delta_t = 20ps$ and t_{rise_time}=1ns → SNR=50

→ reduce noise (technology/design)
→ reduce edge time (module design)

Evolution of the jitter with the amplitude of the signal (rise time =1ns, noise =1mV)



How to achieve the specifications

- **Key point : resolution 20ps$_{RMS}$ on a dynamic range of 100**

  ⟶ 2 types of time measurement chains frequently used

Plus vs Cons

1/ "leading edge discriminator + digital TDC "

- **- bad resolution for high signal due to slope effect because the threshold is tuned for the low amplitude (for large dynamic range)**
- **- time walk effect needs to be compensated (by TOT or energy measurement)**
- **++ high counting rate and low dead time**

2/ "Waveform TDC + digital Constant Fraction Discriminator"

- **- low impact on the resolution for low energy & ++ high resolution for high energy**
- **++ time walk effect strongly compensated (dCFD)**
- **-- limitation of the counting rate and of the significative dead time**

Dominique Breton's talk will explain in detail why "Waveform TDC" offers better performances and has been chosen...

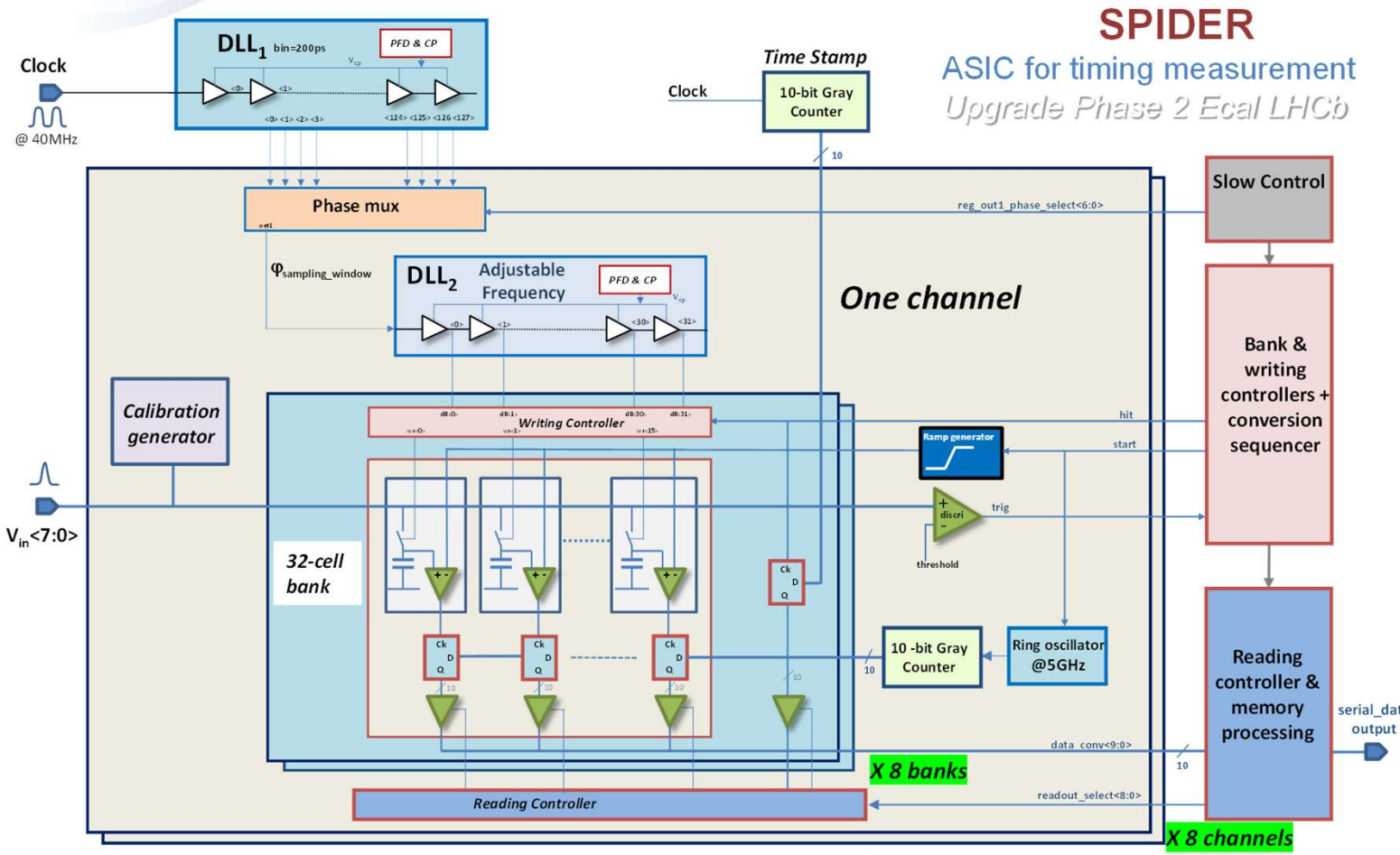
Concept of the « pipelined analog memory »

Reminder : a classical Waveform TDC is made of a <u>single circular memory bank</u> with a sampling depth of N signal points <u>which limits the counting rate</u>

- **To increase the counting rate, a multi-bank memory working like a pipeline is required and must run sequentially**
- **To implement multi-bank memory with a reasonable size per channel (physical constraints), we define a optimized sampling window to deal with only the interesting part of the signal, which consequently reduces the size of each memory bank**
- **To reduce the channel data rate, only the 8 samples required to make the dCFD calculation possible are sent to the companion FPGA**

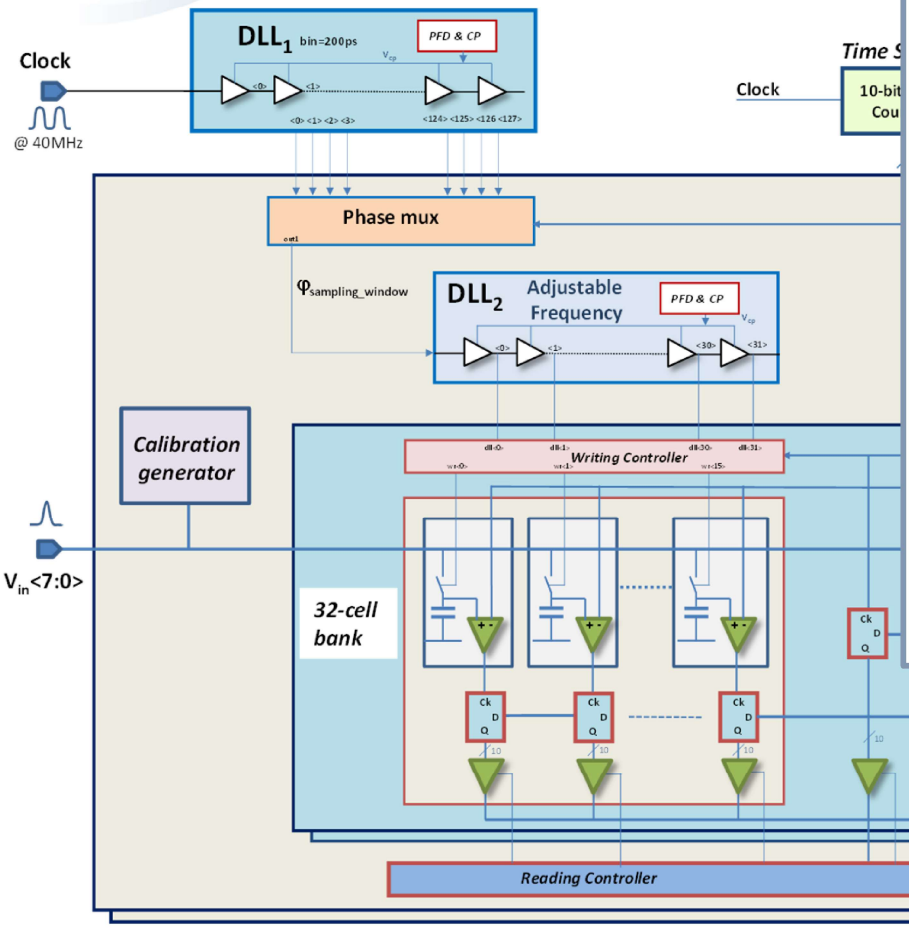
With this improvements, the pipelined waveform TDC is a good way to address the requirements on timing path

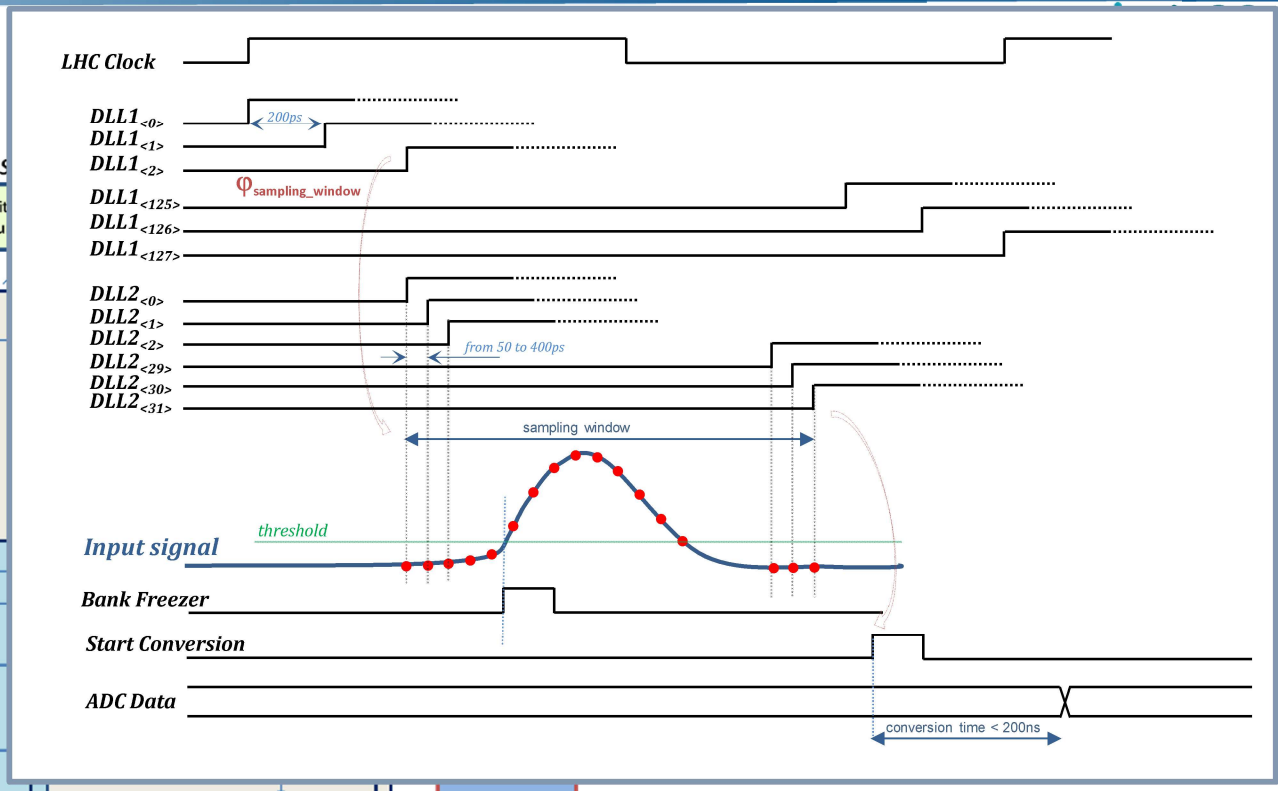
Architecture



SPIDER block diagram

Architecture





SPIDER block diagram

Main Specifications

- **Technology: 65nm (the most lasting technology, 10 years (?)), 1.2V power supply**
- **Input signal : rise time from 1ns to 1.5ns, dynamic range V_{in}=[10mV-1V]**

To achieve the time resolution of 20ps, we evaluate :

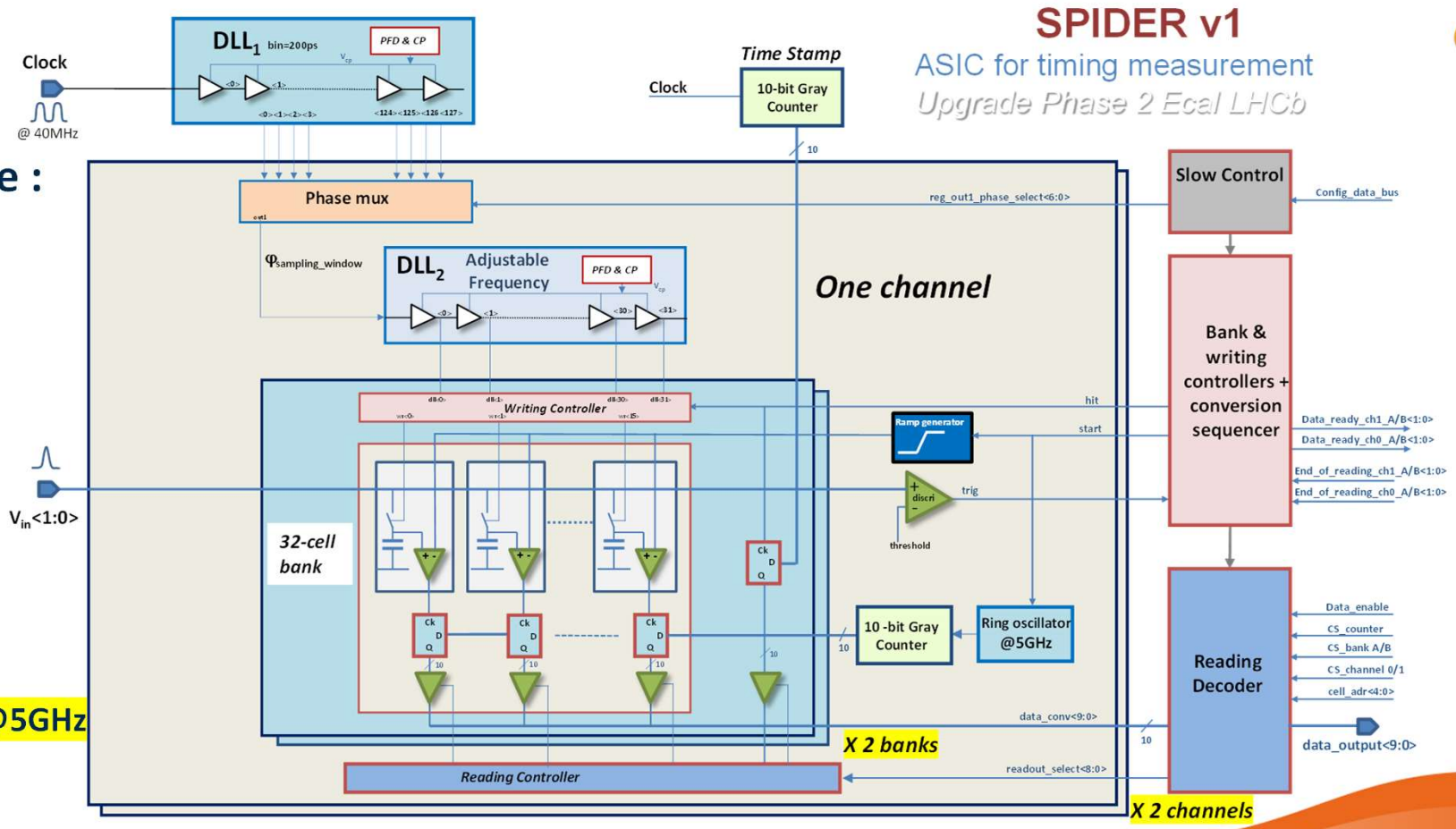
- **Need for a memory cell (switches & capacitor) compatible with a noise voltage around 0.5mV**
- **Need of a resolution of 10 bits for the sampling : 10-bit Wilkinson ADC@5GHz to reduce the conversion time (200ns for 10bits i-e 8 clock periods)**
- **Need for 128-delay-cell DLL1 running @40MHz → bin ≈ 200ps to tune the beginning of the sampling window**
- **Need for 32-delay-cell DLL2 running from 80MHz to 640 MHz → bin ≈ 50ps to 400ps to select the sampling frequency between 2.5GHz and 20GHz**

➢ Architecture: «2 dual-bank channels»

SPIDER first prototype : contains all critical blocks

Proof of concept :

- ✓ **Clocks & DLLs**
- ✓ **Memory cell in 65nm**
- ✓ **Multi-bank operation**
- ✓ **10-bit Wilkinson ADC @5GHz**



Status of the SPIDER development

- **Collaboration of 4 labs from IN2P3 (Clermont-Ferrand, Caen, Lyon & Orsay)**
- **Very challenging design! Has started a few months ago.**
- **Repartition in work packages for**
  1) **Delay Locked Loop (DLL1 & DLL2)**
  2) **Analog part (memory cell, trigger comparator, ADC comparator, ramp generator) + Sampling & ADC management (bank & writing controller + conversion sequencer)**
  3) **Counting digital part for "10-bit Wilkinson ADC & coarse time" (Gray counters, ring oscillator)**
  4) **Slow control & Readout management part (reading decoder)**
  5) **Phase Locked Loop (not critical for first prototype)**

The first prototype submission is expected at the end of 2023

Thank you for your attention!