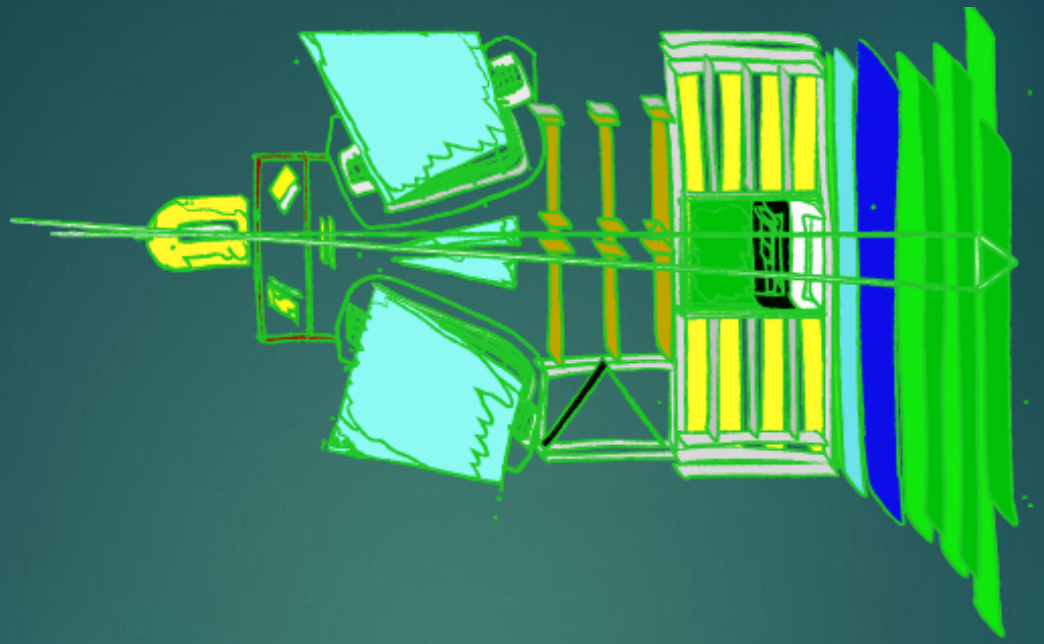


Front-End electronics

Christophe Beigbeder CNRS / IJCLab (Orsay, France),
on behalf of the Electronic Calorimeter groups

LHCb ECAL Upgrade II workshop. Orsay Dec 13th 2022

Outlook

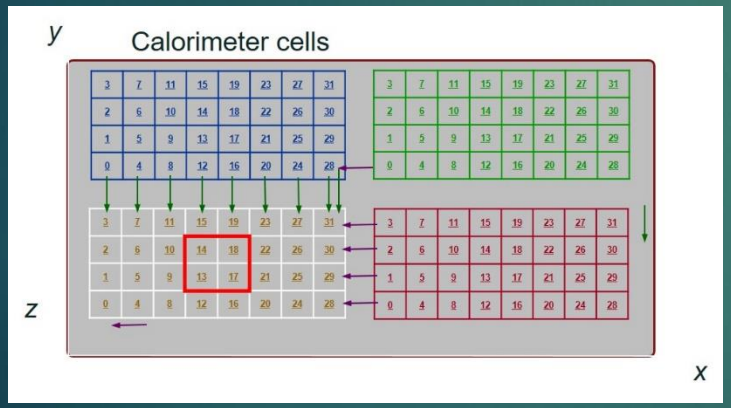
I. Present design
II. Proposed Architecture for upgrades 1b and 2
III. Project organisation
IV. Conclusion

Present Electronics Overview

- 8 + 2 Racks (ECAL,HCAL),18 Crates are situated on the calorimeter platform
  - Above and close to the detector : 10 kRad foreseen for the Run 3
- Commercial 9U crate. 3 max per rack, equipped with heat exchanger (water) and turbine on the top.
- Power supplies : specially developed by Wiener for the LHC projects . Radiation tolerant.
  - There are modules for low voltages on each crate.
  - In the bottom of the rack , RCM 380 to 48 V distributed to the Marathon Module
  - ~15 years old. Spares from dismounted sub-detectors (PS/SPD)
- Crate houses ~16 Febs, one Crate Controller and for some of them cards for the Led calibration system
  - 4 Slots potentially available for extra Febs to fully populate the crate
- The backplane powers and interconnects the boards for both slow control and signals coming from or going to other crates/racks to produce the trigger elements
- The Feb receives the 32 input signals via ~ 15 / 20 meter long cables from the HCAL and ECAL
- The system with 5 Fe boards and a dedicated firmware is also used for the Plume luminometer

Present Electronics Overview

- The Feb perform @ 40 MHz the energy measurement and a pre-processing for the trigger with the following :
  - The shaping and the integration of the analog signal -> ICECAL chip.
  - The 12 bit conversion thanks to a commercial ADC.
  - The processing of the signal in MICROCHIP (ACTEL) FPGAs
    - The pedestal subtraction and low frequency noise cancellation
    - The trigger primitives
    - The event formatting
- The Feb transmits and receives Fe/trigger data from its left and up side neighbours via the backplane (@40 MHz) and Cat5 cables (@280 MHz) for 280 In/Out bits per board

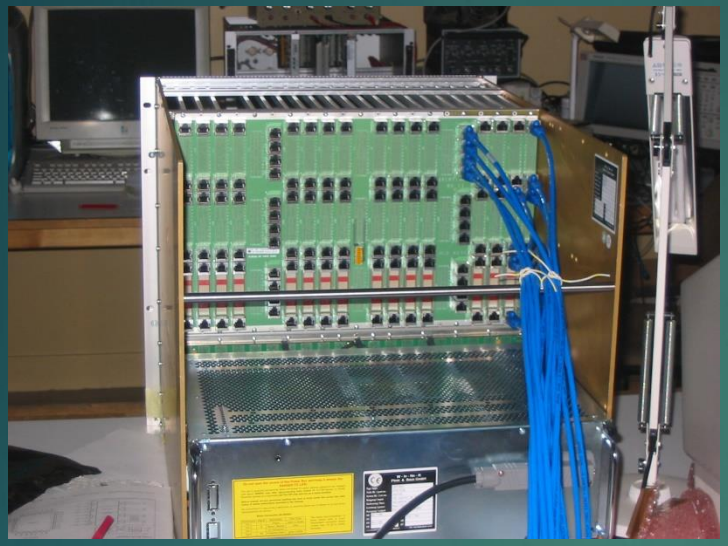


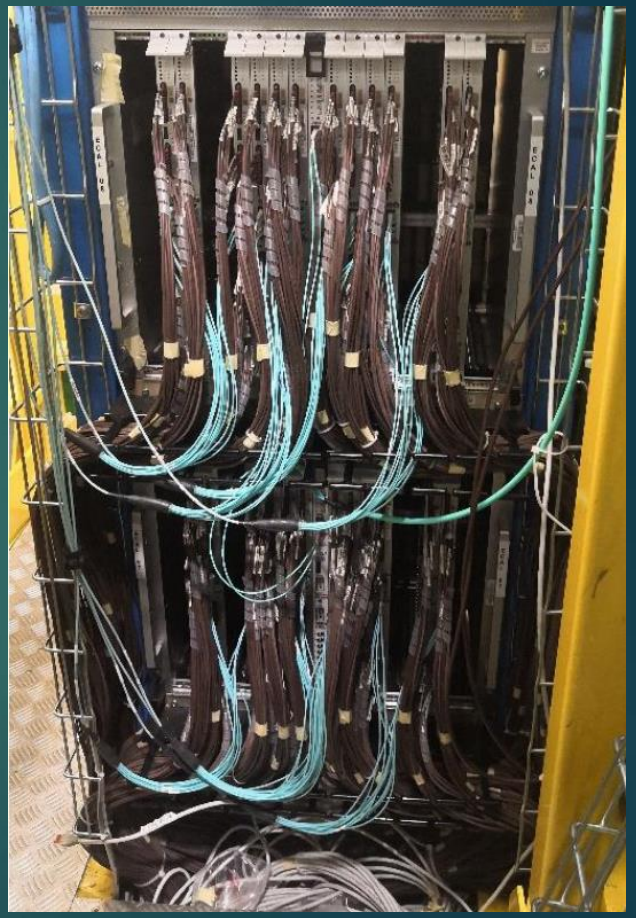
- Each board calculates the Energy of each of the 32 clusters (ET) then extract the cluster with the Highest Energy and its corresponding address, the Total Energy per board and determine the Multiplicity, how many channels are above a defined threshold.
- The trigger algorithm needs to concentrate all the data in a single chip to process the 45 X 10 bits. Actel - Igloo2- MG2L150 - 1152 pins

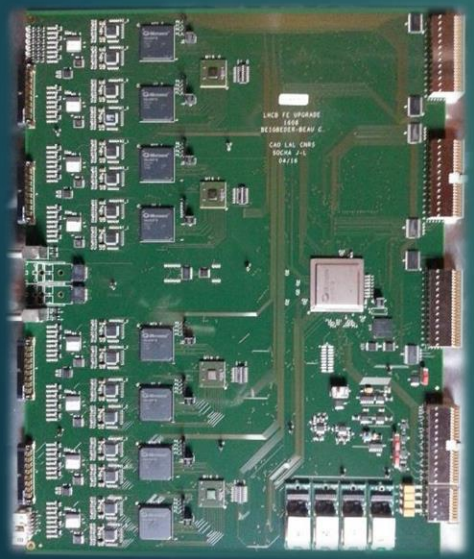
- The Feb transmits Fe data (energy/channel) together with the trigger elements and the reduced BXID to the DAQ after serialization by GBT (112 bits@40 MHz) and 4 links to the PCI 40

- ~ 300 Fe boards and 25 Crate Controlers was produced

Electronics for the upgrade1b&2







Electronics for the upgrade1b&2

Start discussion beginning of 2021

One meeting @ CERN during LHCb week

three calorimeter brainstorming meetings

https://indico.cern.ch/event/982989/

https://indico.cern.ch/event/968608/

LHCB Upgrade2 electronics kick off meeting by Ken @ CERN

LHCb Upgrade2 electronics workshop in June 2022

Since mid 2022 : Regular monthly meeting on chip design and reporting during Calorimeter meeting and LHCb week

Electronics for the upgrade1b&2

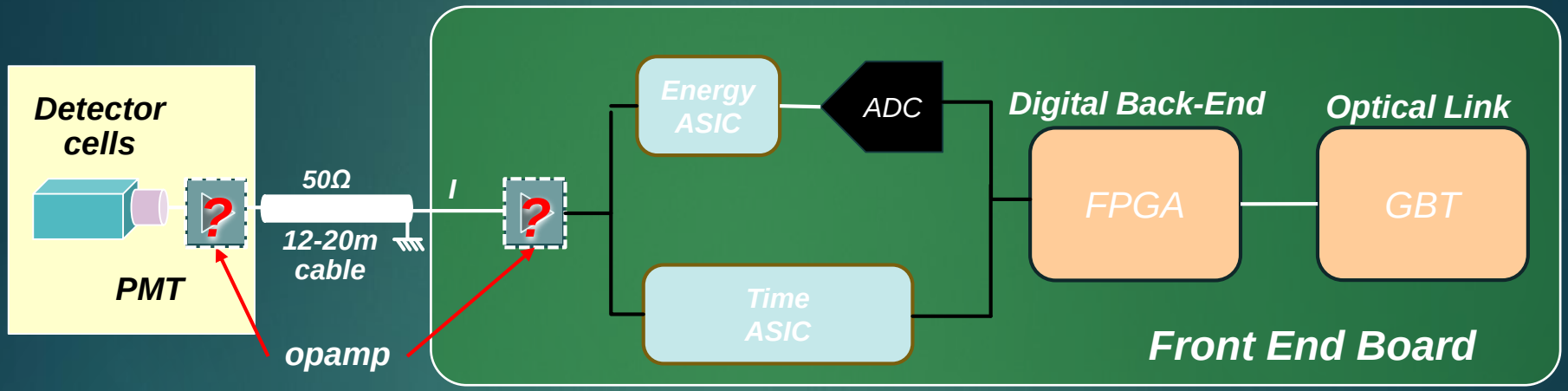
- Current participants : *6 Labs , 2 are not members of the LHCb collaboration*
- IJCLab, Orsay (contact : Christophe Beigbeder).
- ICCUB, Barcelona (contact : Edu Picatoste).
- LPC Clermont-Ferrand (contact : Samuel Manen).
- IFIC, Valencia (contact : José Mazorra de Cos).
- IP2I, Lyon (contact : Hervé Mathez).
- LPC Caen (contact : Laurent Leterrier)
- Funding :
  - IN2P3 R&T (50 K€ granted), 3yrs (1st prototype).
  - R&D&I Complementary Plans of the Spanish Government. European Union–NextGenerationEU (granted at ICCUB, requested at IFIC).

Electronics for the upgrade1b&2

- Key parameters
  - Produce time measurement in the range of ~ 20ps (signal dynamic dependant)
  - Number of channels: ~30000 (double side readout)
  - Trigger less architecture
  - Occupancy: Time measurement on a signal over a threshold for a targeted occupancy of 10% in average.
  - Dynamic range : 50 Mev-100 Gev of transverse energy for Energy measurement and 50 Mev- 5 Gev for the timing
  - Energy measurement on 12 Bits every 25ns (no zero suppress)
- Constraints and consequences
  - Total dose: ~100 Mrad in the hottest region.
  - 40 KRad on the platform for for 300 fb^{-1} offer the opportunity to use a large choice of components or Asic technologies
    - FPGA : Microchip or Xilinx
    - Use of commercial components possible after radiation hardness qualifications.
    - Less material and electronics on the detector
  - We have to stick to the production of the CERN components :
    - ~ 2 steps for the developments according to the LHC schedule

Electronics for the upgrade1b&2

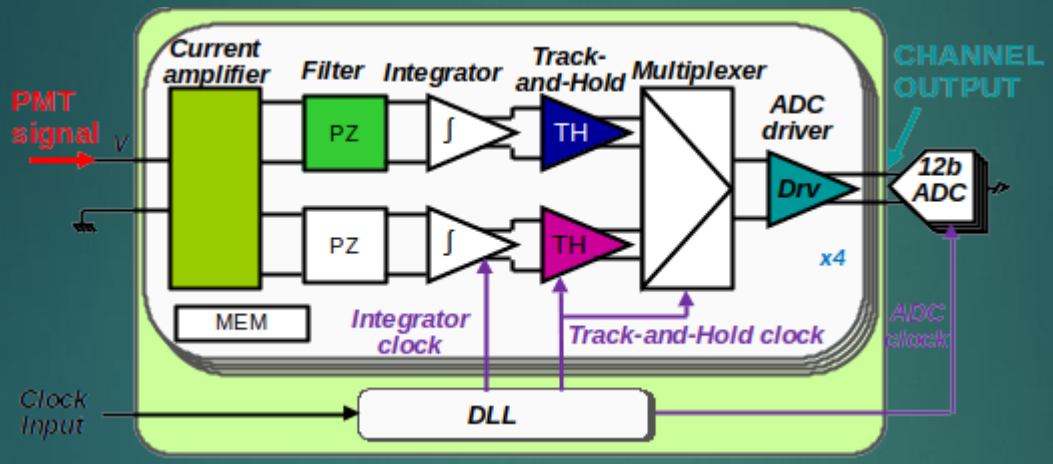
- Chosen architecture



- Two separate processing paths with dedicated Asics in the same techno 65 nm :
  - Energy path close to the current ICECAL scheme (mostly analog processing)
  - Timing path based on a waveform TDC.
  - For dynamic range compatibilities, cable attenuation, Signal range Gain , noise, BW requirements:
    - Amplification and shaping either at the PM level or on the FEB
    - Opamp stage + dedicated passive attenuator for each ASIC could provide the optimal signal conditioning (see Edu's talk)

Electronics for the upgrade1b&2

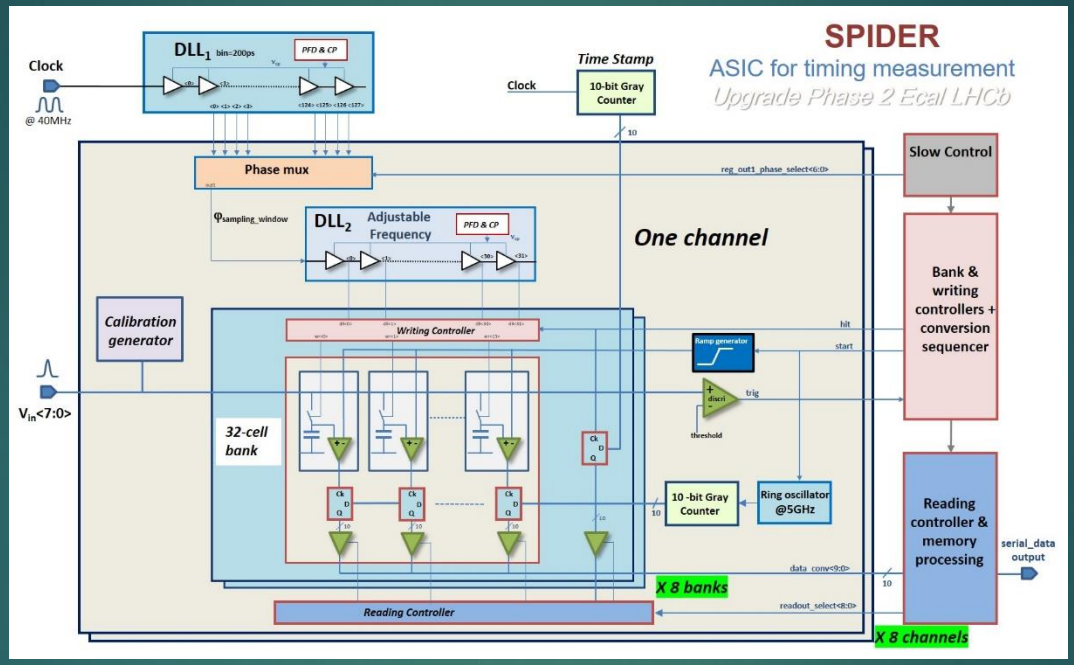
- Energy path based on the evolution of the ICECAL chip



- New design but keeping the same principles and functionalities of the ICECAL
  - Dual gain to cover the large dynamic range
  - Integrating the 12 bits ADC is under consideration
    - See next talks on "ICECAL II " by Jose

Electronics for the upgrade1b&2

- Timing path based on the SPIDER chip



- TDC : analog memories based on switched capacitor arrays (SCA)
  - 50-400 ps binning. 3 ps resolution for ~1ns rise time at the optimum amplitude.
  - Pipelined architecture to reduce dead time and match the average occupancy
  - Adjusted window of interest to reduce readout latency and techno size constraints.
    - See next talks on SPIDER by Philippe and requirements for precise time measurement by Dominique

Electronics for the upgrade1b&2

- The Front end processing part
  - Use the radiation tolerant Microchip PolarFire chip, tested up to 400 kRad
  - Receives the energy information from the 12 bit ADC as it's presently done
  - Process the charge information keeping the same as actual
    - Pedestal subtraction and low frequencies noise cancellation
  - Receives the timing information by serial links, for each of the channels
  - Process the timing information
    - DE serialized the data streams: samples and coarse counter (reduced BXID)
    - Extract the time thanks to an embedded digital CFD
  - Associate the charge to the time by comparing the FPGA BXID counter and the reduced BXID coming with the SPIDER data (derandomizer)

=> Is the actual system with links between cards and crate still needed : to keep, to ameliorate ...

  - For timing correction for adjacent towers
  - For Trigger primitives
  - For any pre processing, using the FPGAs

= > This has a real Impact on the design of the whole system

Electronics for the upgrade1b&2

- Steps for the electronic upgrades : RUN 4 (2029)

  - Inner part : Channels are in " Inner crates" not mixed with middle and outer part of the detector and could be housed in the same crate with non replaced Inner channels .
    - ~3500 single side readout in place of the ~1000 , ~2500 channels / 80 boards .
    - ~ 110 Fe boards mechanically identical to the actual ones with 32 channels inputs for connectivity reasons, housed in ~ 7 crates (5 coming from PD/SPD)
    - CC- Crates – Power supplies – Cooling should be kept as the rest of the electronics
    - Cables : may use of the existing one
    - Use of the CERN new components, already available for evaluation
      - lpGBT (10 Gbits) . Optical drivers
      - PCIe 400 version1 (see Julien's talk)
      - The 2 systems has to be compatible
        - PCIe400 – Crate controller
        - Data format : New Calo firmware for the PCIe 400

  ⇒ Feb design closed to the existing one in term of architecture and integration

  ⇒ Run two systems : latency , data format

  ⇒ Planning is quite aggressive specially for the Asic developments and production

  => Option of upgrading the electronics like it is done for the run5 has to be studied (other scenario)

Electronics for the upgrade1b&2

- Steps for the electronic upgrades : RUN 5 (2035)
  - A complete redesign of the system
    - ~15000 double readout channels including the Inner part
    - ~ 32 000 cables => Make sure it's possible otherwise we have to change the complete philosophy of our design
    - 472 Feb (64 channels) and 30 Crates
    - Extension of the platform necessary
    - New crates
      - New backplane with connectivity for the analog signals coming by the rear side of the crate ; possible signal interconnections between crates
      - New power distribution backplane
    - New power supplies : active participation with CERN already welcomed
    - New DAQ and new crate controller

⇒ Feb design is based on the RUN 4 developments even if the topology is completely changed

⇒ Asic production and schedule looks ok (large gap between run4-run5)

⇒ Schedule for Run5 looks more "comfortable" than for Run 4

Project schedule and organization

- ASICs : Technical organization is ready for the two developments
  - All the WP are covered for the two chips
    - IN2P3 labs for the timing
    - Spanish labs for the energy
      - No problems for sharing part of the design between labs
      - Possible integration of the chips in a single one
  - Confidentiality rules concerning certain parts of the design has been fixed
  - Asic for timing
    - End 2023 : first prototype with 2 channels
    - mid 2025 : second prototype with the definitive pinout
    - Mid 2027 : Production for the 3500 channels ie ~450 chips
    - End 2031 : Production of the latest version :
  - Asic for Energy
    - ~ Same schedule than the ASIC for the timing.
- Test bench : develop together with LPC based on the Sampic test bench
- Test bench for ICECAL will be similar to the present one in Barcelona
- Test beam : dedicated board with Microsemi FPGA and version 1 of the SPIDER

Project schedule and organization

- Fe board for Run 4
  - Can start already with the present manpower at IJCLab and LPC
  - Start implementing all CERN components LpGBT - Optical Drivers
  - First version on 2025 following the Asic developments to be ready for 2028
    - fabrication Installation and commissionning in 2028

- Fe boards for Run 5
  - Production for ~ 400 boards and commissionning takes several years based on our experience on the development of the electronics for Run 1-3 and needs manpower
  - Discussions has not already started on :
    - Crate controller
    - Backplanes
    - Cables and connectors studies
    - Power supplies
    - Crates- Racks
    - Cooling

⇒ Part of it was the CERN responsibilities specially for Run1. What can we expect from CERN now

=> Manpower is missing on all this topics regarding the possible involvement of the labs already in the project. Labs has to integrate to the project as soon as possible

Conclusion

- The architecture of the electronics is almost defined and Asics developments have already started
- Still on–going studies and questions concerning the very Front-end, PMT base and signal distribution to the two ASICs, single or dual gain ....
- The time resolution is mainly dominated by the Detector performance (dynamic, rising time, noise)
- The schedule is quite tight for the Run 4 specially for the Asics developments and consequently for the boards
- The different scenarios for Run4 need to be evaluated carefully
- Open the collaboration to other labs is absolutely necessary to face all the developments needed specially for Run 5