Some very preliminary thoughts

Implications on integration, electronics, DAQ

Some initial thoughts for discussion

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Goals for the imaging/timing layer(s)

Imaging calorimeter helps, see Zhengwei's presentation

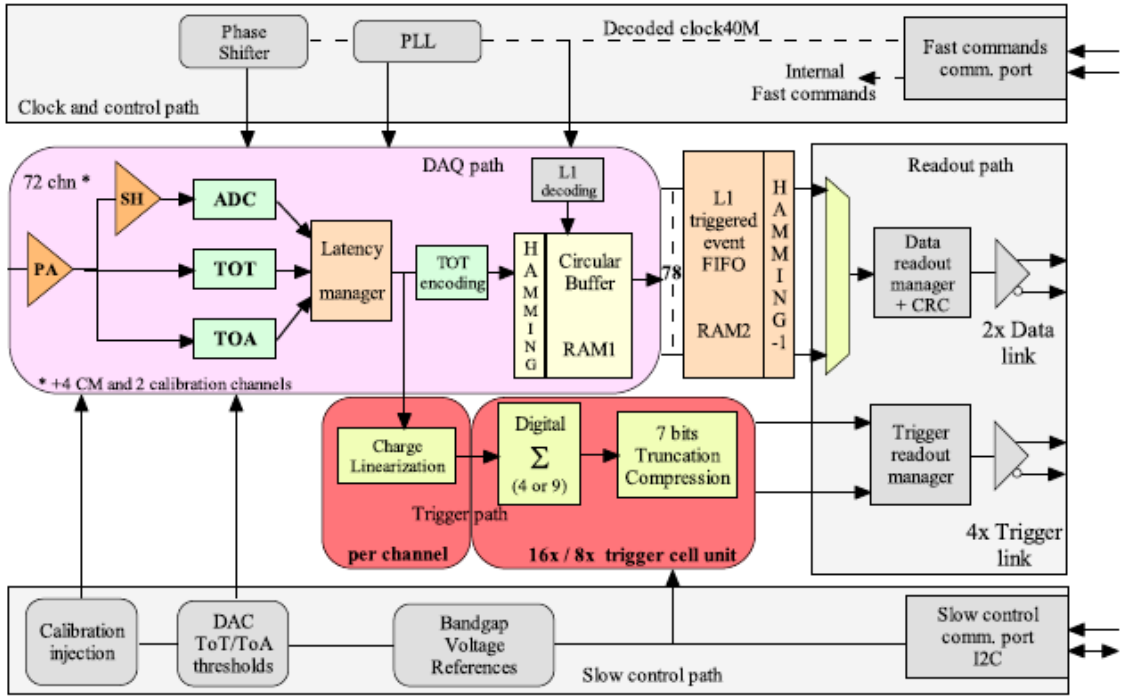
- Focus: upgrade II, operation with high-pileup & some residual spillover that affect the time resolution
- Higher granularity helps in pattern recognition for adjacent showers/particles
- Assumptions: we can remove the constraints of having the front-end processing at the periphery allowing us to fine-tune the detector segmentation to the imaging/timing goal⇒associate a precise 4d coordinate to each shower:
  - electron identification,
  - disentangle merged π^0/electrons/single photons
  - Particle ID with time of flight

Starting point: learn about different architectures

Dominique Breton's talk yesterday gives an interesting perspective on this

- Which FE architecture?
  - Integrate TDC in front-end (e.g. HCGROC, courtesy of C. de la Taille)
    - Less processing downstream
    - Optimized for digital calorimeters with cell size comparable to the ones envisaged for the timing/imaging layer
  - Digitizing architecture: take as many samples as needed (Aardvarc from Nalu Electronics)
    - Better estimation of the overall charge without the need for shaping (another source of pile-up)
    - Use of the full waveform information for timing extraction
    - Robust method for pile-up suppression can be implemented

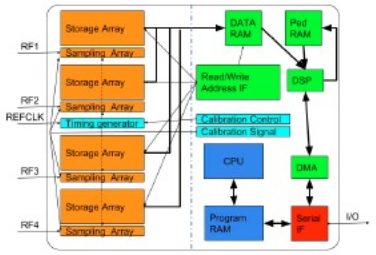
The readout architecture I: ADC/TOT/TOA (e.g. HGCROC)

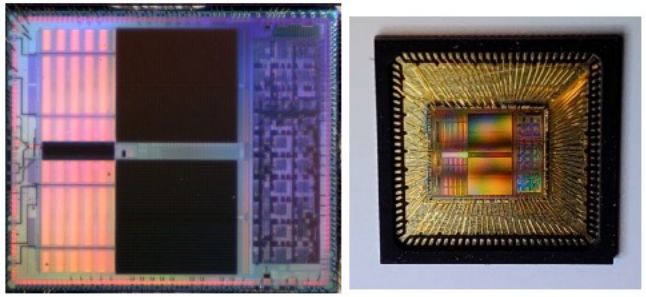


- Front-end architecture using ADC and TOT for charge information and TOA for time-stamp
- Discriminator allows for zero suppression
- Common mode suppression algorithm mitigates noise possibly induced in distributed systems
- Use of a fixed threshold discriminator deteriorates time resolution for larger pulse heights Dominique Breton's talk yesterday

Multisampling option to be studied (with LAPPD, possible variant for LGADs/Si option)

AARDVARCv3





Designed for high rate experiments in independent streaming mode

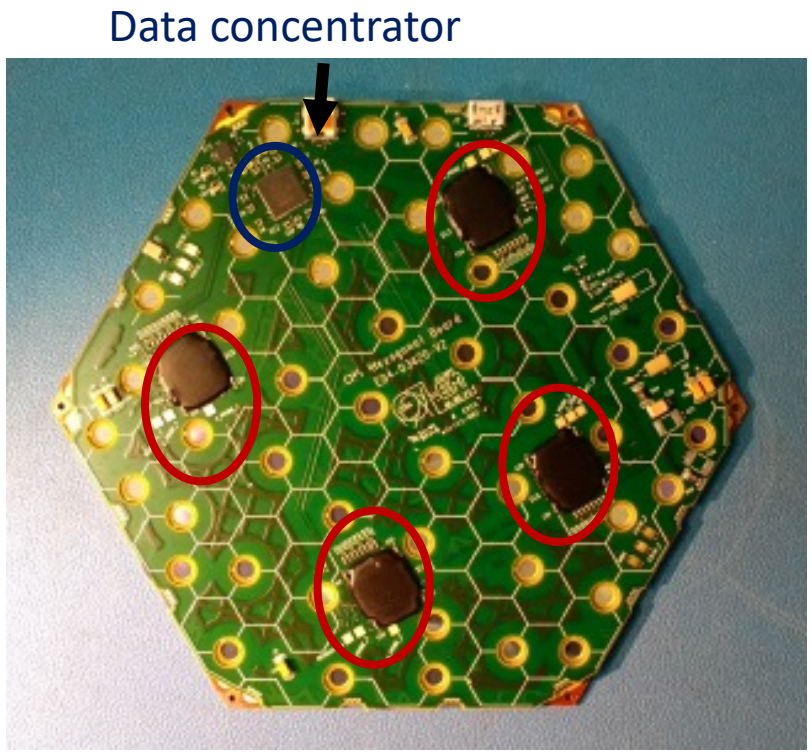
1. **Setup**: Using RxIn, or parallel interface, the analog and digital parameters are written
2. **Acquisition**: data is continuously sampled and stored in round robin fashion in 256 (128 for rev4) windows of 64 samples -
3. **Triggering Digitization**: using either external trigger or self-trigger (possibly combination of channels)
   a. Interval around the trigger is selected
   b. Windows in the interval is digitized (only "marked" windows if in ROI mode
4. **Readout**: As soon as data is ready:
   a. Data from digitized channels and windows are sent all 16 channels via the serial interface *Tx*, using the TxClk
5. Back to 2. Wait for new trigger

Using the banking system, phases 2 and 3+4 can overlap (on different regions) thus permitting dead-free operation.

Note: it requires a collecting node always ready to receive data

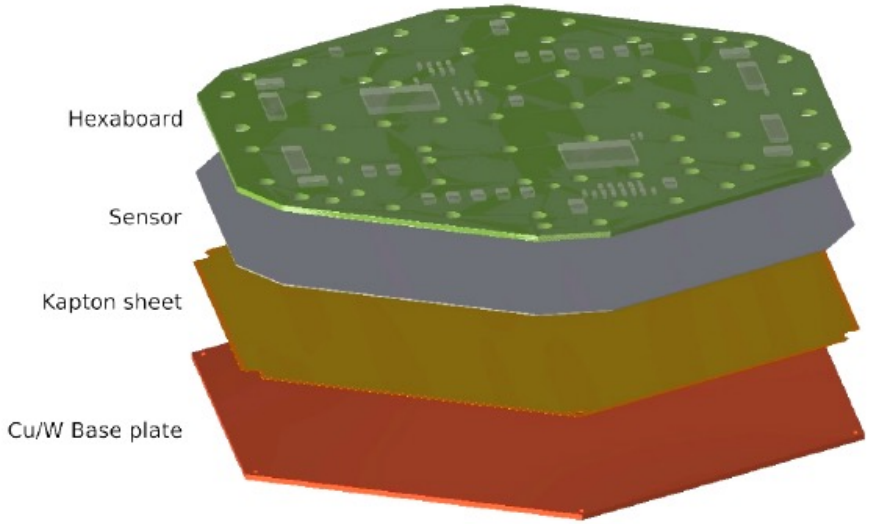
Some numerology

- 1 detector plane is 1050 20 cm X 20 cm tiles (LAPPD) or 4200 10 cm X 10 cm tiles (Si)
- A 10x10 cm^2 tile can be organized into 4-100 channel readout chips + 1 data concentrator/processor chip
- A large but manageable system



System aspects

- System aspects to be understood:
  - Routing of power (LV/HV)
  - Data flow architecture & data format and connections with readout boards
  - Packaging and interconnectivity
  - cooling
- It is a challenging task but may enable new physics opportunities



Conclusion

- Initial thoughts on how to achieve a detector plane/detector planes to provide high spatial resolution/precision timing combinations
- Pursuing this project may lead to new ideas to implement in the "baseline design"
- This effort is synergistic with a broad R&D program picking up steam in the US and may lead to a broadening of our community