Energy ASIC for ECAL Upgrade II

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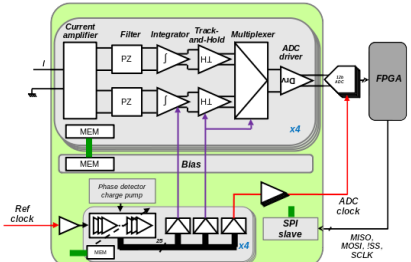
Introduction

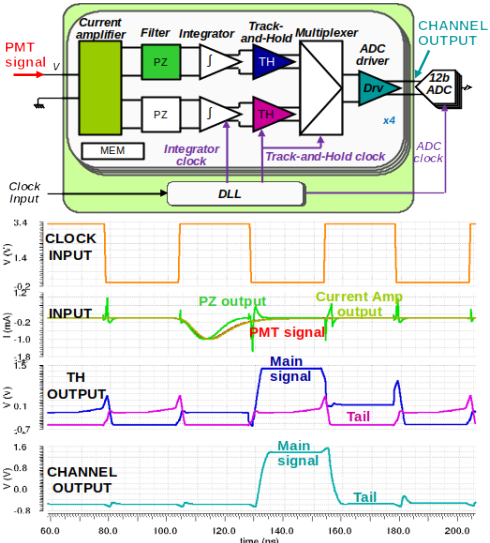
- Energy measurement for ECAL UII following current ICECAL architecture.
- Resolution of 12bit required with 1V supply → noise below 250µV
  - two parallel processing chains with different gains.
  - internal discriminator for automatic gain selection.
- No dead-time operation with in-channel integration and sampling.
  - dual gated time-interleaved architecture to allow reset time.
  - switching noise → differential signal as soon as possible.



Analog Processing

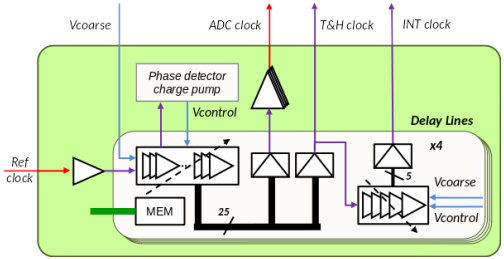
Analog processing chain:

- Input Stage:
  - voltage input mode (high Z)
  - low noise + high bandwidth
  - single ended to differential
  - four independent signal outputs
  - extra discriminator output
- PZ cancellation Shaper:
  - minimize spillover
  - tunable pole and zero
- Integrator:
  - tunable feedback capacitor
- Track & Hold:
  - high slew rate



Synchronization

- Digital conversion syncrhonized from inside the chip.
  - Dedicadted DLL per channel.
- Three separate phases for integrator, track & hold and ADC.
- Predictable subchannel selection after reset/power-up.
- Internal digitization is also considered but low priority.



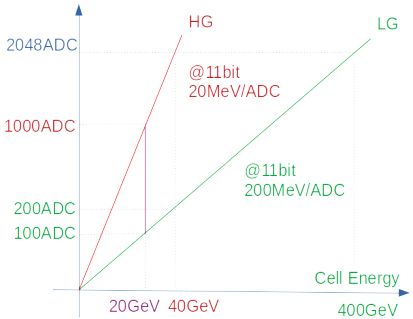
Specifications

- Initial approach: assume similar specifications as ICECAL.
  - Energy range(E_T): $0 - 10 GeV/c$,
  - Calibration HG: 20MeV/ADC*,
  - Calibration LG: 200MeV/ADC*,
  - Dynamic range: $12 bit$,
  - Noise: $< 1 LSB$,
  - Shaping: $25 ns$(99% of the charge),
  - Spillover residue level: $\pm 1\%$,
  - Linearity: $< 1\%$,
  - Crosstalk: $< 0.5\%$,
  - Termination: High Z,

  *proposal under discussion.
- Sampling phase tunable per channel with dedicated outputs per block.
- Pedestal subtraction from previous event.
- Data transmission at 40MHz, continuous readout with no deadtime.

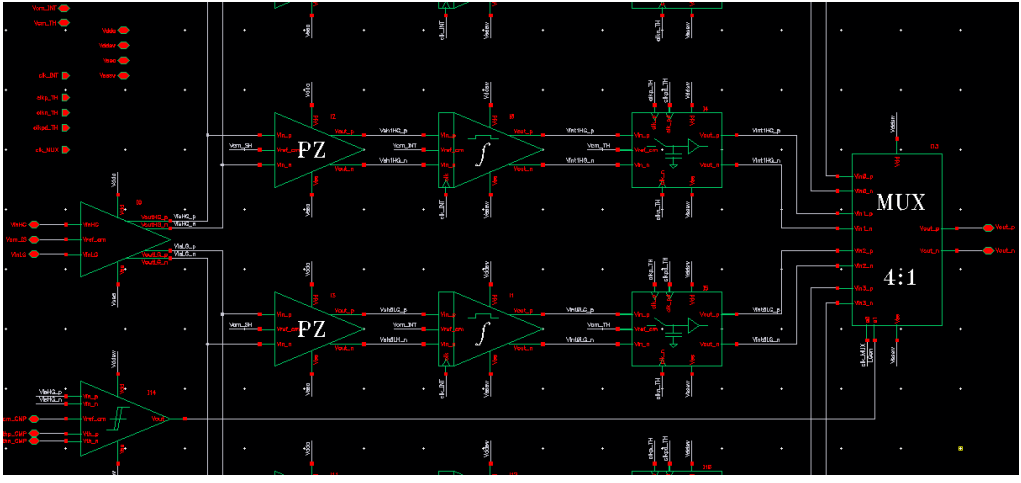
Calibration

- Two gain system requires separate ranges with different calibrations.
- Relative error spikes directly above transition energy (LG side).
  - Low Gain: maximum cell energy for 10GeV E_T with full containment.
  - High Gain: trade off between gain ratio and low energy resolution.
  - Transition: energy value should minimize impact on physics.



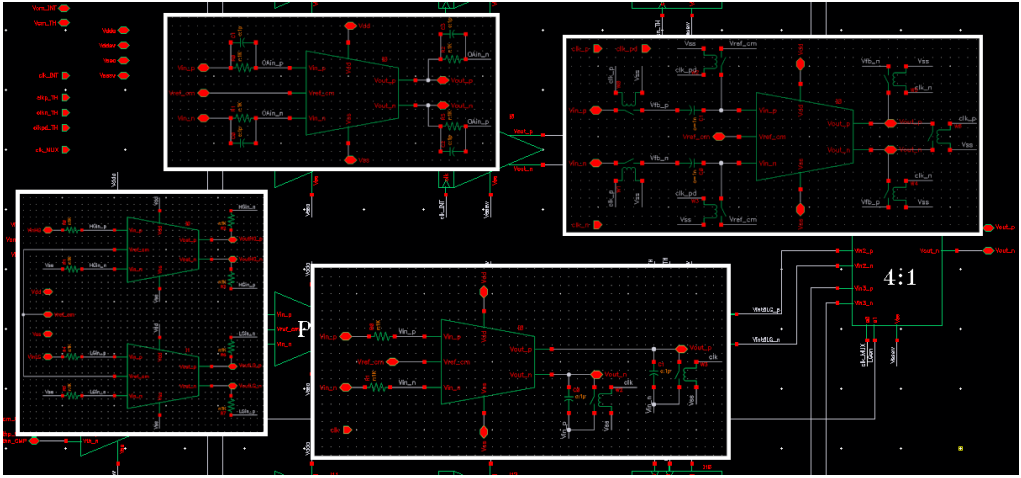
Energy Channel

- Hierarchical schematic for the energy channel.



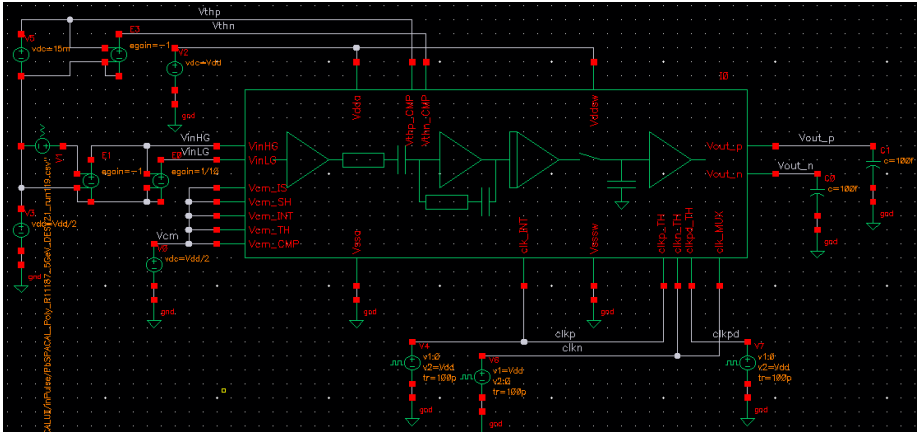
Energy Channel Blocks

- Block schematics using ideal blocks (OpAmp macromodel).



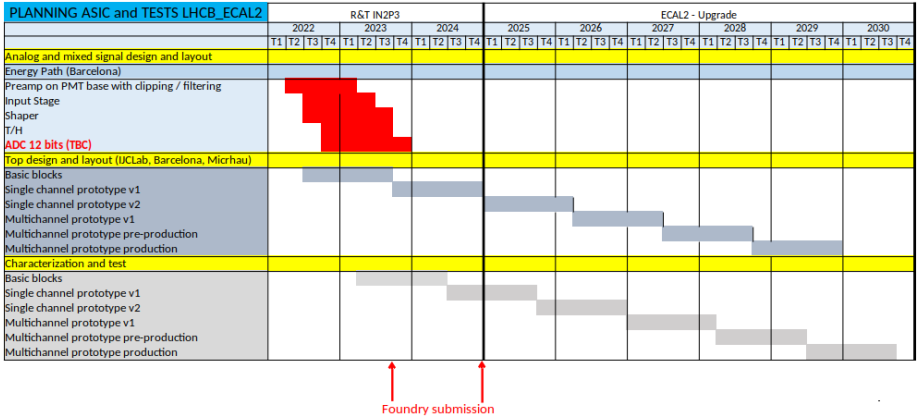
Energy Channel Testbench

- Channel testsbench using PbSPACAL+Poly average pulse shape.
- Issues solving operation point, individual testbenches in progress.



Planning

- Tight schedule to arrive to first submission by mid 2023.
- Open issues need to be solved (light yield, PMT circuit, calibration).



Thanks a lot for your attention!