



R&D

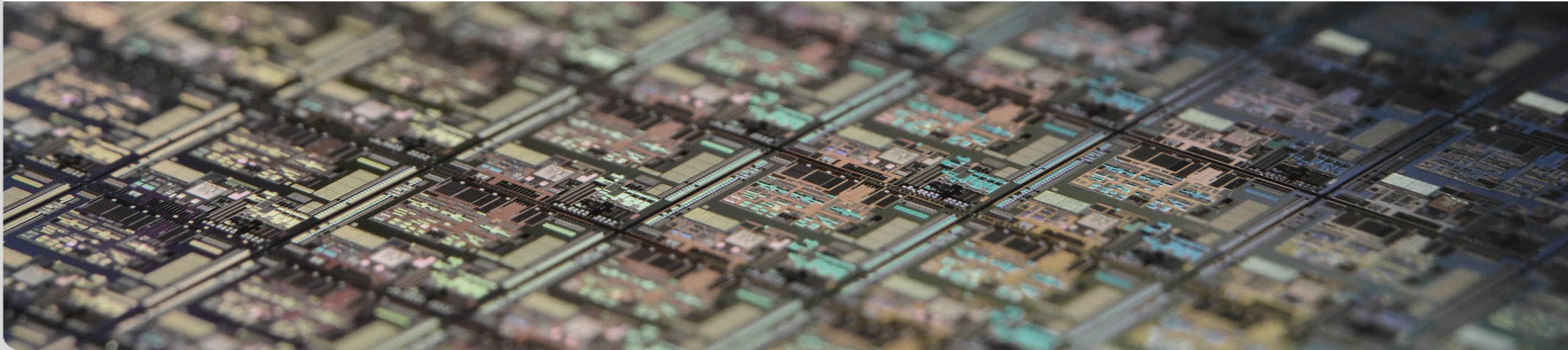


Federal Ministry  
of Education  
and Research

# Measurements of Total Ionizing Dose Effects in TPSCo 65 nm and Influence of NMOS Bulk Bias

A. Dorda, R. Ballabriga, G. Borghello, M. Campbell, W. Deng, G. H. Hong,  
I. Kremastiotis, W. Snoeys, G. Termo

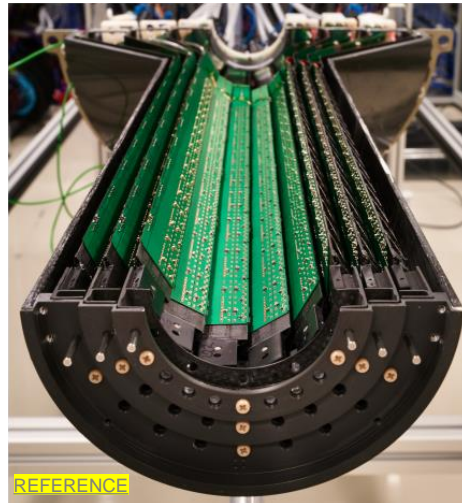
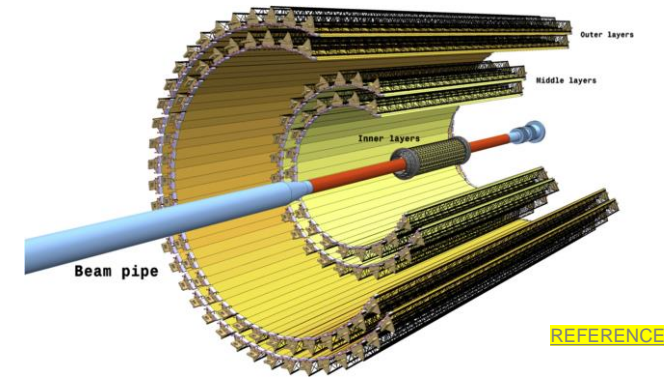
EP-ESE-EME



# Context

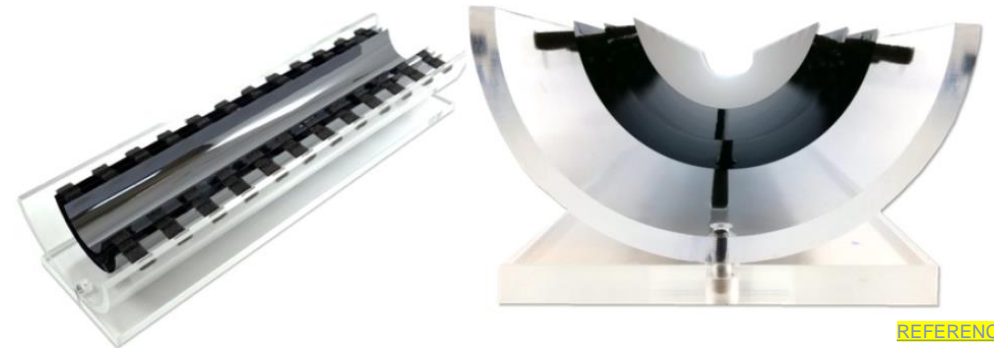
- CERN EP R&D WP1.2

- First candidate chosen **TPSCo 65 nm ISC technology**
- Develop new monolithic pixel sensors for CERN experiments (i.e. ALICE ITS3)



ALICE ITS2 UPGRADE

Inner detector with polygonal shape



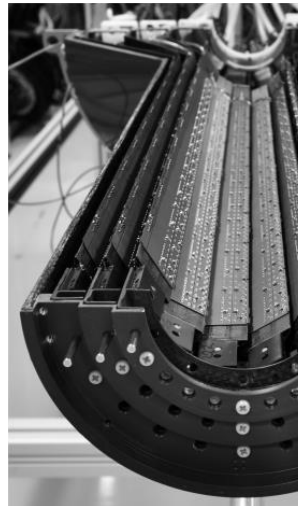
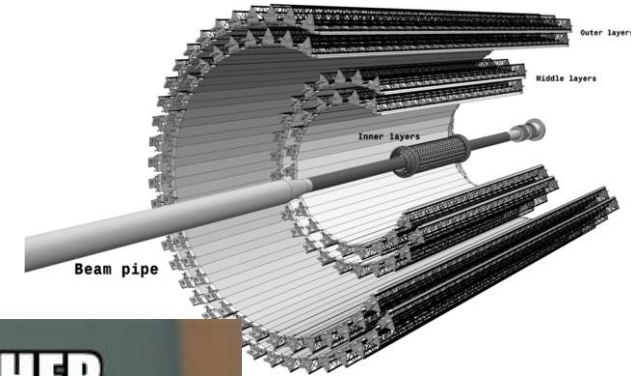
ALICE ITS3 UPGRADE \*IN PROGRESS\*

Inner detector with fully cylindrical shape

# Context

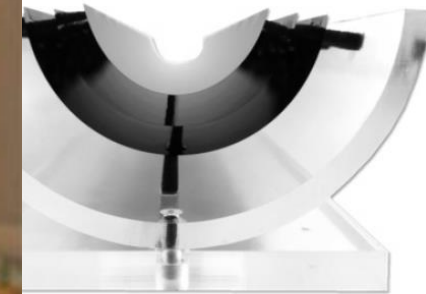
- CERN EP R&D WP1.2

- First candidate chosen **TPSCo 65 nm ISC technology**
- Develop new monolithic pixel sensors for CERN experiments (i.e. ALICE ITS3)



ALICE ITS2 UPC

Inner detector with polygonal shape

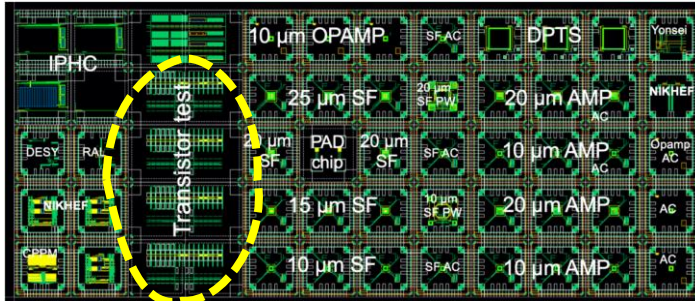


IN PROGRESS\*

Cylindrical shape

**Expected Total Ionizing Dose (TID) of 1 Grad SiO<sub>2</sub>**

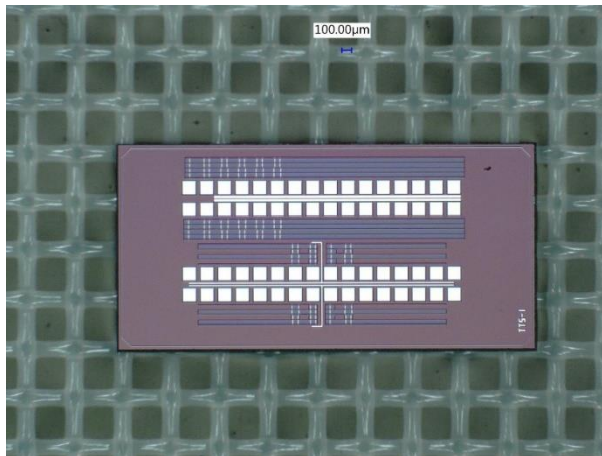
# TPSCo 65 nm transistors characterization



Layout submitted with TTS

- Objective: to offer a preliminary characterization of this technology to the designers
  - TTS (Transistor Test Structures): for process verification
  - TTS chips contain arrays with different transistor sizes from this technology

They came back from the foundry!

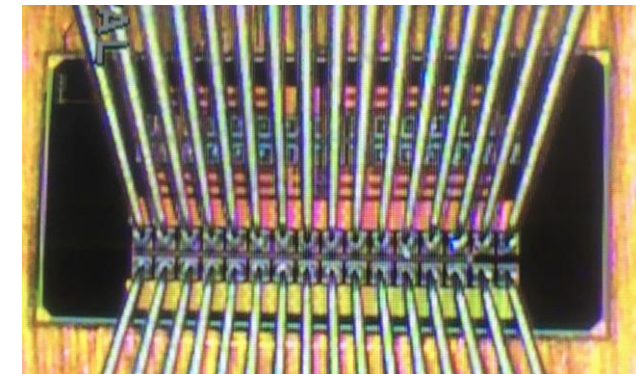


TTS1 with 1.2 V core transistors

Probing station

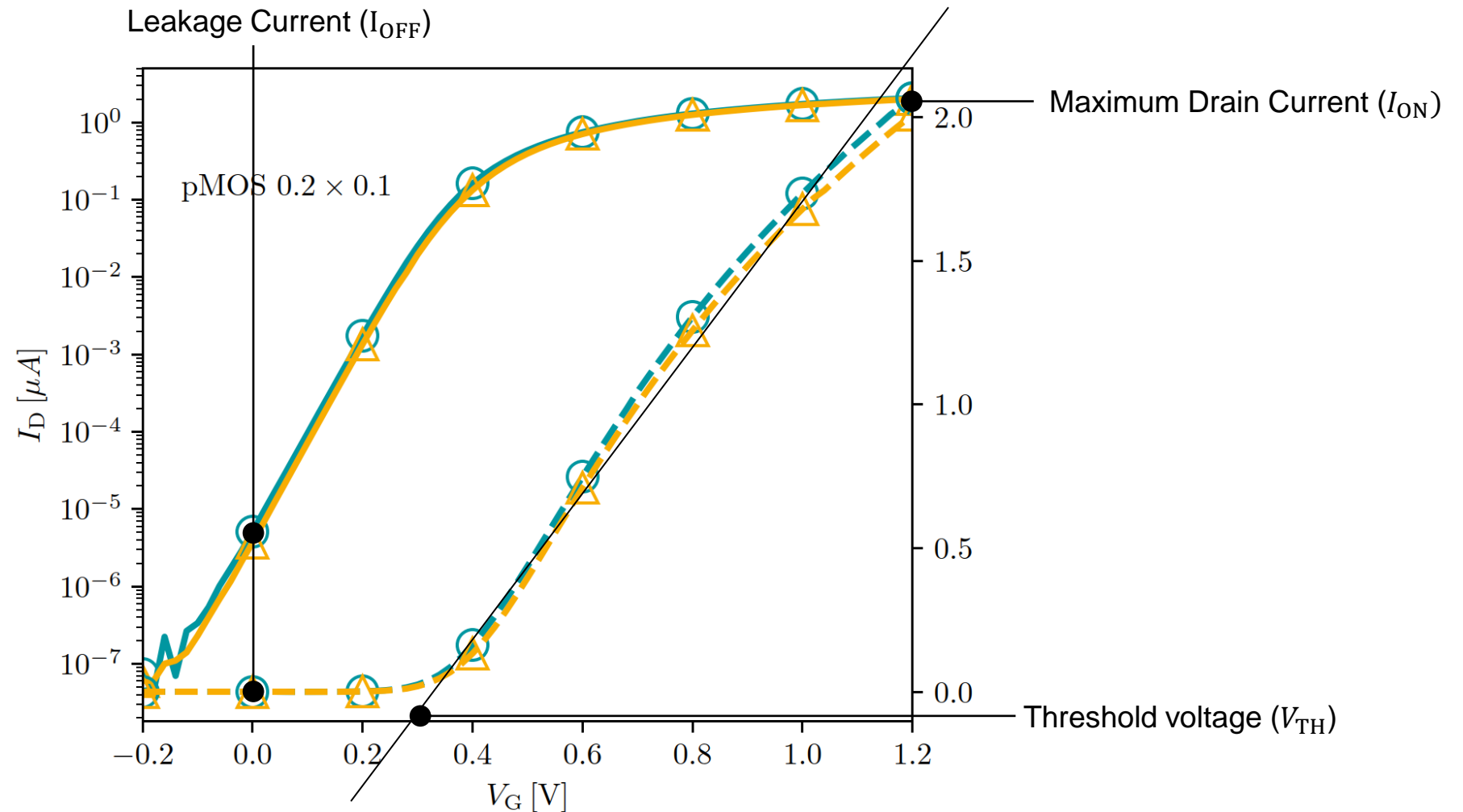


Needles connected to the TTS pads



Now we can bias gate, source, drain and bulk, and we can measure!

# The $I_D$ vs. $V_G$ measurements: Definition of $I_{ON}$ , $V_{TH}$ , $I_{OFF}$

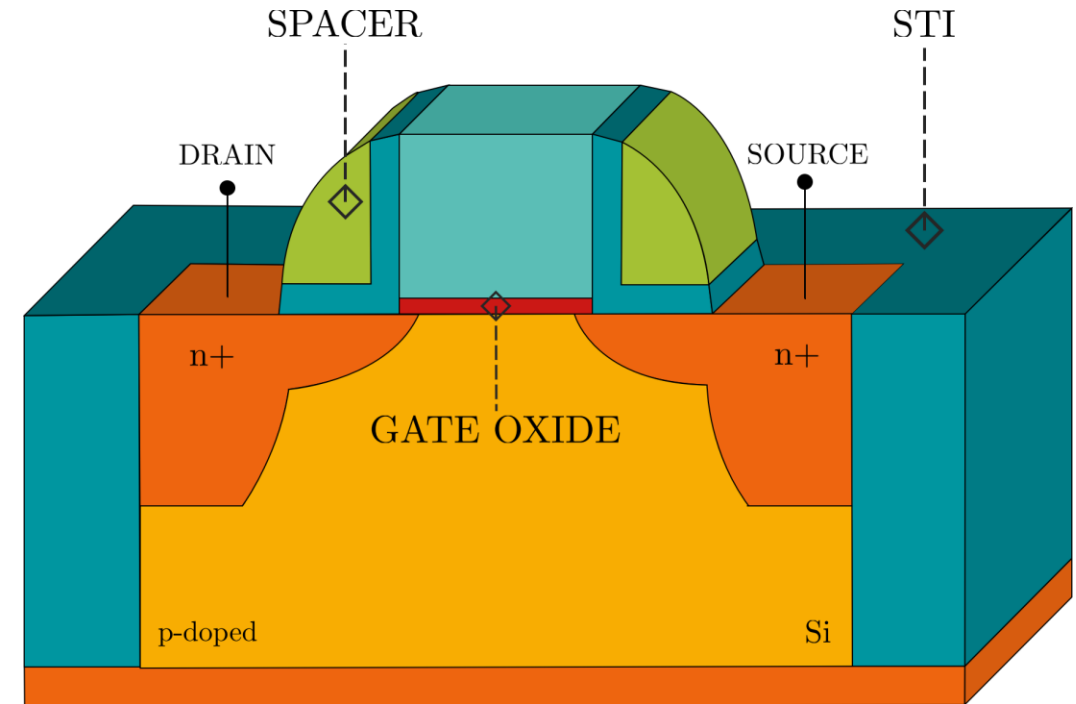


# RESULTS FROM IRRADIATION MEASUREMENTS

# Why irradiating the transistors?

Main known radiation-induced effects in modern planar CMOS technologies:

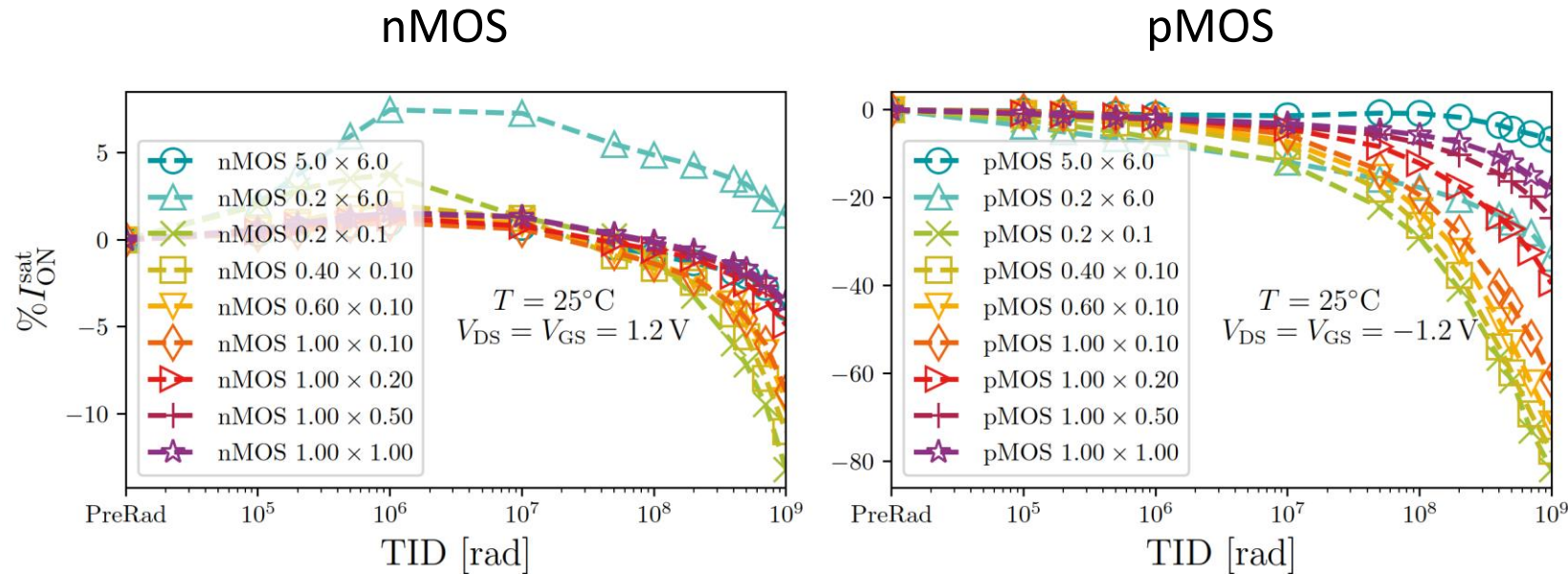
- **RISCE (Radiation-Induced Short Channel Effects):** Due to positive charges accumulating at the **spacers**
- **RINCE (Radiation-Induced Narrow Effects):** Due to positive charges accumulating at the **Shallow Trench Isolation (STI)**
- **Radiation-Induced Leakage Current:** Due to positive charges accumulating at the **STI of the nMOS** during OFF state



Expected Total Ionizing Dose (TID) of 1 Grad SiO<sub>2</sub>

We need to make sure that TPSCo 65 nm behaves like previous 65 nm technologies from other manufacturers

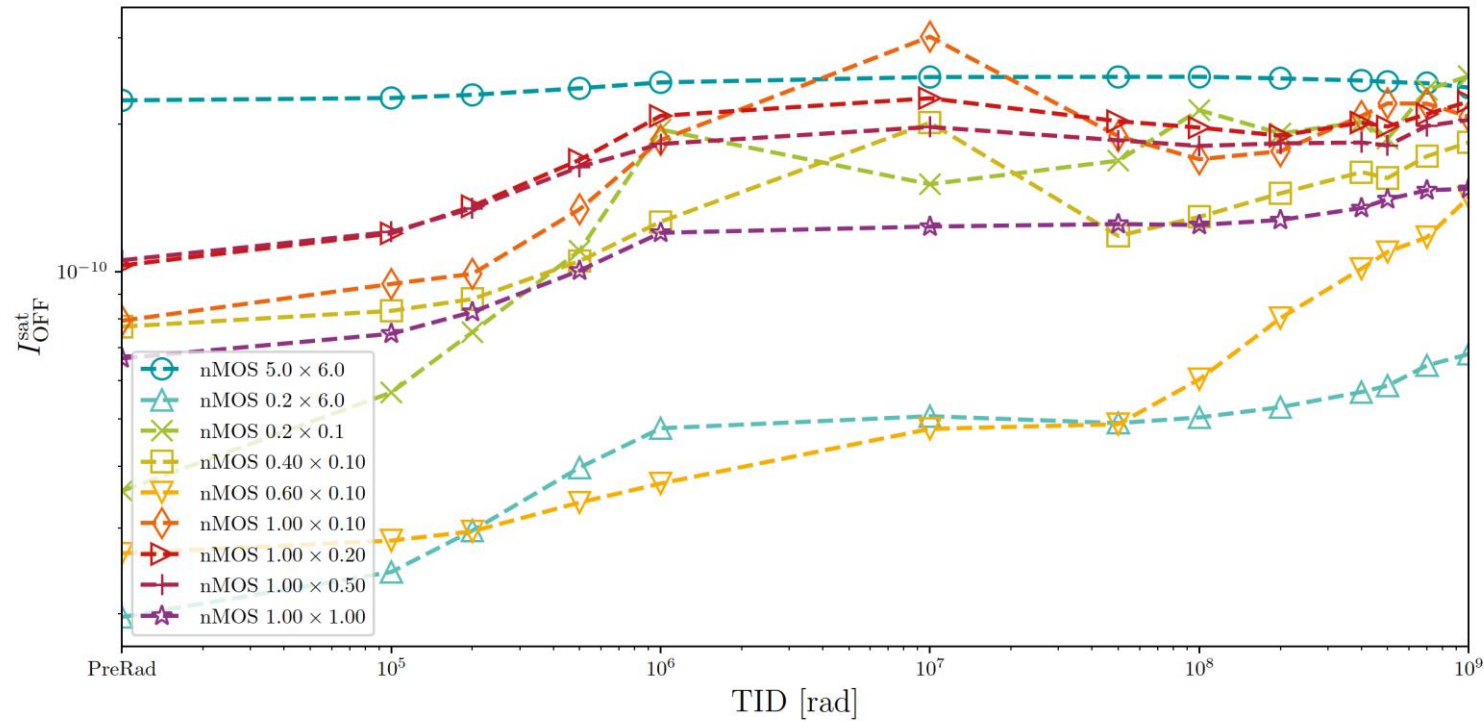
# Measurements up to 1 Grad TID ( $\text{SiO}_2$ ): $I_{\text{ON}}$ Degradation



- ✓ This degradation is comparable with other 65 nm technologies
  - Up to **80% drop of  $I_{\text{ON}}^{\text{sat}}$**  delivered by the pMOS. Channel length dependence
  - Up to **15% degradation of  $I_{\text{ON}}^{\text{sat}}$**  of the nMOS



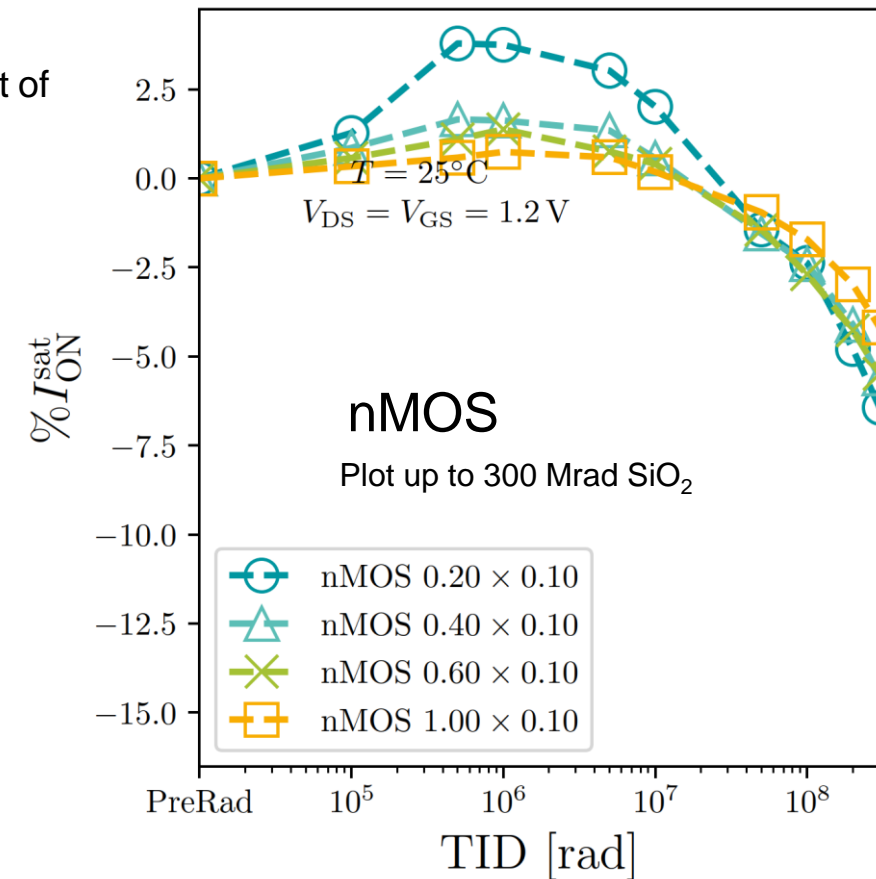
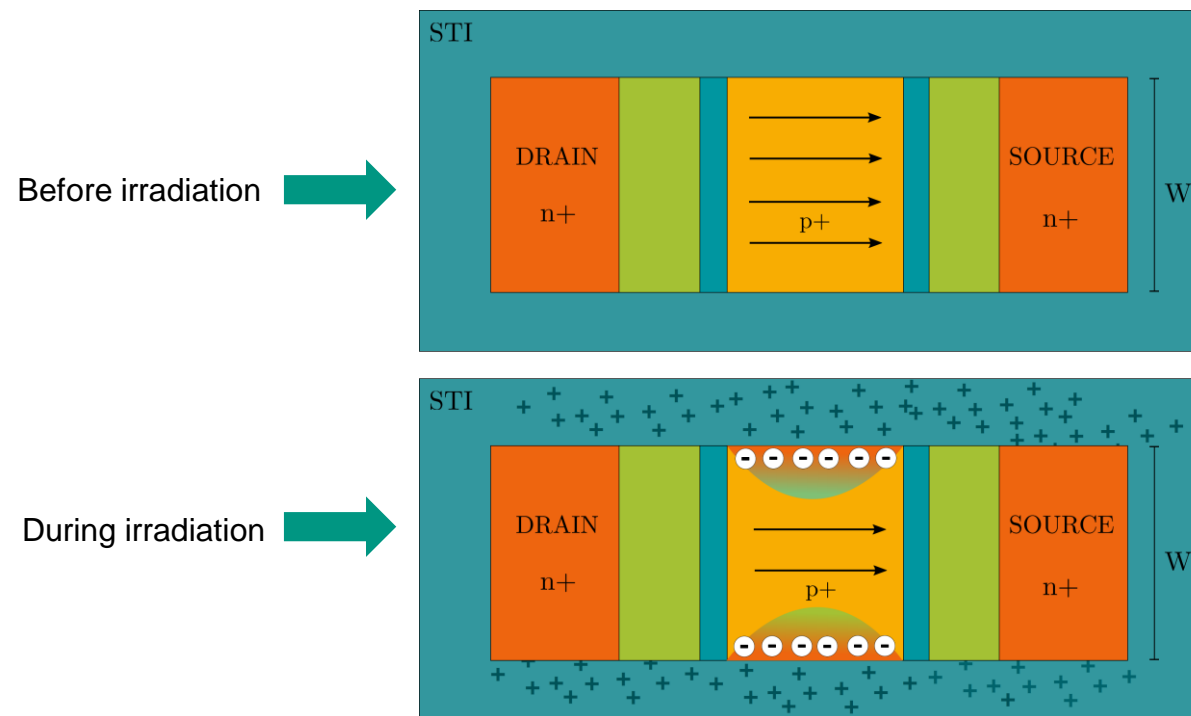
# Measurements up to 1 Grad TID (SiO<sub>2</sub>): Radiation Induced Leakage Current



✓ Robustness of this node regarding radiation-induced leakage current.  $I_{OFF}^{sat}$  increase below one order of magnitude

# Radiation-Induced Narrow Channel Effects (RINCE): nMOS

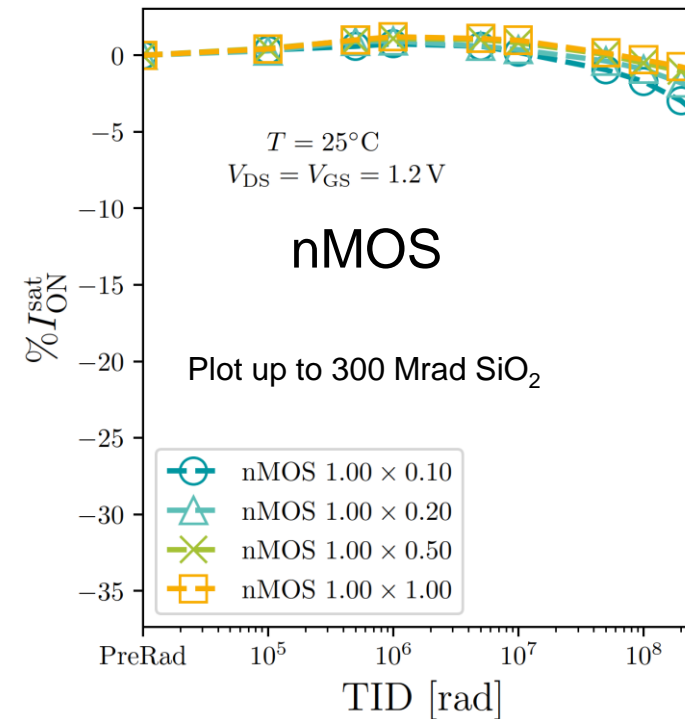
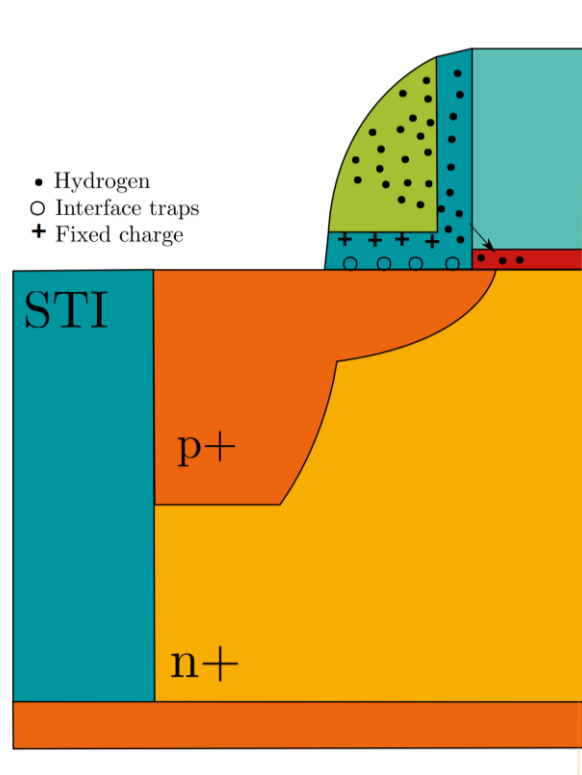
1. Beginning of irradiation: positive charges accumulate at the STI lowering  $V_{TH}$  and increasing  $I_{ON}^{sat}$ .
2. Increasing TID, negative charges accumulate at STI/Si compensating the effect of trapped holes and degrading  $I_{ON}^{sat}$ .



# Radiation-Induced Short Channel Effects (RISCE)

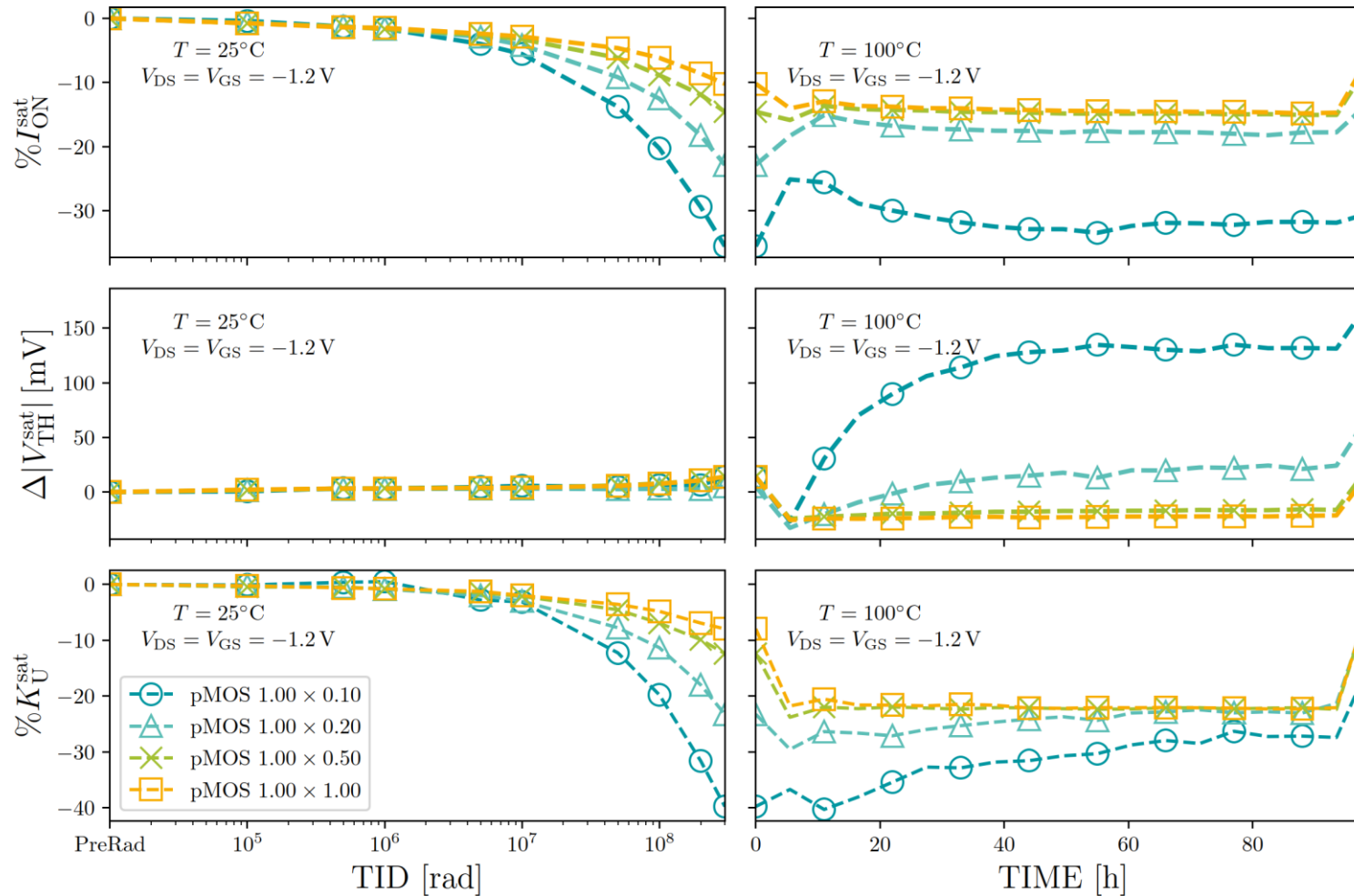
RISCE is characterized by:

1. During irradiation: increase of series resistance on the sides of the channel
2. During annealing:  $V_{TH}$  shift due to the transport of H<sup>+</sup> ion in the gate oxide



# Radiation-Induced Short Channel Effects (RISCE): pMOS

Plot up to 300 Mrad SiO<sub>2</sub>

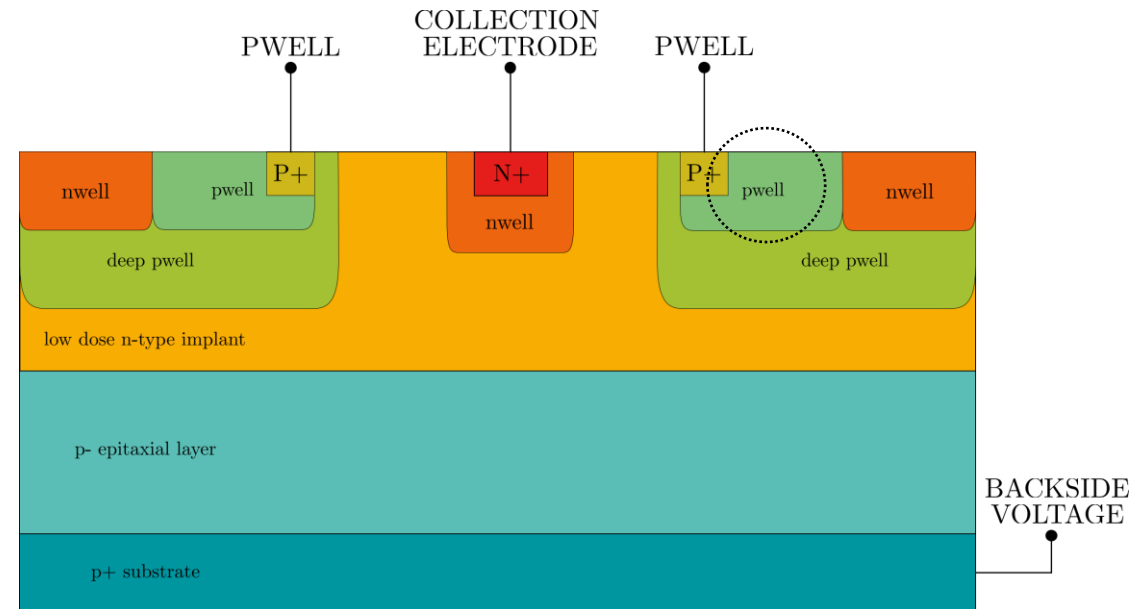


Last points after annealing at room temperature

$$K_\mu = \frac{\mu_n C_{\text{OX}} W}{2 L}$$

# RESULTS FROM NMOS BULK BIAS MEASUREMENTS

# Why nMOS Bulk Bias?



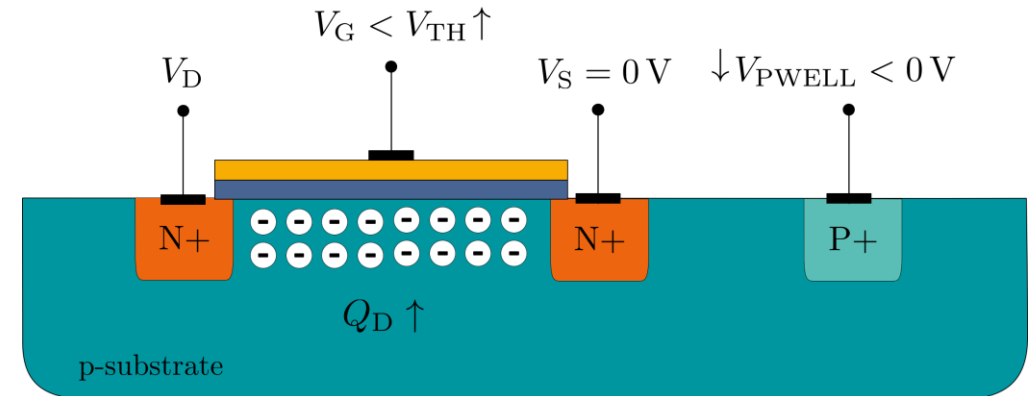
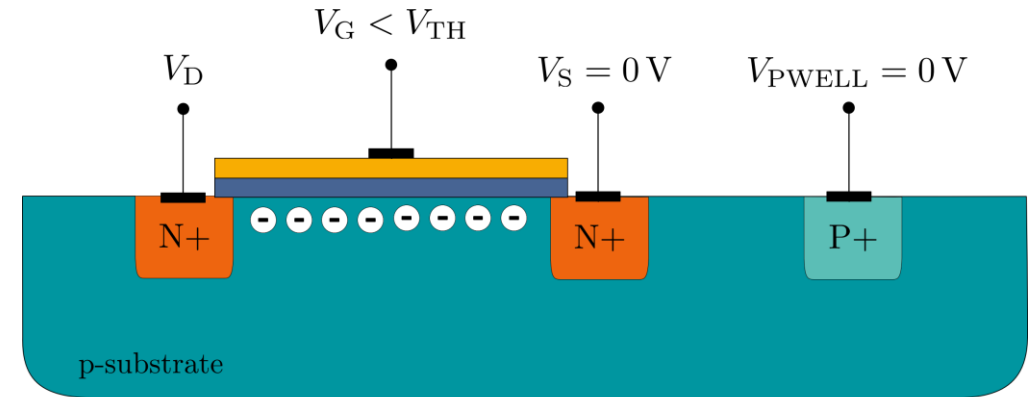
- nMOS on the pixel matrix have their bulk (PWELL) and substrate (BACKSIDE VOLTAGE) biased down to -6 V
- This allows to enhance the depletion and the detection but **there is a side consequence** → **BODY EFFECT**
- This study aims to analyse the behaviour of nMOS transistors at an unusual operating point at which the models provided by the foundry are not longer valid.

# The Body Effect

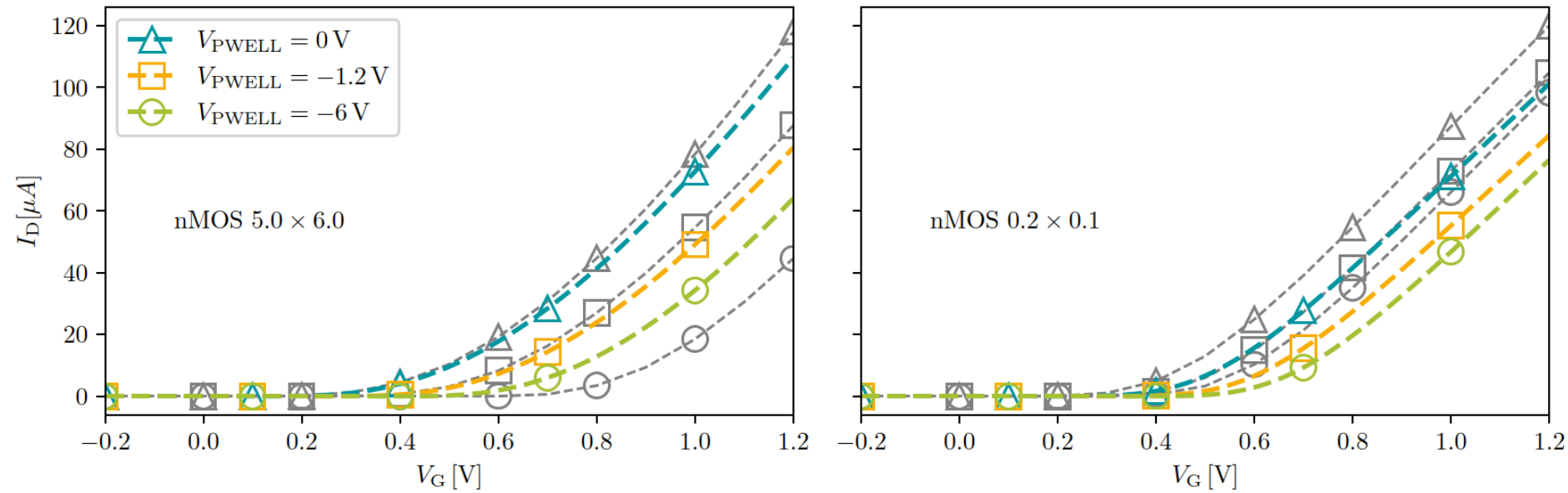
- As  $V_{PWELL} < 0 V$ , the depletion region becomes wider  $\rightarrow$  charge at the depletion region ( $Q_d$ ) increases
- The charge at the gate must mirror  $Q_d$  to create inversion layer
- $V_{TH}$  increases following  $Q_d$ :

$$V_{TH} = V_{TH0} + \gamma \left( \sqrt{2 \phi_F + V_{SPWELL}} - \sqrt{|2 \phi_F|} \right)$$

- $V_G$  increases to create inversion layer



# Measurements at Different Biases and Comparison with Simulation



1. Measurements of nMOS transistors with  $V_{PWELL} = -6\text{ V}$  show an **increase of the nominal  $V_{TH}$  of  $\sim 260\text{ mV}$**  together with a  **$\sim 40\%$  drop of  $I_{ON}^{sat}$**
2.  $V_{TH}$  shift is **overestimated for maximum size devices** and **underestimated for minimum size devices**
3. In both cases **not accurate at large reverse biases**



## Conclusion

- ✓ Irradiation response like other 65 nm technologies from other manufacturers
  - Up to 1 Grad (SiO<sub>2</sub>): max. ~15%  $I_{ON}^{sat}$  drop for nMOS and max. ~80%  $I_{ON}^{sat}$  drop for pMOS
  - Up to 300 Mrad (SiO<sub>2</sub>) and subsequent 100°C annealing: presence of RISCE and RINCE.  $V_{TH}$  shift of 200 mV and  $K_U^{sat}$  recovery after annealing at 25°C
  - Radiation Induced Leakage Current increase less than one order of magnitude
- !! Large negative bulk biases induce an important body effect
  - Simulation with TYP corner not accurate at large reverse biases (error w.r.t. the simulation reaches ~160 mV)
  - Measurements of nMOS transistors with  $V_{PWELL} = -6$  V show an increase of the nominal  $V_{TH}$  of ~260 mV

**THANK YOU!**

# Bibliography



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## Definition of $\%I_{ON}$ , $V_{TH}$ , $I_{OFF}$ , $K_{\mu}$

Variation of Maximum Drain Current ( $\%I_{ON}$ ) —●  $\%I_{ON}(TID) = 100 \frac{I_{ON}(TID) - I_{ON}(TID = 0 \text{ rad})}{I_{ON}(TID = 0 \text{ rad})}$

Threshold voltage ( $V_{TH}$ ) —● Defined as necessary  $V_{GS}$  to create conducting channel between drain and source. Extracted from IDVG measurements using linear extrapolation method

Leakage Current ( $I_{OFF}$ ) —● Defined as the measured  $I_D$  current when  $V_G = 0 \text{ V}$  (transistor OFF) and  $V_{DS} > 0$

Transconductance ( $K_{\mu}$ ) *in saturation* —● 
$$K_{\mu} = \frac{\mu_n C_{OX} W}{2 L}$$
 Extracted from IDVG measurements as the derivative of  $\sqrt{I_D^{sat}}$