Task 7.2.2 - Shower development in SDHCAL

Mary-Cruz Fouz

CIEMAT

UE participants

Belgium: Ghent

France: CNRS-IP2I, CNRS-LPC, CNRS-OMEGA

Spain: CIEMAT

Non-UE participants

China: SJTU - Shanghai Jiao Tong University

South Korea: GWNU - Gangneung–Wonju National University

& SNUBH- Seoul National University Bundang Hospital

Introduction – The SDHCAL concept

SDHCAL - **S**emi-**D**igital **H**adronic **CAL**orimeter

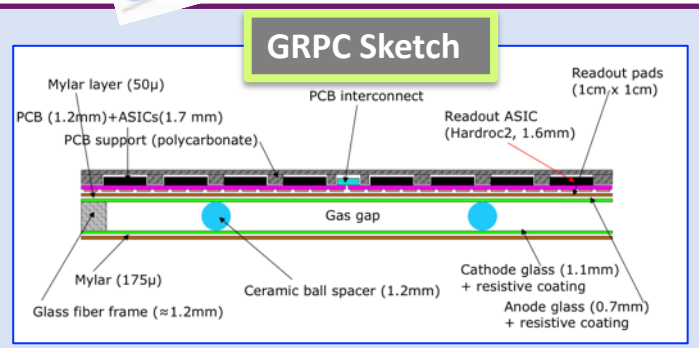
A sampling hadronic calorimeter under development at CALICE Collaboration intended to be used with PFA reconstruction techniques. (➔ High Granularity is a must)
One of the proposed options for the *ILD (International Large Detector) at the ILC (International Linear Collider)* and for and *CEPC (Circular Electron Positron Collider)* detectors

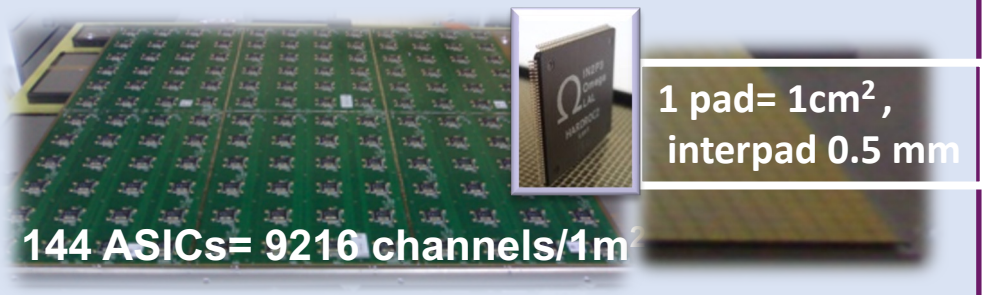
Sampling calorimeter: ***Absorber: Stainless Steel + Detector: Glass Resistive plate Chambers***

Detector: **GRPC (Glass Resistive Plate Chambers)** operating in **avalanche mode**

1x1 cm^2 pads. Semi-Digital Readout, 2bits **- 3 thresholds**
➔ It counts **how many** and **which pads** have a **signal larger than one of the 3 thresholds**

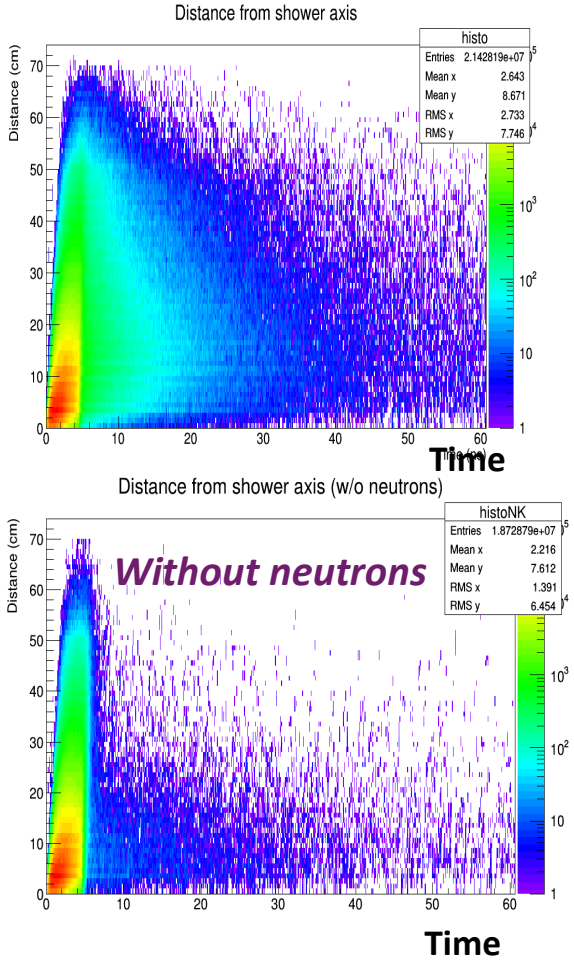
Embedded electronics:
PCB separated from the GRPC by a mylar layer (50µm).
➔ Bottom: **1x1cm2 pads**
➔ Top: **HARDROC** (**HA**dronic **R**pc **R**ead**O**ut **C**hip) & related connections
Power-pulsed electronics: In **stand-by during dead time** in between ILC Collisions or spills in beam tests



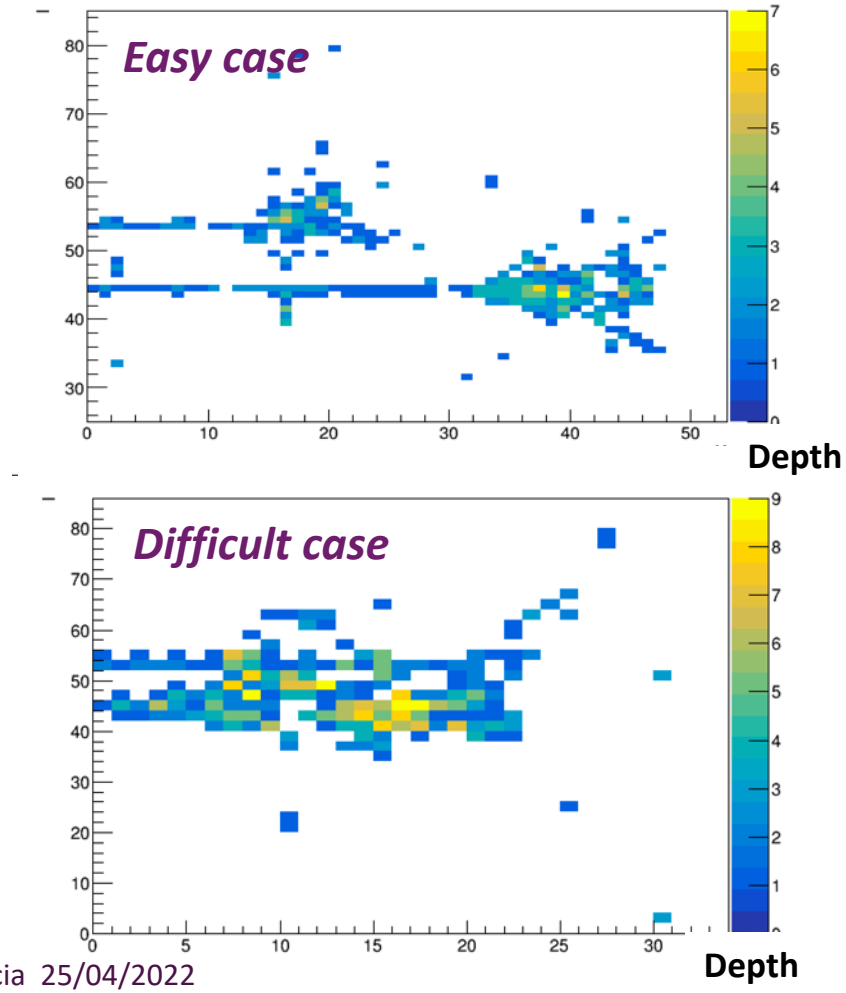


Motivation of including timing readout

Timing could be an important factor to identify delayed neutrons and better reconstruct their energy



Time information can help to separate close by showers and reduce the confusion for a better PFA application.
Example: pi-(20 GeV), K-(10 GeV) separated by 8 cm.



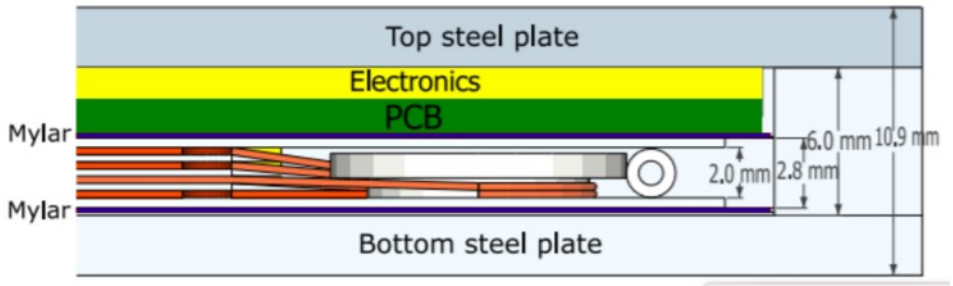
SDHCAL at AIDAInnova – Task 7.2.2

General goal: Extending the Semi-Digital Hadronic CALorimeter (SDHCAL) to include timing information (100 - 200ps resolution) for a **5D-calorimetry (space, amplitude & timing)**

Implementation: **Build small multi-gap RPC (MRPC)** equipped with a **new version of electronics** with **timing capabilities** to prove the final performance

The use of MRPC will improve the intrinsic timing of the detector but **electronic on the previous SDHCAL 1m3 prototype** has not high resolution timing capabilities.

➔ Readout Chip **HARDROC3**. Time Stamping=**200ns**



Electronics for SDHCAL

Baseline ASIC

Petiroc2A/B

It is not the ASIC for the long term,
only for exploring the capabilities.
Some limitations as: difficult to chain,
limited digital logic, deadtime

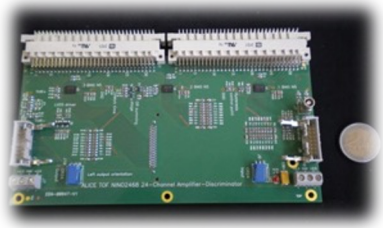
- 32 channels
- on-chip TDC
- Time resolution below 40ps

Developed at CNRS-OMEGA
partially thanks to AIDA2020
for CMS-muon upgrade

Other ASICS being or to be used

NINO

ASIC designed for the ALICE MRPC (TOF array)
- 8 channels
- Time resoltion ~50 ps



LiROC+picoTDC

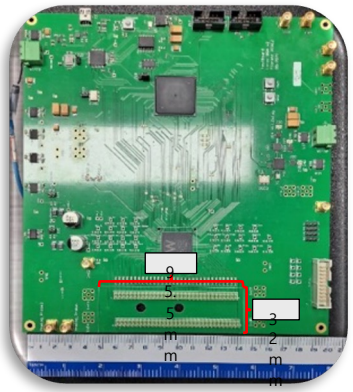
weeroc

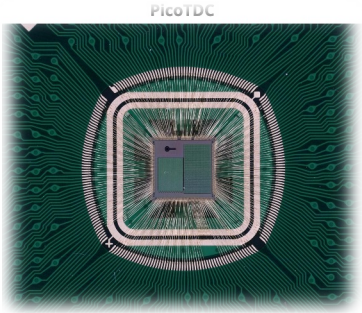
Board is under development by the WEEROC company

Based on LiROC + picoTDC

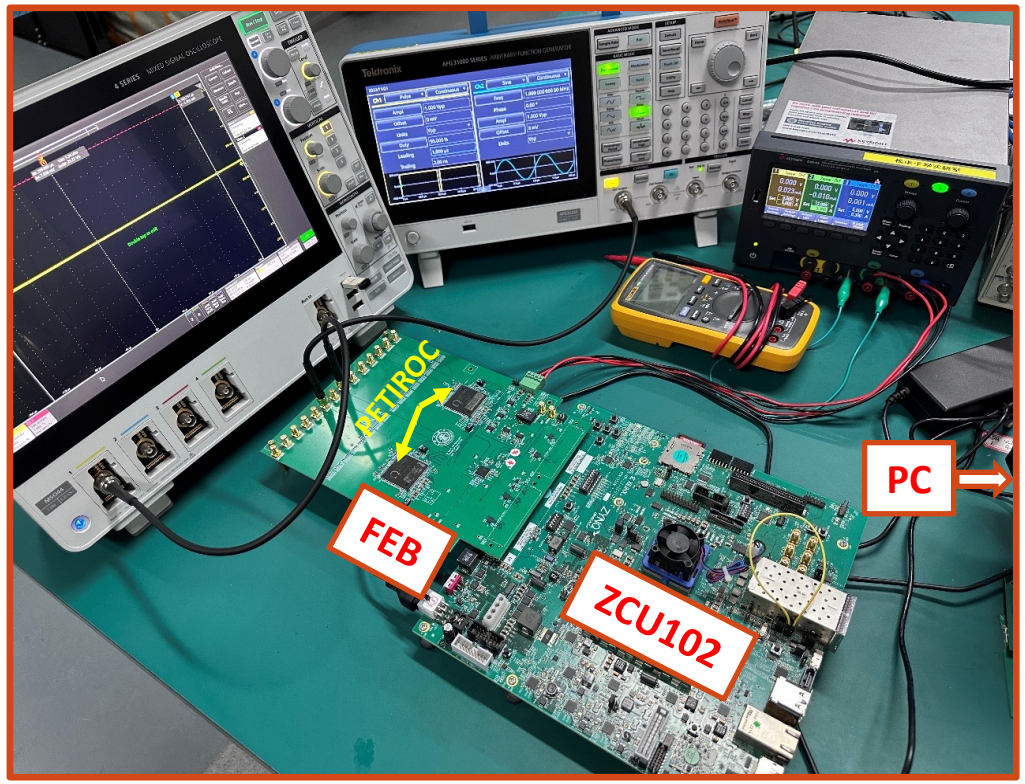
64-channel ASIC

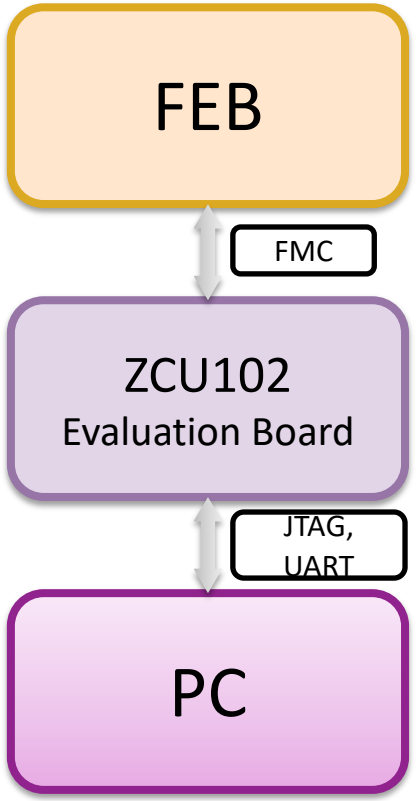
64 channel TDC ASIC
Time resolution <12 ps





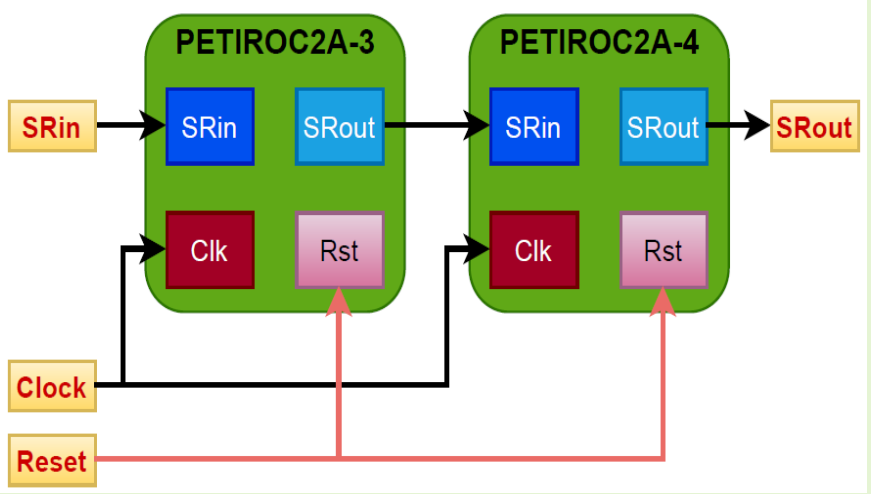
Some tests on PETIROC - Setup





Configuration of Petiroc2

Two chips can be configured through daisy chain.



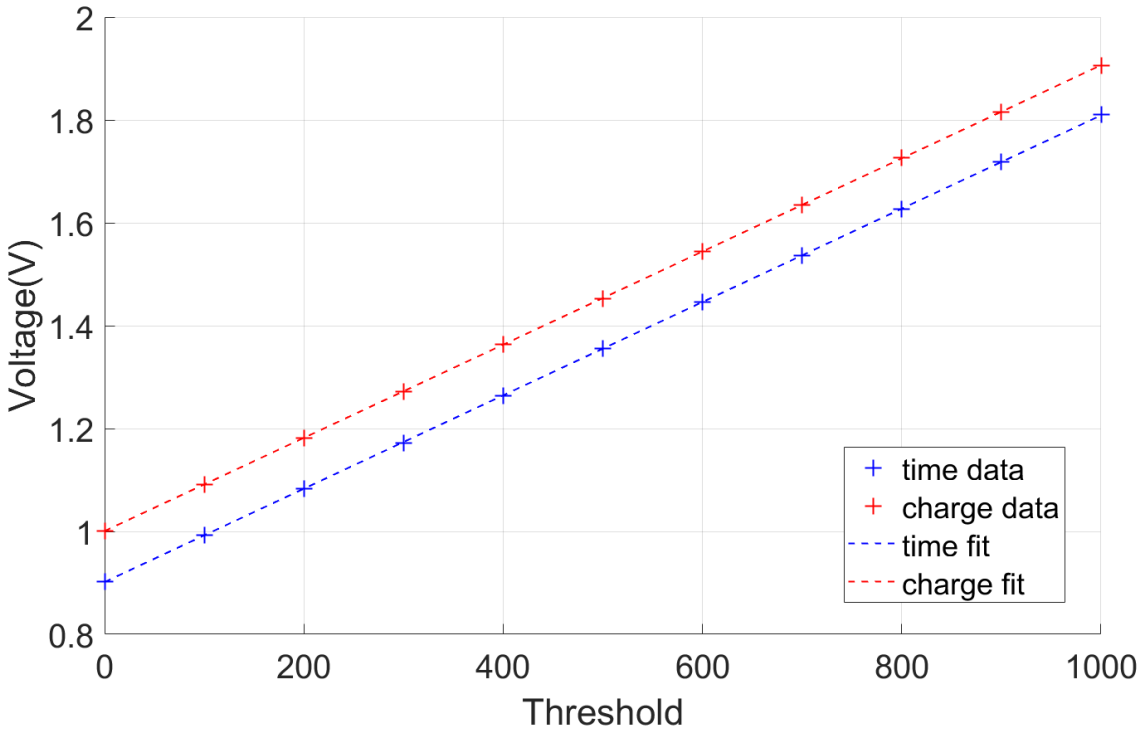
Validation

Reference Voltages checks
Threshold tests

Next: Use Ethernet to replace UART protocol to realize high speed data transfer from FEB to PC

Petiroc2B threshold tests

- Set different time and charge thresholds through 10-bit DAC configuration
- Use a voltage meter to measure the analog output of thresholds
- Linear regression and compare with the datasheet



Test Results of ours:

$$V_{time} = 0.0009 * threshold + 0.9016$$
$$V_{charge} = 0.0009 * threshold + 1.0008$$

Test Results from datasheet v2.5a:

$$V_{time} = 0.0009 * threshold + 0.8941$$
$$V_{charge} = 0.0009 * threshold + 1.0131$$

✓ The analog output of time and charge thresholds matched input DAC.
✓ The configuration of Petiroc2B is valid.

Single injection tests

- To test if the new version of FEB has clean signals without crosstalk, we first did some single injection tests:
  1. Inject the signal to one of the 32 channels of one of the Petiroc2B chips.
  2. readout the 960-bit data.
  3. check 'if_hit' data to see if any hits are recorded except for the injected channel.
- All the masks are disabled during the tests.

✓ No crosstalk in the FEB

inject channel

if_hit data

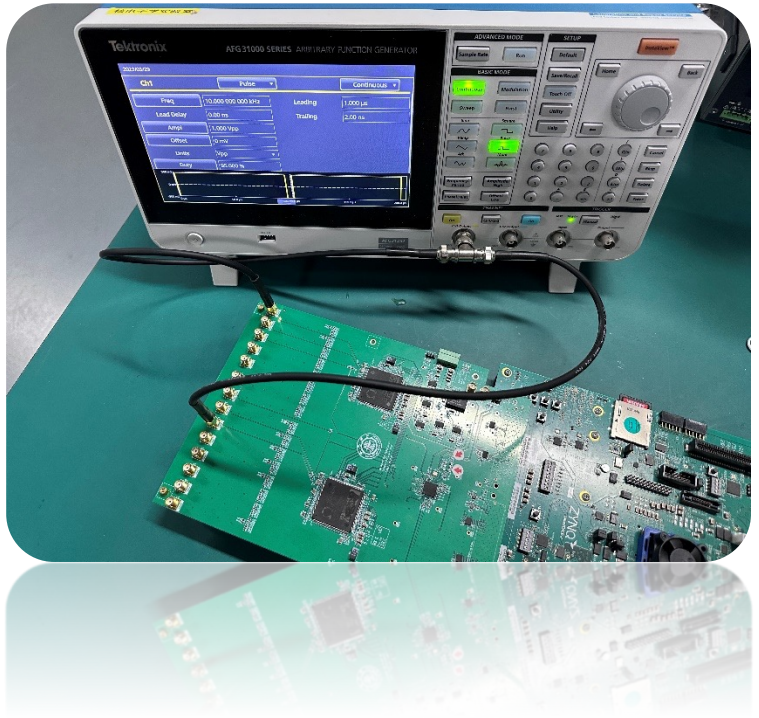
chip1	chn0	chn4	chn8	chn12	chn16	chn29	chip2	chn0	chn4
chn0	1	0	0	0	0	0	chn0	1	0
chn1	0	0	0	0	0	0	chn1	0	0
chn2	0	0	0	0	0	0	chn2	0	0
chn3	0	0	0	0	0	0	chn3	0	0
chn4	0	1	0	0	0	0	chn4	0	1
chn5	0	0	0	0	0	0	chn5	0	0
chn6	0	0	0	0	0	0	chn6	0	0
chn7	0	0	0	0	0	0	chn7	0	0
chn8	0	0	1	0	0	0	chn8	0	0
chn9	0	0	0	0	0	0	chn9	0	0
chn10	0	0	0	0	0	0	chn10	0	0
chn11	0	0	0	0	0	0	chn11	0	0
chn12	0	0	0	1	0	0	chn12	0	0
chn13	0	0	0	0	0	0	chn13	0	0
chn14	0	0	0	0	0	0	chn14	0	0
chn15	0	0	0	0	0	0	chn15	0	0
chn16	0	0	0	0	1	0	chn16	0	0
chn17	0	0	0	0	0	0	chn17	0	0
chn18	0	0	0	0	0	0	chn18	0	0
chn19	0	0	0	0	0	0	chn19	0	0
chn20	0	0	0	0	0	0	chn20	0	0
chn21	0	0	0	0	0	0	chn21	0	0
chn22	0	0	0	0	0	0	chn22	0	0
chn23	0	0	0	0	0	0	chn23	0	0
chn24	0	0	0	0	0	0	chn24	0	0
chn25	0	0	0	0	0	0	chn25	0	0
chn26	0	0	0	0	0	0	chn26	0	0
chn27	0	0	0	0	0	0	chn27	0	0
chn28	0	0	0	0	0	0	chn28	0	0
chn29	0	0	0	0	0	1	chn29	0	0
chn30	0	0	0	0	0	0	chn30	0	0
chn31	0	0	0	0	0	0	chn31	0	0

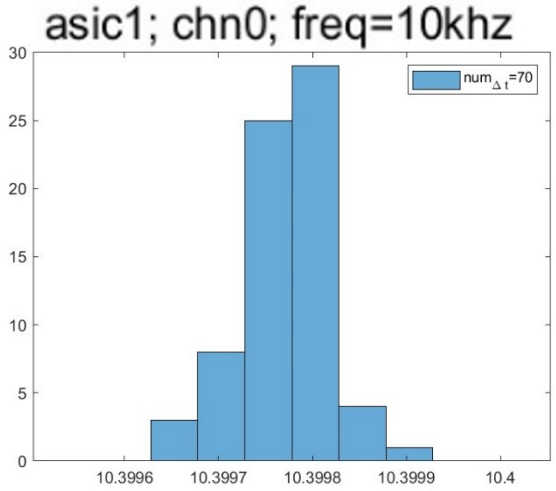
Two chips timing

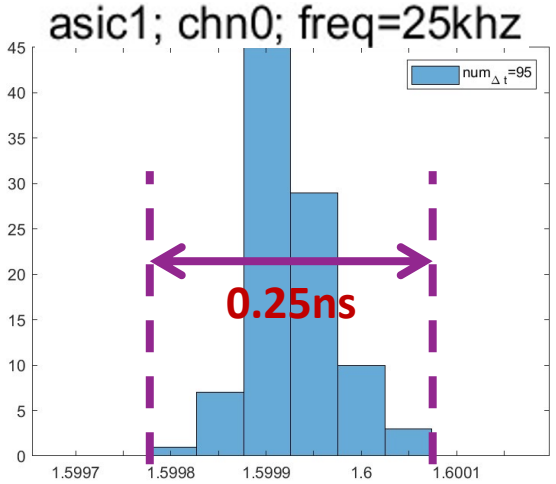
Same signal injected into two chips (with a double-pass).

Δt_{12} : Δt between two Petiroc2B chips of each hit.

$\overline{\Delta t_{12}}(\mu s)$	$\mathrm{std}(\Delta t_1)(ps)$	$\mathrm{std}(\Delta t_2)(ps)$	$\mathrm{std}(\Delta t_{12})(ps)$	$f_{sig}(kHz)$
5.8000	41.0912	49.5356	73.5276	25
5.7999	48.6895	51.9453	78.4336	10







MRPC chambers under development

Small chambers

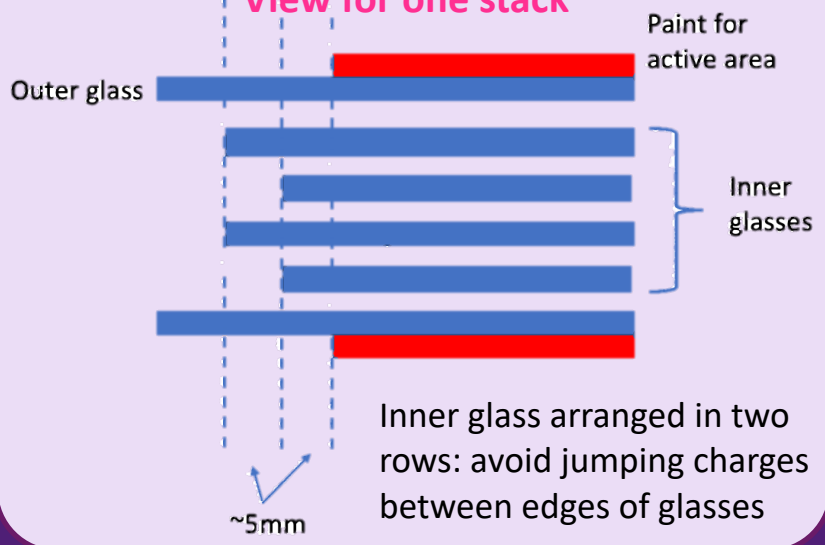
Low resistivity glass for high rates

Glass resistivity ~ 10^{10} Ωcm

Glass thickness : 500 µm

2 stack 5 gaps

View for one stack



Inner glass arranged in two rows: avoid jumping charges between edges of glasses

Fast timing MRPC

Glass resistivity ~ **5x10^{12} Ωcm**

Glass thickness : 330 µm

Single stack 5 gaps

X-Y strip type MRPC

Strip: **5mm pitch(4mm width)**

Ceramic Fishing lines: Ø **230 µm**

Expecting less charge going to the fishing line

Large chambers

Glass resistivity ~ 10^{12} - 10^{13} Ωcm

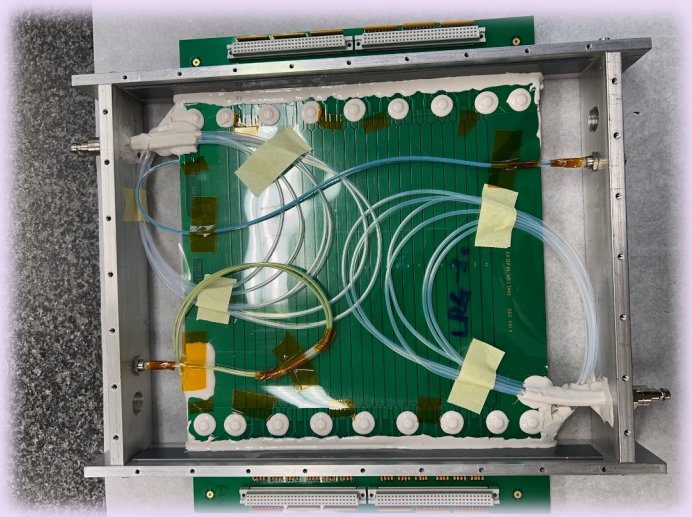
1x1m2 chambers

two times 4-gap PCB inserted between the two

Using spacers

1cm Strip width

Chamber + Electronic tests
“Low resistivity” glass



Sealed gas gap
Teflon tubes to make uniform gas flow

Electronics

- **NINO** chip for signal treatment
- **V1290A TDC** for digitization
  Caen 32/16 Channel Multihit TDC, 25ps LSB

Beam test at CERN
April (ongoing) and August

Fast timing MRPC

Active area: 20 x 20 cm^2

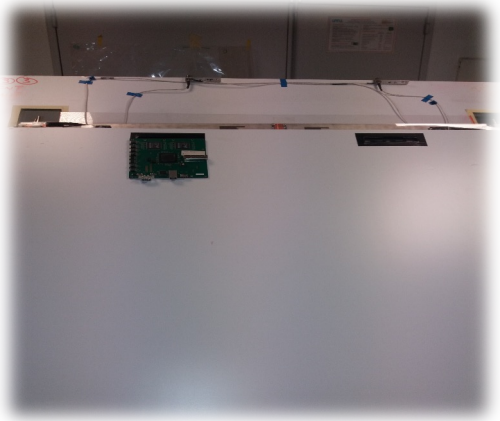
Electronics

LiROC + picoTDC not ready

Use **NINO card + HPTDC** (25ps)

For adaptation from single to differential signals, an interface card has been designed and manufactured for NINO, recently.

Chamber + Electronic tests
“Standard” glass 1x1m2 chamber



Readout by: PETIROC+ external TDC
Same cards as the ones developed for upgraded CMS RPC
2 PETIROC2 + FPGA Cyclone V + ethernet

At the moment 64 strips in total can be read out but can be extended on future if needed.

Some tests to be done in incoming weeks

Tentative timeline

Year 2:

PCB & FE design

acquisition boards & software design

Year 3:

Tests of the FE Electronics and acquisition boards

Year 4:

completed modules in test beam

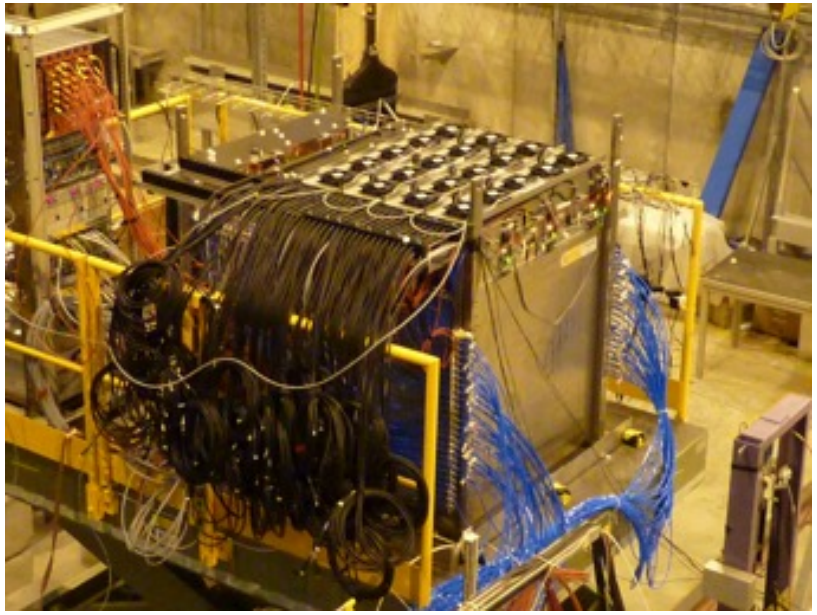
(inside SDHCAL prototype)

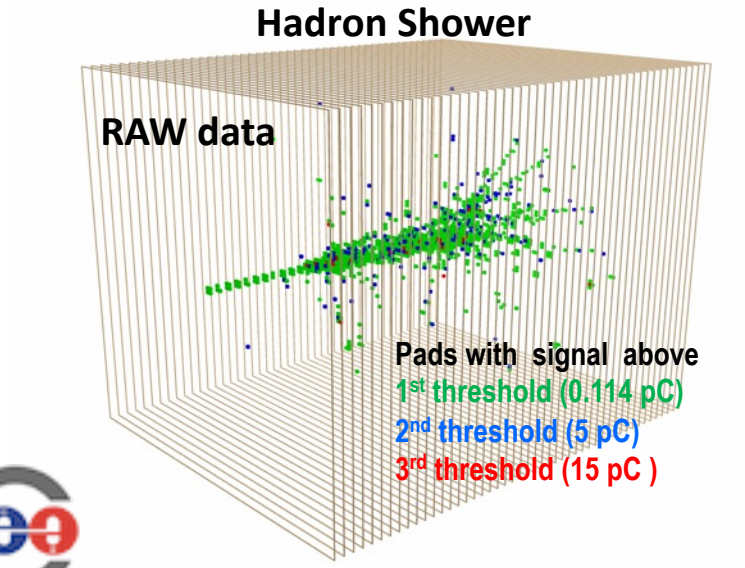
THANK YOU
FOR YOUR
ATTENTION

Introduction – The SDHCAL 1m3 SDHCAL Prototype

SDHCAL ~1.3m^3 prototype
At Test Beam @ CERN

~ half million channels!!
(More than in the full calorimeter systems of the LHC experiments)





Excellent detailed view of shower development