



Task 7.4.1

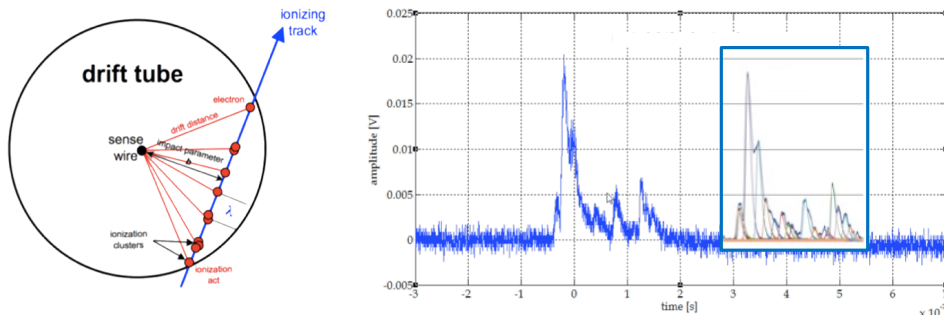
A 4-channel electronic board for Cluster Counting

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Cluster Counting pills



Determine, in the signal, the ordered sequence of the electrons arrival

$$\text{times: } \{t_j^{el}\} \quad j = 1, n_{el}$$

Based on the dependence of the average time separation between consecutive clusters and on the time spread due to diffusion, as a function of the drift time, define the probability function, that the j^{th}

$$\text{electron belongs to the } i^{th} \text{ cluster: } P(j, i) \quad j = 1, n_{el}, \quad i = 1, n_{cl}$$

from this derive the most probable time ordered sequence of the

$$\text{original ionization clusters: } \{t_i^{cl}\} \quad i = 1, n_{cl}$$

Single out, in every recorded detector signal, the isolated structures related to the arrival on the anode wire of the electrons belonging to a single ionization act.

$$\frac{\sigma_{dE/dx}}{(dE/dx)} = 0.41 \cdot n^{-0.43} \cdot (L_{track} [m] \cdot P[atm])^{-0.32}$$

from Walenta parameterization (1980)

dE/dx

for the
IDEA
Drift
Chamber

truncated mean cut (70-80%)
 $n = 112$ and a 2m track at 1 atm give

$$\sigma \approx 4.3\%$$

versus

$$\frac{\sigma_{dN_{cl}/dx}}{(dN_{cl}/dx)} = (\delta_{cl} \cdot L_{track})^{-1/2}$$

from Poisson distribution

dN_{cl}/dx

$\delta_{cl} = 12.5/cm$ for He/iC₄H₁₀=90/10
and a 2m track give

$$\sigma \approx 2.0\%$$

For any given first cluster (FC) drift time, the cluster timing technique exploits the time distribution of all successive clusters to determine, by using statistical (MPS) or ML techniques, hit by hit, the most probable impact parameter, thus reducing the bias and improving the average spatial resolution with respect to that obtainable with the FC method alone:

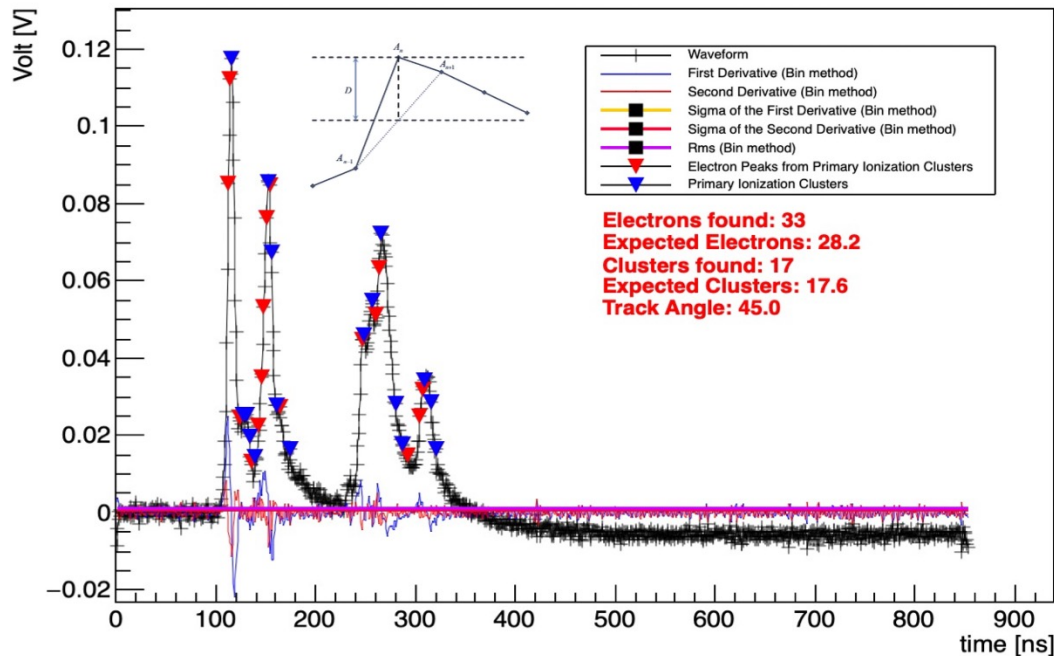
over a 1 cm drift cell, spatial resolution may improve by $\geq 20\%$
down to $\lesssim 80 \mu m$.

Fringe benefits of the cluster timing technique are:

- event time stamping (at the level of ≈ 1 ns);
- improvements on charge division;
- Improvements on left-right time difference.

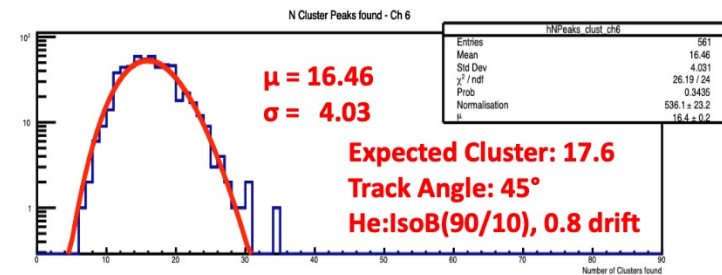
Example: finding electron peaks in beam test data

Reconstruction Primary Ionization Clusters (CLUSTER Algorithm)



Sense Wire Diameter 10 μm – Cell Size 1.0 cm – Track Angle 45° –
 1.2 GSa/s – Gas Mixture He: IsoB 90/10 – 165 GeV

Number of Cluster Distribution



Expected number of cluster[*] = δ cluster/cm (MIP) x drift tube size [cm] x 1.3 (relativistic rise) x $1/\cos(\alpha)$

- α is the angle of the muon track w.r.t. drift tube direction
- δ cluster/cm (mip) changes from 12, 15, 18 respectively for He: IsoB 90/10, 85/15 and 80/20 gas mixtures
- Actual drift tube size are 0.8, 1.2, and 1.8 respectively for 1 cm, 1.5 cm, and 2 cm cell size tubes

Cluster Counting/Timing (CC/T) strategy

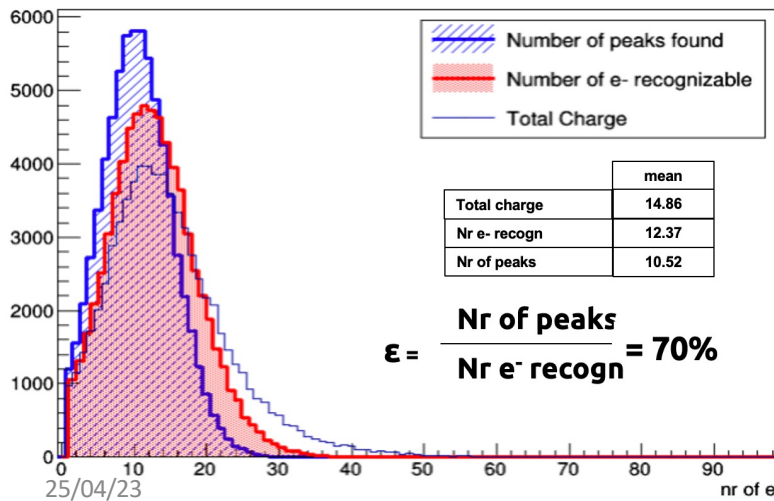
- The objective of the project is to be able to implement, on a single FPGA, CC/T algorithms (with high peak finding efficiency) for the parallel preprocessing of as many channels as possible (4, at this stage) to **reduce cost and complexity** of the system and to gain **flexibility in determining the proximity correlations** between hit cells for **track segment finding** and for **triggering purposes**. Furthermore, applying the CC/T technique in real time has the additional advantage of **reducing the amount of data transfer and of data storage** (the data generated by the digitization at high speed of drift chamber signals can reach transfer rates up to a few TB/s).
- An effective approach to data reduction consists in transferring, in real time and for each hit drift cell, only the minimal information relevant to the application of the cluster counting/timing techniques: **the amplitude and the arrival time of each peak associated with each individual ionization electron**.
- This can be accomplished by using a **FPGA for the real time analysis** of the data generated by the drift chamber and successively digitized by an ADC.
- There are three possible CC/T algorithms already implemented or yet to be implemented:
 - **Derivative** (implemented): It is based on the first and second derivative of the digitized signal function
 - **RTA** (under development): It is based on a bin-by-bin difference of the waveform with a normalized search template.
 - **RNN / CNN** (to be implemented): Long Short-Term Memory (LSTM), and Recurrent Neural Network (RNN) for peak finder

Derivative algorithm

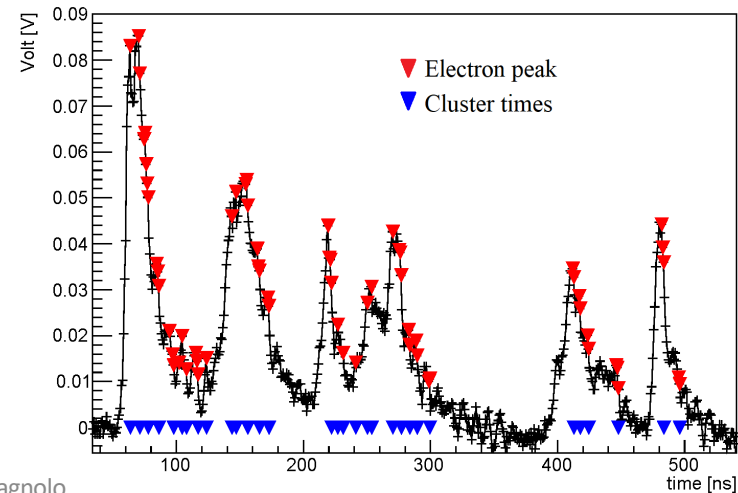
- A first simple tested algorithm of peak finder is based on the first and second derivative of the digitized signal function f , is defined for each time bin i , Δb being the number of bins over which the average value of f is calculated:

$$f'(i) = \frac{f(i) - \bar{f}(i - \Delta b)}{\Delta b} \quad f''(i) = f'(i) - f'(i - 1)$$

- A peak is found when $\Delta f, f'$ and f'' are above pre-defined threshold levels.

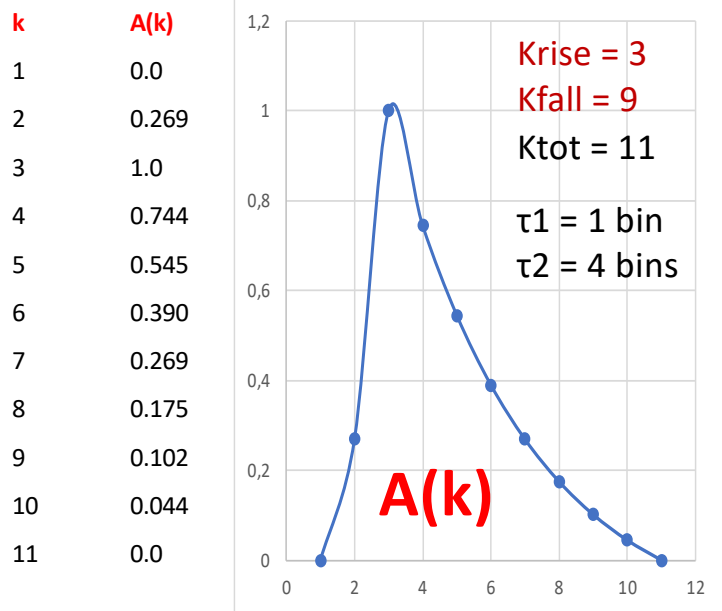


2 cm drift tube Track angle 45°

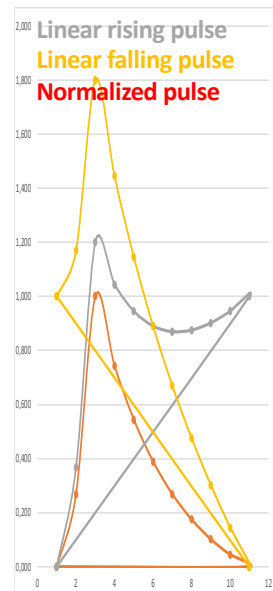


Recursive Template Algorithm

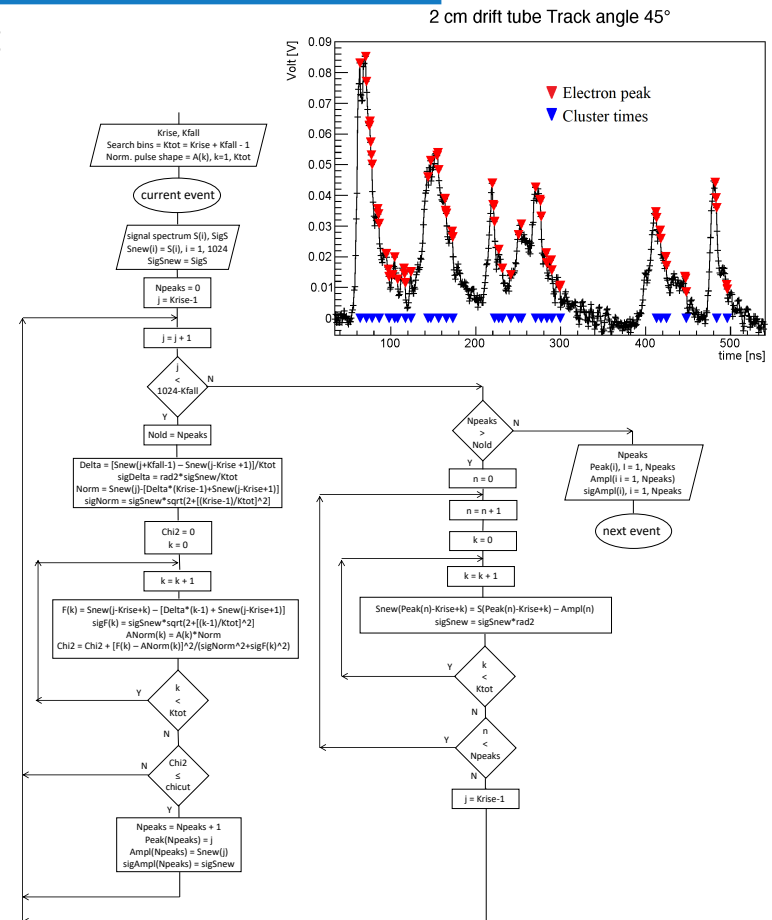
- Optimization in progress to compare performance with respect to the derivative algorithm.
- Both algorithms are quite elementary from the computational point of view for implementation in FPGA's with few parameters to be optimized.



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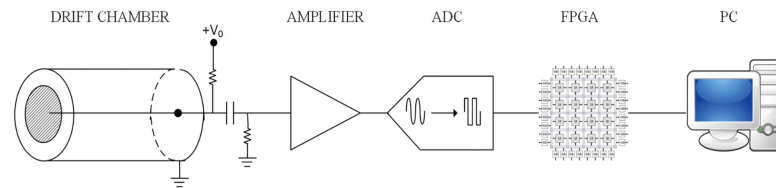
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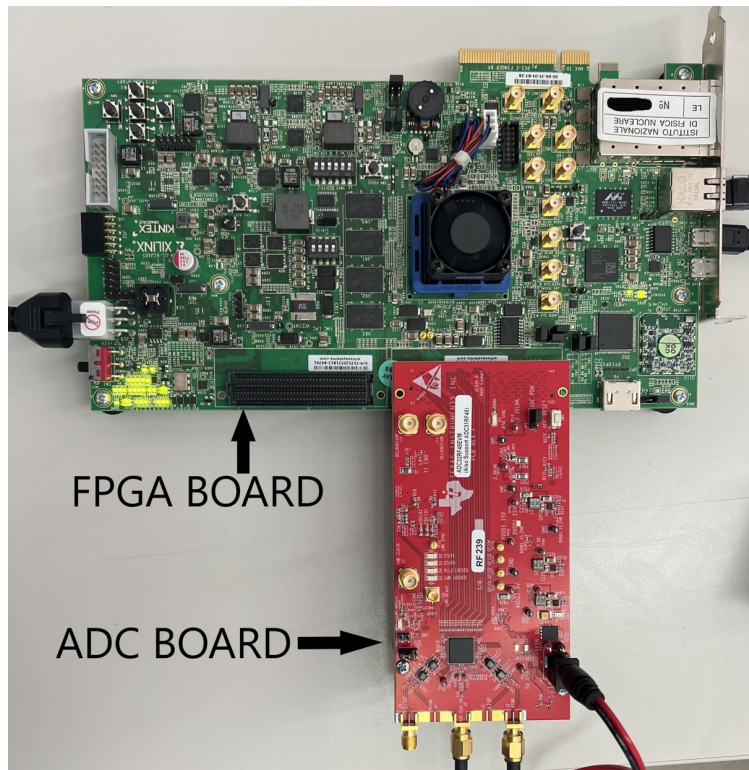
Algorithm implementation

The verified solution for a single channel



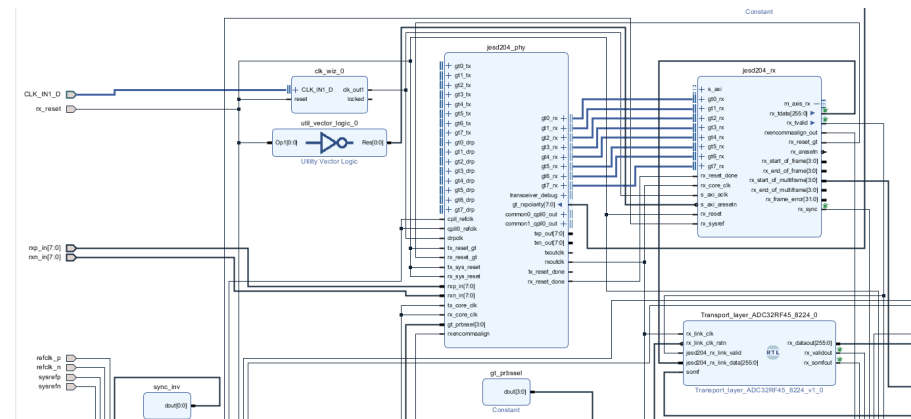
- To implement a board with **multiple channels** readout, three different approaches are currently being tried:
 - **TEXAS INSTRUMENT ADC32RF45**
 - **NALU SCIENTIFIC ASoCv3 and HDSoc**
 - **CAEN digitizer VX2751**
- First task (in particular, for the first and second case) is implementing the **data transfer to the DAQ system** to take advantage of the **10Gbit/s standard**:
 - optical fiber with SFP + connectors
 - SFP + to RJ45 adapters
- Second task is finding the most efficient way to **store the elaborated information** before the data transfer.

KCU105 + ADC ADC32RF45



25/04/23

- The code for the single channel in the old framework has been translated to the new Xilinx framework
- The communication with the new ADC has been carried out and simulations of timing and power consumption have been completed
- The code for using the 10Gb standard SFP + connections has been developed (next slide)
- The integration between the CC/T algorithm block needs to be terminated



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KCU105 + ADC ADC32RF45: 10G SFP+

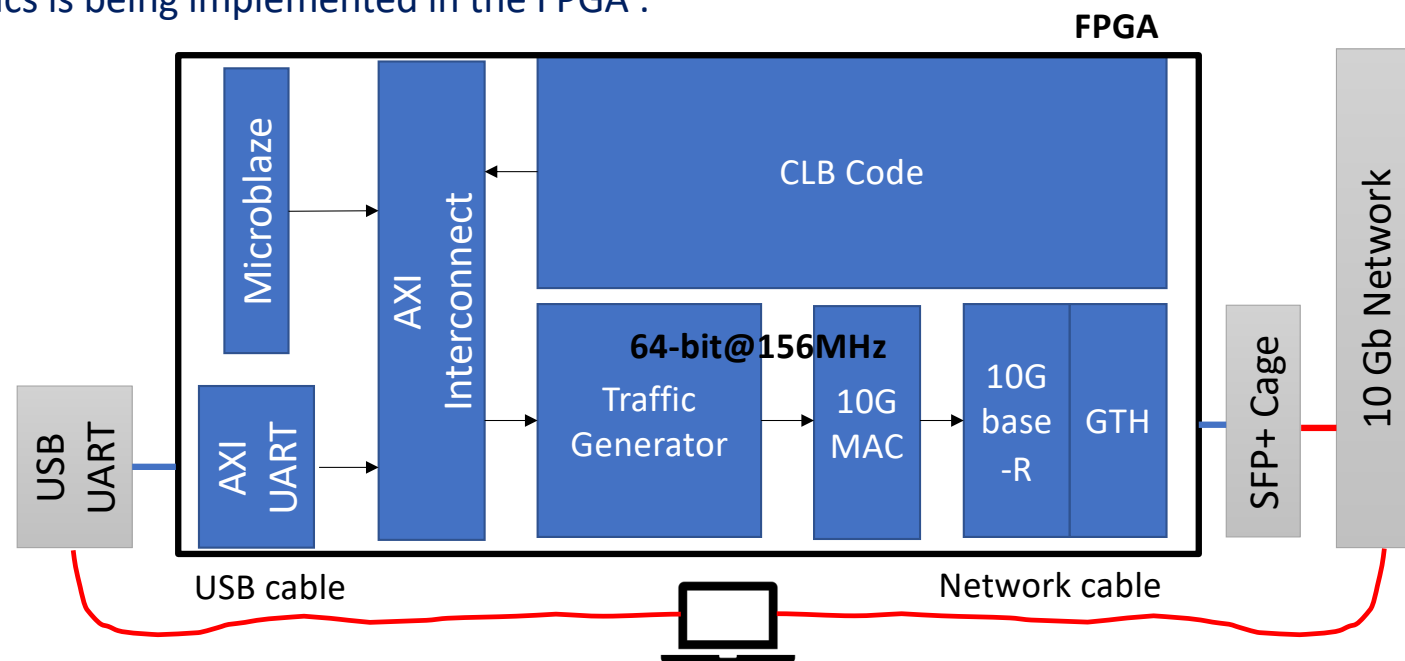
- A 1Gb network is sufficient for a single ADC but, in some cases, one has packet losses or corruption: during the tests some synchronization problems on the second channel of the ADC have been experienced
- To speed up communication with DAQ and PC, a data communication through the SFP + ports has been developed with a 10Gb speed via fiber or copper (a small local network is being set up)
- The following block schematics is being implemented in the FPGA :



10Gb SFP+



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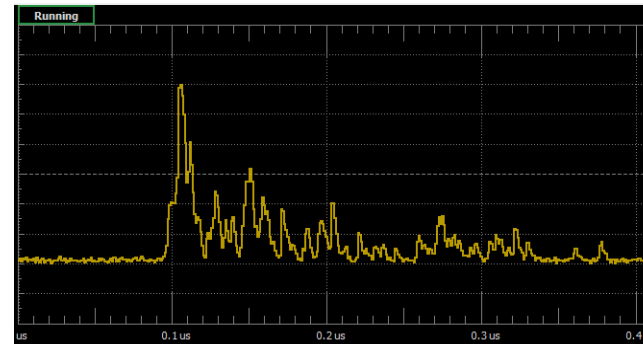
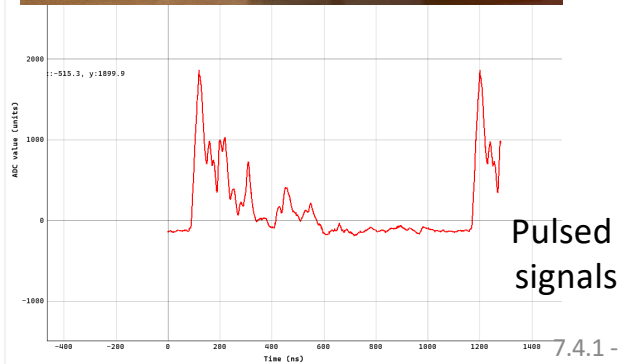
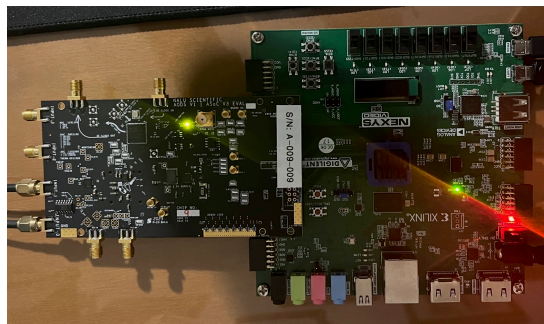


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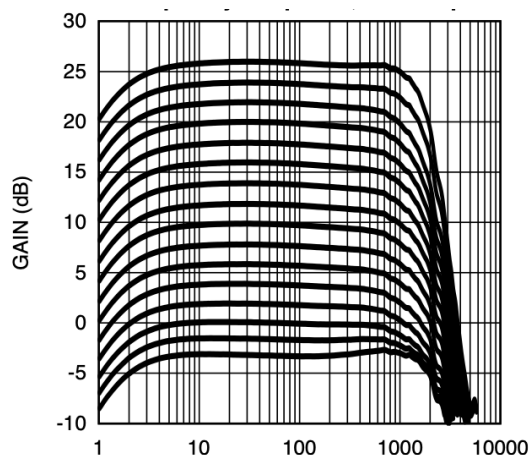
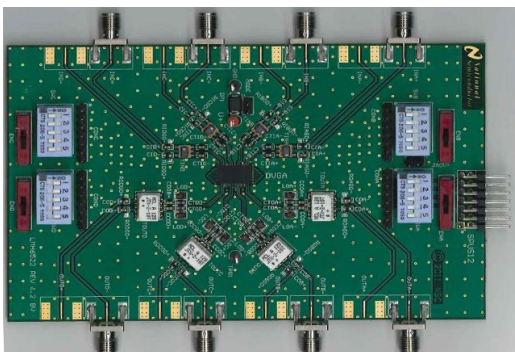
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Naluscientific ASoCV3

- We have recently received from **Naluscientific** a 4-ch **ASoCv3** evaluation board, which is currently being tested with a pulse generator
- Next task is to connect the ASoCv3 board to a 4-ch amplifier (**LMH6522**) to perform tests with drift tubes
- Currently we cannot implement the algorithm directly because we do not have access to the source code (we are in strict contact with Naluscientific) and use their acquisition software (**Naluscope**)



LMH6522



- So far single or dual channels amplifiers have been used. For a DC with several tens of thousand channels, the amplifier PCBs need considerable space close to the detector, therefore, the **distribution of power and of cooling** may impose serious constraints.
- The basic idea is to use a single chip to **drive one or more multi-channel digitizers**

A possible choice: LMH6522

- The **LMH6522** contains 4, high performance, digitally controlled variable gain amplifiers (DVGA).
- The **gain** is digitally controlled over a **31 dB range**.
- Gain Step Accuracy: **0.2 dB**
- **Disable Function for Each Channel**
- **1,5 GHz Bandwidth**
- **-65 dBc cross talk** between adjacent channels
- **Low Power Mode for Power Management Flexibility (about 400mA)**

Naluscientific HDSoc

Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoc	1-3	0.6	2k	64	80-120	May'21
AARDVARC	8-14	2.5	32k	4	4	Rev 3 avail
AODS	1-2	1	16k	1-4	100-200	Rev 1 avail
STRAWZ	5	2	2k	64	10	Dec'22


HDSoc

Parameter	Spec
Sampling Rate	1-2 GSa/s
ABW	> 600MHz
Depth	2k Sa
Trigger Buffer	~3 us*
Deadtime	0**
Channels	64
Supply/Range	2.5
ADC bits	12
Timing accuracy	80-120ps
Technology	250 nm CMOS
Power	TBD

- We expect a **HDSoc evaluation board** within this month, thanks to CAEN Technologies US branch (Naluscientific distributor)
- CAEN will also send us a FERS card and, most likely, the IP core to be able to implement our algorithms

Caen VX2740

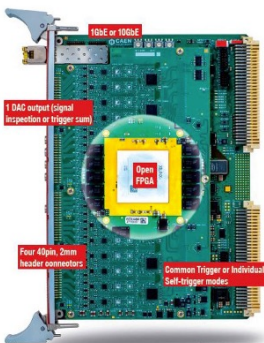
- We have been provided by **CAEN** with the **VX2740** digitizer (a lower performance version of the **VX2751**, better suited for CC/T and still under development and test)
- We are becoming familiar with the **openFPGA SCICompiler** software (released a few days ago) and we are using a trial license with a timebomb, not allowing us to do full development.
- We are waiting for CAEN to have a full license



VX2740: the first of a kind

64 channel, 125 MS/s, 16 - bit waveform digitizer

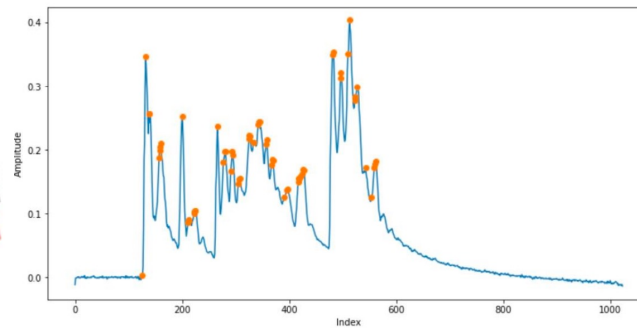
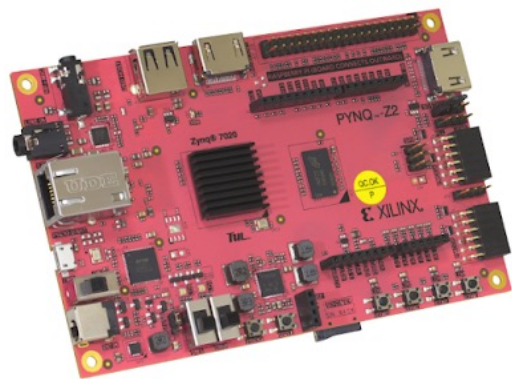
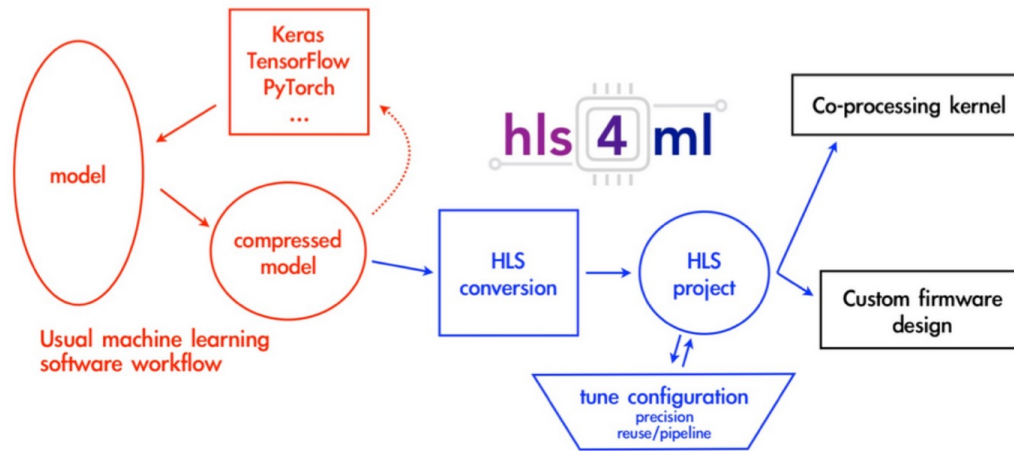
- High channel density spectroscopy
- Good fit for Neutrino and Dark Matter experiment
- **Open FPGA**: SCI-Compiler tool for beginners (**COMING SOON**) or advanced firmware template
- Four 40-pin, 2 mm header connectors with DIFF or SE inputs
- 1 GbE, 10 GbE, USB 3.0 and CONET 2.0 (optional) connectivity
- Common Trigger (waveforms) or Individual Self-trigger modes
- **DPP options**: PHA, QDC, PSD, CFD
- Advanced Waveform Readout modes: ZLE, DAW
- DT2740, 64 channels in Desktop form factor (**COMING SOON**)



Available in **desktop** form factor

Model	# channels	MS/s	# bit	Applications
x2740	64	125	16	64 MCAs for high channel density spectroscopy Good fit for Neutrino and Dark Matter exp. Currently available
x2745 Advanced version of x2740	64	125	16	Variable gain input stage Designed for Si detectors readout COMING SOON
x2725/x2730	32	250/500	14	Medium-fast detectors Sub-ns timing combined with high energy resolution Optimal trade off between cost and performances
x2751	16	1000	14	Ultra-fast detectors (diamond, MPCs, SiPMs) with ps timing applications Potential upgrade to higher sampling rate
x2724	32	125	16	Spectroscopy & MCA Advanced Front-End (gain, shaping, AC/DC coupling ...) Semiconductor detector (HPGe, Clover, SDD, ...) Typically connected to charge Sensitive Preamplifier

Implementing ML algorithms (for peak finding) on FPGA



The first step required for the implementation of **neural networks** on FPGAs is the conversion of the high-level code used for the creation of the network (**QKeras**) into a **High-Level Synthesis (HLS)**. To accomplish this task, the **hls4ml** package will be used. A schematic workflow of hls4ml is illustrated in the figures.

1. The red section indicates the usual software steps required to design a neural network for a specific task.
2. The blue section of the workflow is the task done by hls4ml, which translates the model into an HLS project that can be synthesized and implemented to run on an FPGA.

Milestones and deliverables

Milestones

- month 36: 4-ch system board (ADC + FPGA) engineered (support from CAEN)
- month 46: board completed

Deliverables

- month 46: board tested under particles beams (written report)

Despite the various delays experienced (COVID-19 pandemic, cancellation of Russian support), we think that this schedule can reasonably be met.