WP11 summary

2nd annual meeting

A. Rivetti (INFN) Ch de La Taille (CNRS)

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

Objectives

- **Task 11.1. Coordination and Communication [CNRS+INFN]**

- **Task 11.2. Exploratory study of advanced CMOS (28 nm)**
  - INFN PV, AGH, CNRS CPPM, UBONN
  - Explore advanced 28 nm CMOS for future trackers AGH, CNRS CPPM
  - Design and test front-end prototypes INFN PV, UBONN

- **Task 11.3. Networking and ASICs for other WPs (65/130 nm)**
  - AGH, CNRS OMEGA, IP2I, DESY, INFN (BA, BO, PV, TO) Uni Heidelberg, WEEROC (industry)
  - Cold and timing ASICs in 65/130nm CMOS : CNRS OMEGA, IP2I
  - MPGD readout ASICs : INFN (BO, TO)
  - Silicon and SiPM readout ASICs for future colliders and timing applications : AGH, CNRS OMEGA, DESY, UniH, WEEROC

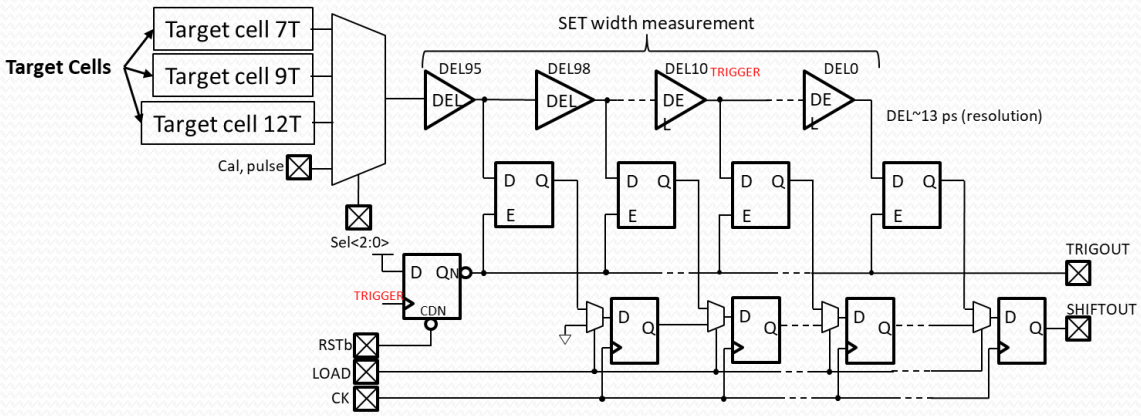
tasks 11.2 (28 nm)

- AGH : study ADCs and PLLs and participate to next LPGBT
  - Ultra-low power ADC 10bits 100 MHz <1 mW : simulations in progress
- CPPM : test vehicles for SEU/SET and TID studies : prototyped in dec 22
- Ubonn : study FPGA implementation for next generation chips and digital blocks
- INFN PV : work in synergy with FALAPHEL INFN project, further studies of analog front-ends and IP blocks
  - Two different Analog Front Ends are being investigated :
    - ToT A/D conversion, Flash A/D conversion
  - Foreseen MPW in oct 2023

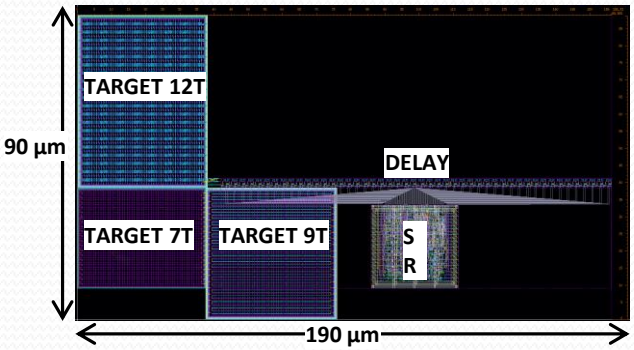
Falaphel

SET Bloc design

SET sub-bloc synoptic

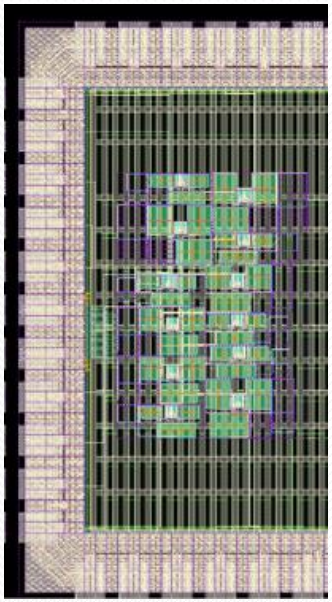


Designer : Denis Fougeron



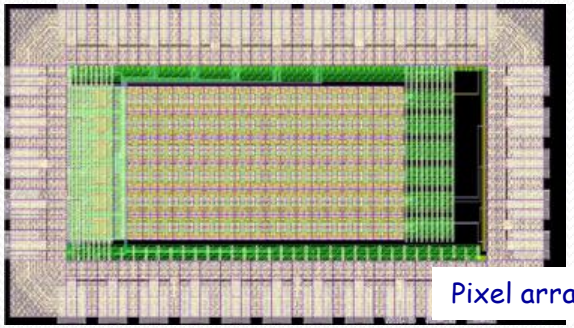
Layout example for INVD4 cell

- Each sub-bloc contains
  - 3 target cells made up of thousands of basic cells + 1 calibration input
  - Circuit for SET width measurement 96 delay cells (13ps/cell) -> from a few ps to 1 ns
  - Shift register to send the data to the output when a trigger signal occurs
- 31 SET sub blocs
  - 24 uses SVT target cells (7T, 9T, 12T) -> **Effect of the cell size**
  - 7 uses LVT or HVT target cells -> Effect of **the device options**
- The whole bloc contains 6 inputs / 13 outputs
- In addition to SET testing, this constitutes a sub-block of the TDC required in the pixel front end

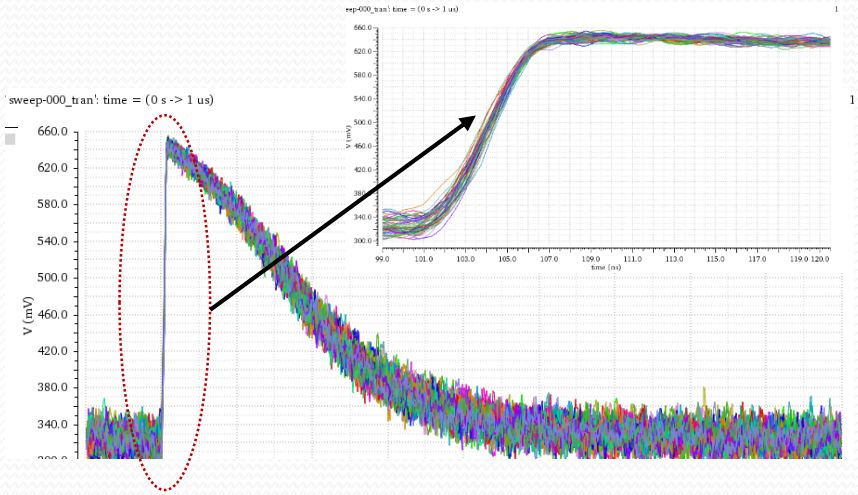


Analog FE pixel prototype

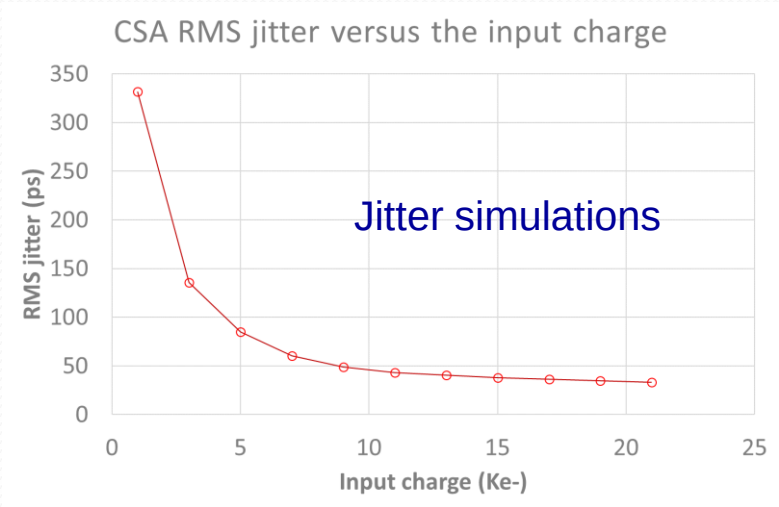
- For each pixel :
  - The charge amplifier current bias can be set in the range of 2µA-20µA
  - MOM capacitance connected to each preamplifier input -> test for different input capacitance values
- Large bandwidth buffers (> 1GHz) implemented and connected for a few pixels for direct jitter measurement
- Simulations for I_{CSA} = 5 µA
  - dV/dt = 100 mV/ns
  - RMS noise = 97 e- RMS for Cin = 100fF
  - Jitter < 100 ps RMS for input charge > 4 ke-
  - Jitter < 40 ps RMS for charge > 10 ke-
- Each pixel contains : CSA + Discriminator + 6 bit DAC
  - Size : 20 µm × 12 µm



Pixel array of 36 × 12 pixels



50 superimposed transient noise simulations



Bergamo/Pavia 28 nm activities in INFN projects

Falaphel (started in 2021)

- Development and integration of Silicon Photonics modulators with high speed, rad-hard electronics in 28 nm

INFN Padova, Pavia, Pisa, Scuola Superiore S. Anna di Pisa, UniPisa, UniMilano (P.I. Fabrizio Palla)

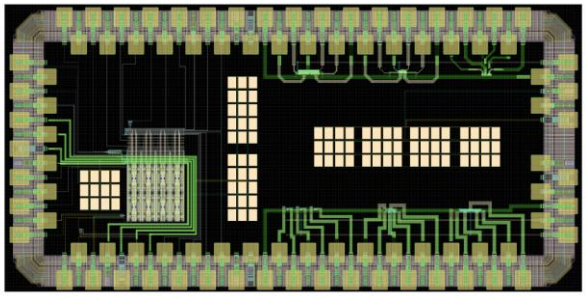
IGNITEd INFN Istituto Nazionale di Fisica Nucleare (started in 2023)

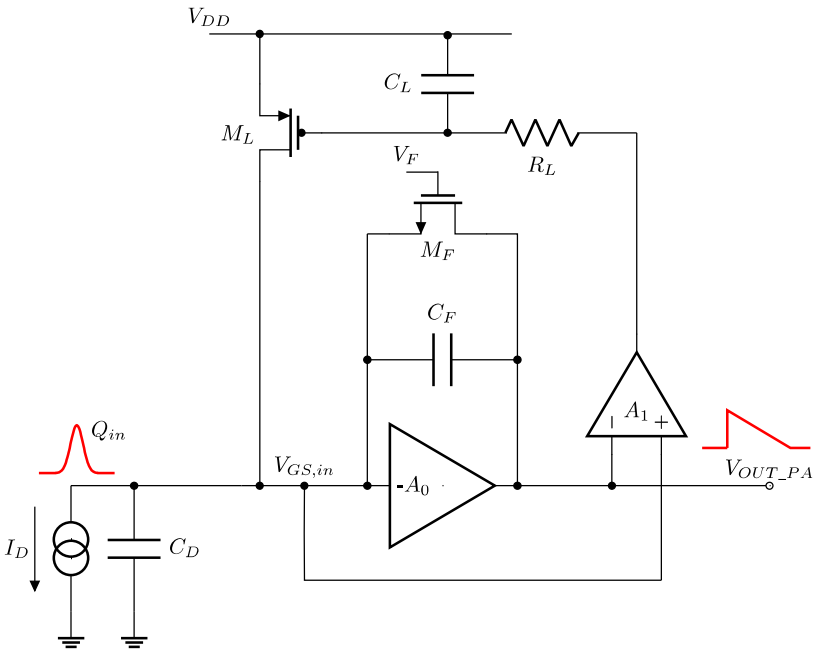
INFN Ground-up iNITiative for µElectronics developments

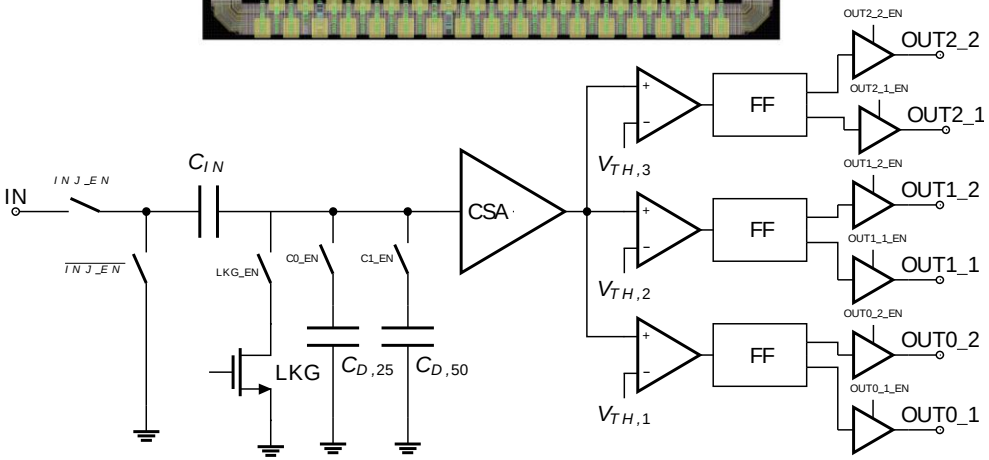
- develop a nominal-size, detector-grade ASIC (≈1-2 cm^2) in CMOS 28 nm technology, coupled to a Silicon Photonics integrated device for high-bandwidth data communications (4D tracking, rad-hard, low threshold operation,…)
- address the requirements of the inner trackers of the next generation of upgrades at colliders
- establish an operative and coordinated network for the exchange of competences at a national level and for a common R&D strategy in microelectronics

INFN Bari, Bologna, Cagliari, Firenze, Genova, LNF, Milano, Milano Bicocca, Padova, Perugia, Pavia, Pisa, Trento, Torino (P.I. Adriano Lai)

Flash ADC based front-end



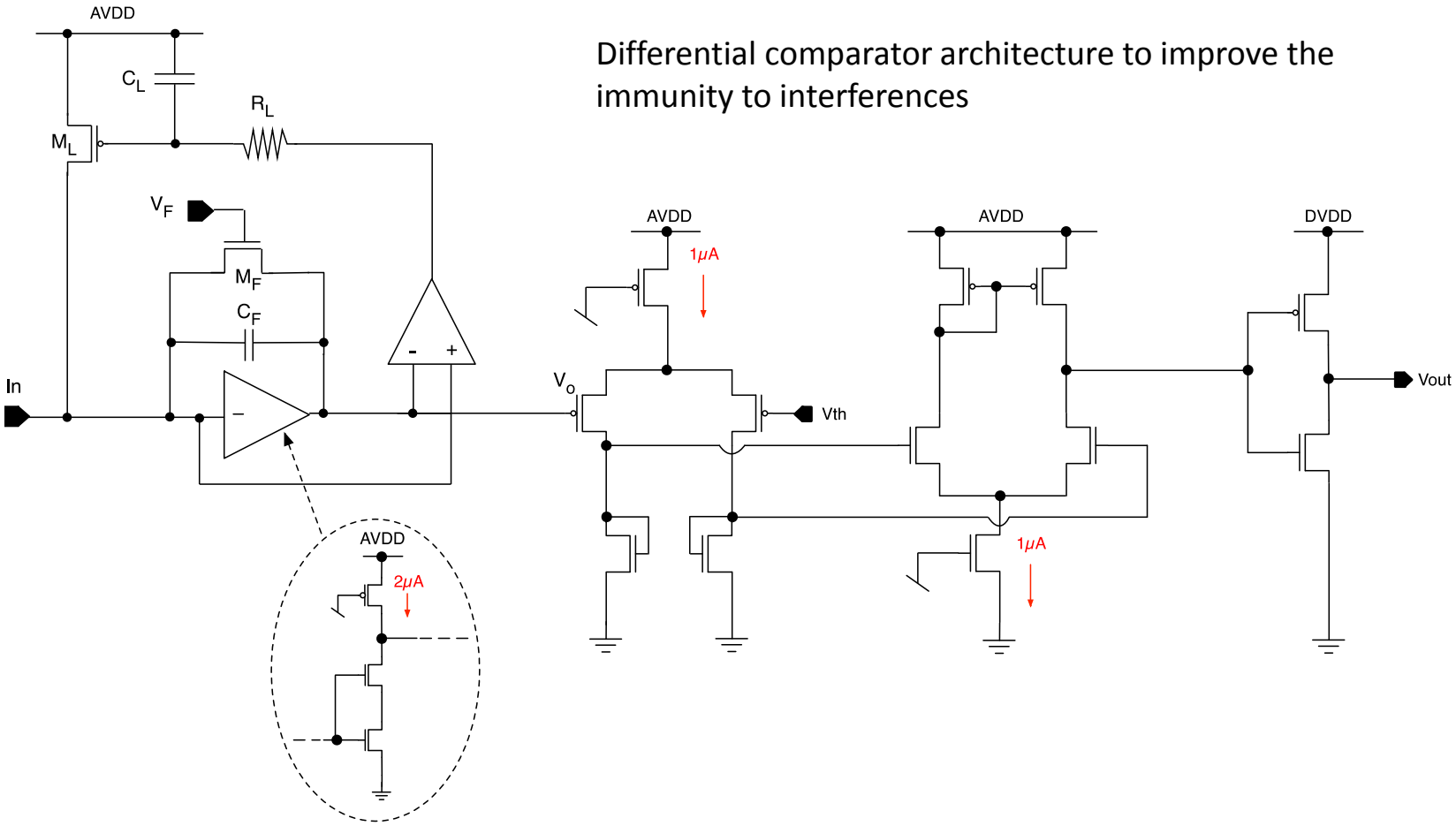




- **Equivalent noise charge @ preamp output** about 65 e rms for Cd =50 fF at – 20 °C
- Compensation of at least 50 nA sensor leakage current

- AC coupled comparators implementing a **2-bit flash ADC**
- **Auto-zeroed comparators**, operated with 40 MHz clock. The implementation is ideally insensitive to device threshold voltage mismatch → threshold tuning DAC not required
- Overall **current consumption**: 5.4 uA → 4.9 µW **power consumption** @ V_{DD}=0.9 V
- Elementary cell size: 25 x 50 µm^2 (analog+digital)
- Minimum **in-time threshold**: 600 e-

ToT-based front-end design



Differential comparator architecture to improve the immunity to interferences

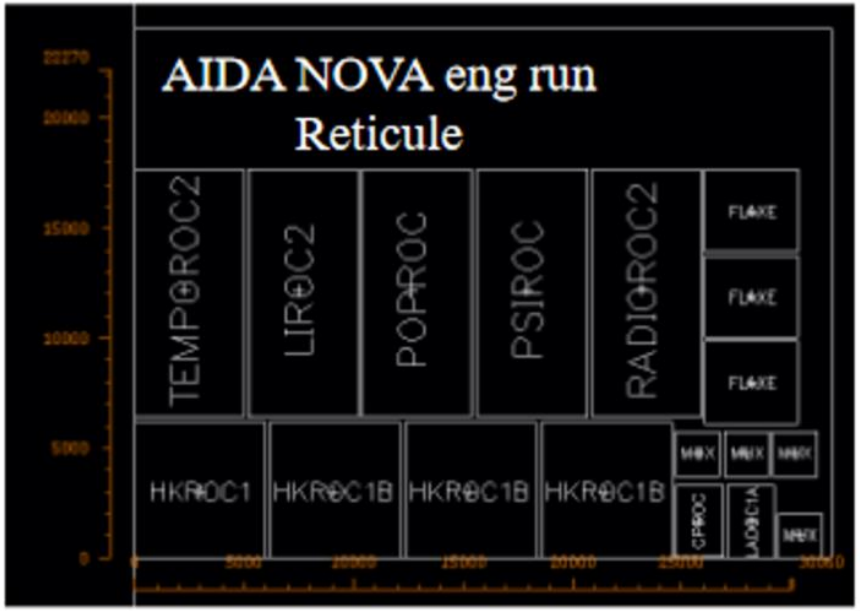
Tasks 11.3 (130 nm)

- AGH : FLAME/FLAXE readout ASIC for LUMICAL, new 10 ps TDC development
- CNRS IP2I : plan to do cryogenic tests on low dropout regulator prototype
- CNRS OMEGA : AC LGADs and PMT timing chip readout in 130 nm
- DESY/Heidelberg : study of SiPM Tile boards with KLAUS5/6 readout
- INFN BA/PV : MPGD 32ch readout ASIC in 130n 12b ADC + 100ps TDC, dual polarity, variable peaking time.
- INFN BO/LNF/TO : uRwell readout chip, based on TIGER chip. Test uRwell chambers with APV and TIGER. Design dedicated chip in 130n.
- INFN TO : engineering run in UMC110n for timing detectors
- WEEROC : SiPM readout for timing and LIDAR applications.

AIDA INNOVA engineering run

- AIDA participation in a 130nm engineering run constitutes D1.1
  - ~25% of the reticle area = 25% of the total cost (300k€)

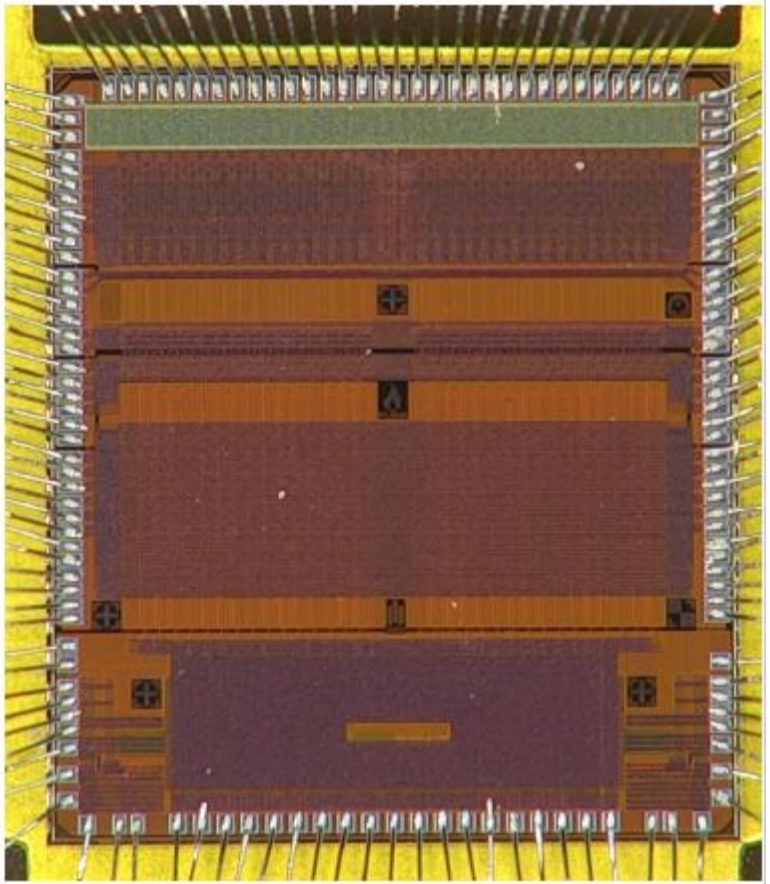
- 4 chips from AIDA-INNOVA partners on this run
  - FLAXE (AGH) : Si/GaAs readout
  - EICROC (OMEGA/AGH/CEA) : LGAD readout
  - LIROC (WEEROC) : SiPM timing
  - PSIROC (WEEROC) : Si readout
  - Submission april 2023
  - Several hundreds of chips will be available



- Chips reviewed in november 2022
  - Constitutes Milestone MS46

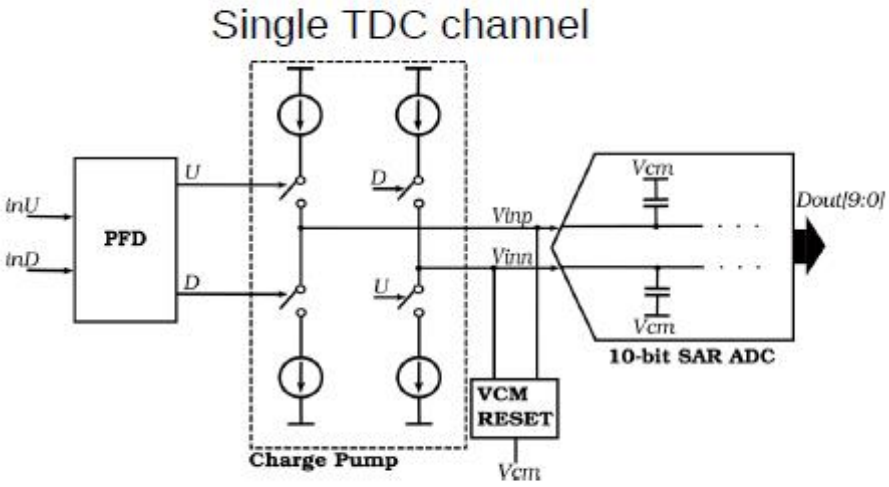
Activities in TSMC 130nm
FLAME & FLAXE ASICs in LUXE experiment

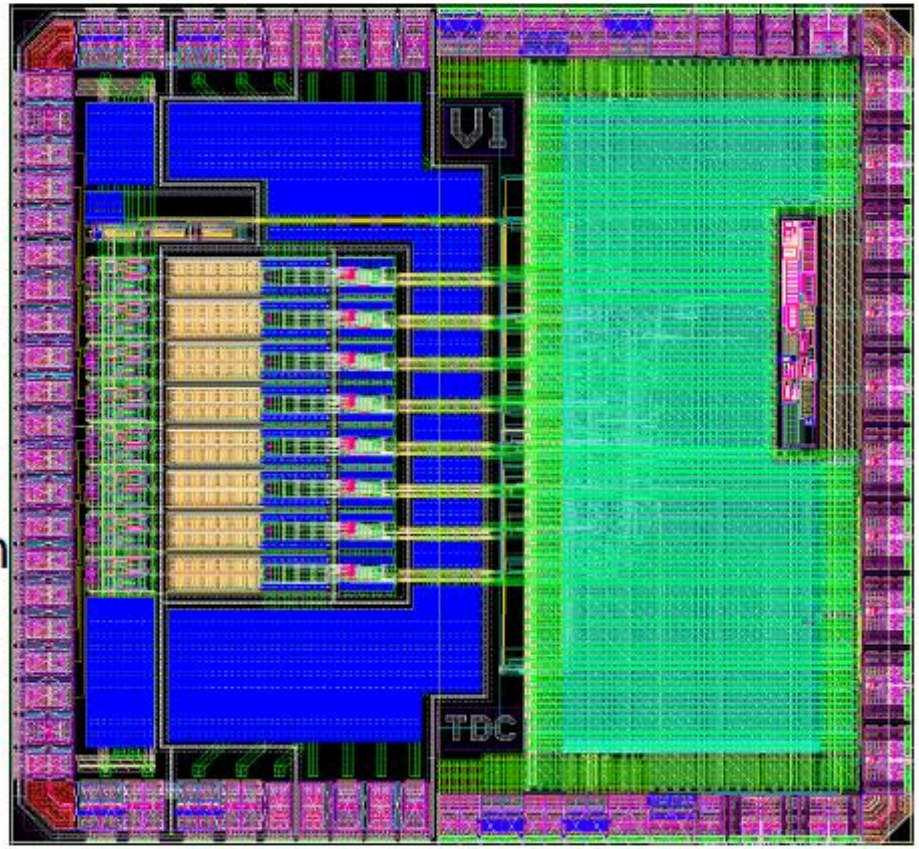
- For ECAL detector in LUXE experiment a new FLAME-based chip called FLAXE (FLAME with much lower data transmission rate) was designed
- Presently FLAME chips are used for first LUXE test-beams. In the last test-beam at DESY, 11-18 September 2022, a 4-chip front-end board (128 channels) was used to study the performance of Si and GaAs sensors and shower development. A lot of data was collected – analyses in progress…
- FLAXE ASIC has been just submitted for production



FLAME

Activities in TSMC 130nm
R&D on precise TDC (~10ps) in CMOS 130nm





- New TAC-based TDC aiming with timing measurement precision of ~10ps, consuming ~1mW per channel, was designed
- 8-channel prototype TDC chip was produced 2022
- Test setup in progress...

New publications

An lpGBT Subsystem for Environmental Monitoring of Experiments

lpGBT collaboration

Mirosław Firlej,[a,1] Tomasz Fiutowski,[a] José Fonseca,[b] Marek Idzik,[a] Szymon Kulis,[b] Paulo Moreira,[b] Jakub Moroń,[a] Krzysztof Świentek[a]

[a] *Faculty of Physics and Applied Computer Science, AGH University of Science and Technology, Al. Mickiewicza 30, 30-059 Kraków, Poland*

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Abstract: In this paper, the Low Power Giga Bit Transceiver (lpGBT) built-in system for environmental monitoring of the LHC experiments is presented. Eight external analogue inputs and eight internal voltages are multiplexed into an instrumentation amplifier with selectable gain, whose output is digitised by a 10-bit SAR ADC. A programmable current source can be enabled for each external input to implement resistance measurements. Internal channels are used to monitor power supplies and the output of the temperature sensor. The environmental monitoring system includes a precise 1 V reference voltage source and a 10-bit voltage DAC. All blocks were designed and fabricated in 65 nm CMOS technology, fully characterised, and the pre- and post-irradiation measurement results are presented in this work.

JINST - just accepted

An Ultra-Low Power 10-bit, 50 MSps SAR ADC for Multi-Channel Readout ASICs

Mirosław Firlej,[a] Tomasz Fiutowski,[a] Marek Idzik,[a] Szymon Kulis,[b] Jakub Moroń,[a,1] Krzysztof Świentek[a]

[a] *Faculty of Physics and Applied Computer Science, AGH University of Science and Technology, Al. Mickiewicza 30, 30-059 Kraków, Poland*

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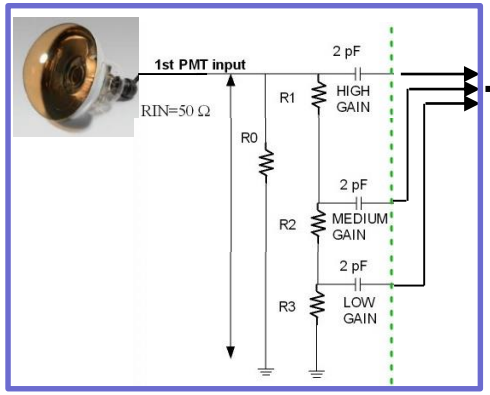
Abstract: The design and measurement results of a fast, ultra-low power, small area 10-bit SAR ADC, developed for multi-channel readout systems, in particular for applications in particle physics experiments, are discussed. A prototype ASIC was designed and fabricated in 130 nm CMOS technology and a wide spectrum of static (INL < 0.4 LSB, DNL < 0.3 LSB) and dynamic (ENOB = 9.45) measurements was performed to study and quantify the performance of ADC. The ADC converts analogue signals with a sampling frequency up to 55 MHz and power consumption below 1 mW. The ADC works asynchronously, so no external clock is required. The ADC Figure of Merit (FOM) at 50 MHz sampling frequency is 24 fJ/*conv.-step*, and is the lowest among the State of the Art designs with similar technology and specifications.

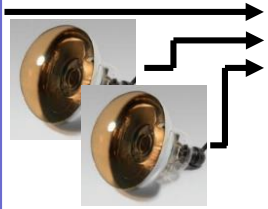
submitted to JINST

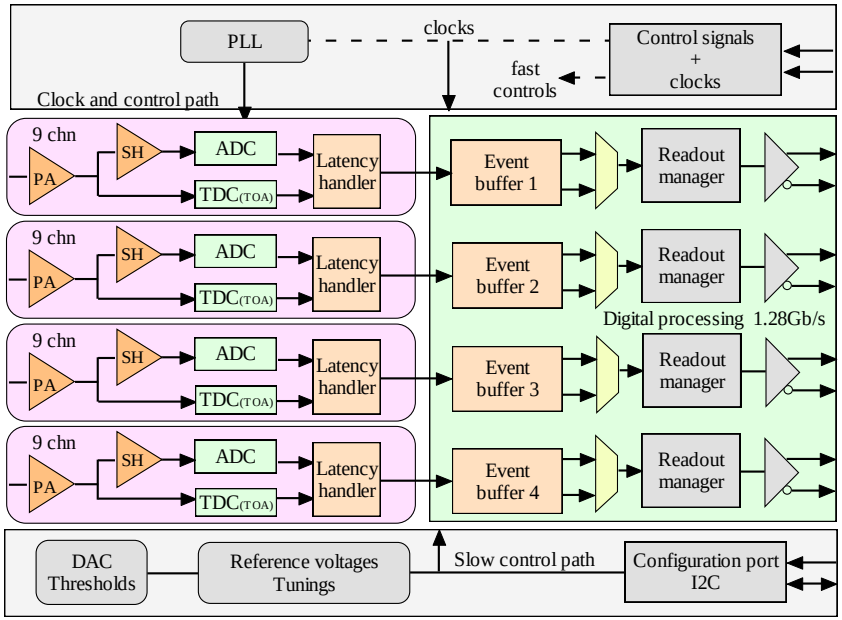
Publication on 80-90 MSps 10-bit ADCs in 65 nm almost completed...

HKROC PMT charge and time readout

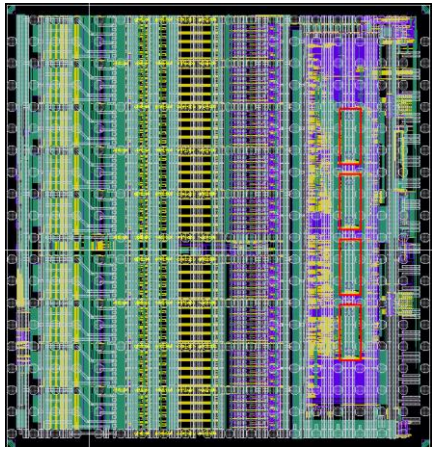
- HKROC has 36 channels: 12 PMTs with High, Medium and Low gain
  - Or 36 PMTs with one gain





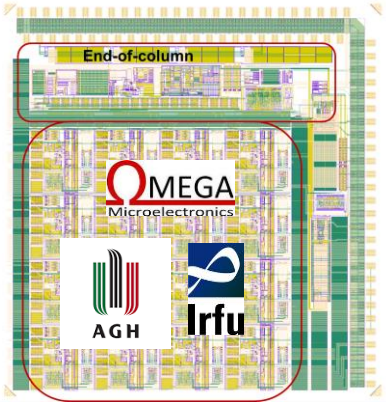


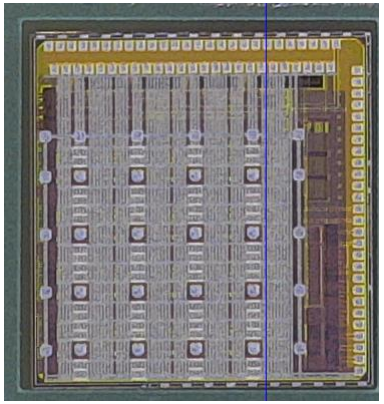
- ASIC in TSMC 130 nm node
- Low power: 10 mW per channel
- Large charge measurement with 3 gains (up to 2500 pC), < 1% linearity
- Integrated timing measurements (25 ps binning)
- Readout with high speed links (1,28 Gb/s), Hit rate up to ~40 MHz
- HKROC is a waveform digitizer with auto-trigger and TDC



EICROC0 : AC LGAD readout

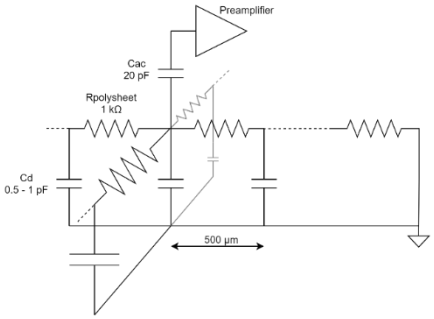
- EICROC0 is a 16-channel testchip for AC-LGADs at EIC
  - Based on ALTIROC (ATLAS HGTD) front-end and HGCROC (CMS HGCAL) ADC/TDC
  - Reads 500x500 µm pixels for sensor evaluation
  - Readout designed for testbeam (not EIC)
  - Fabricated in march 2022, received beg july 2022
  - now under test at IJCLAB and OMEGA
  - New submission in AIDA innova eng. run

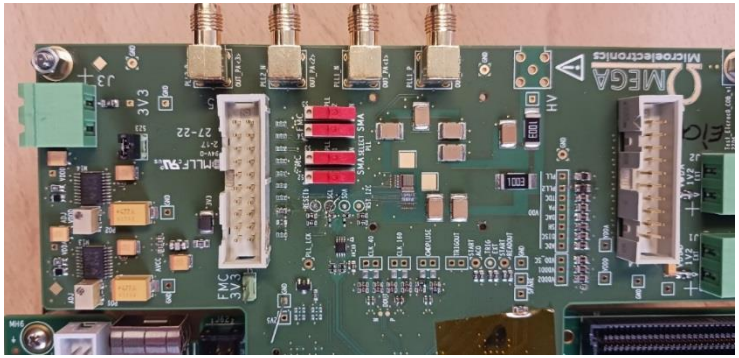




New concept of sensor [N. Cartiglia et al.]

- AC coupled LGAD: **large signal and fast timing**
- Resistive layer for charge sharing: high position resolution
- « Large » pixel allows implementation of **ADC and TDC pixel-wise**





Implication in DRD6 (ECFA Calorimetry R&D)

Trends for calorimeter readout

- On-detector embedded electronics, low power multi-channels ASICS
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC Lar, FATIC…
  - Challenges: # channels, low power, digital noise, data reduction, timing capability

- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC-ee, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence + joint optimization
  - Detector specific front-end but common backend
  - Allows common DAQ and facilitates combined testbeam

- Start from HGCROC / HKROC: Si and SiPM
  - Reduce power from 15 mW to few mW/ch
  - Allows better granularity
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - Several improvements foreseen in the VFE and digitization parts
  - 130 nm or 65 nm ?

Networking and ASICs for other WPs

- **Design and production of several UMC110AE "service" ASICS**
- **Multiple MPWs and engineering runs with production ongoing, silicon expected in May and June 2023**

  - **CASTOR**: Analogue readout chip for cryogenic large-area silicon photomultipliers (SiPMs). A total of 1920 chips (each chip reads a 24cm^2 cryogenic SiPM Tile) will be mounted on the VETO detector of the Darkside-20K dark matter experiment at LNGS. The construction is ongoing and the start of operation of Darkside-20K is due to beginning 2026.

  - **FAST3**a/b/c/d/e/f: Analogue Low-Gain Avalanche Diode (LGAD) sensor readout chip prototypes for scientific R&D purposes; analogue and fast trigger outputs.

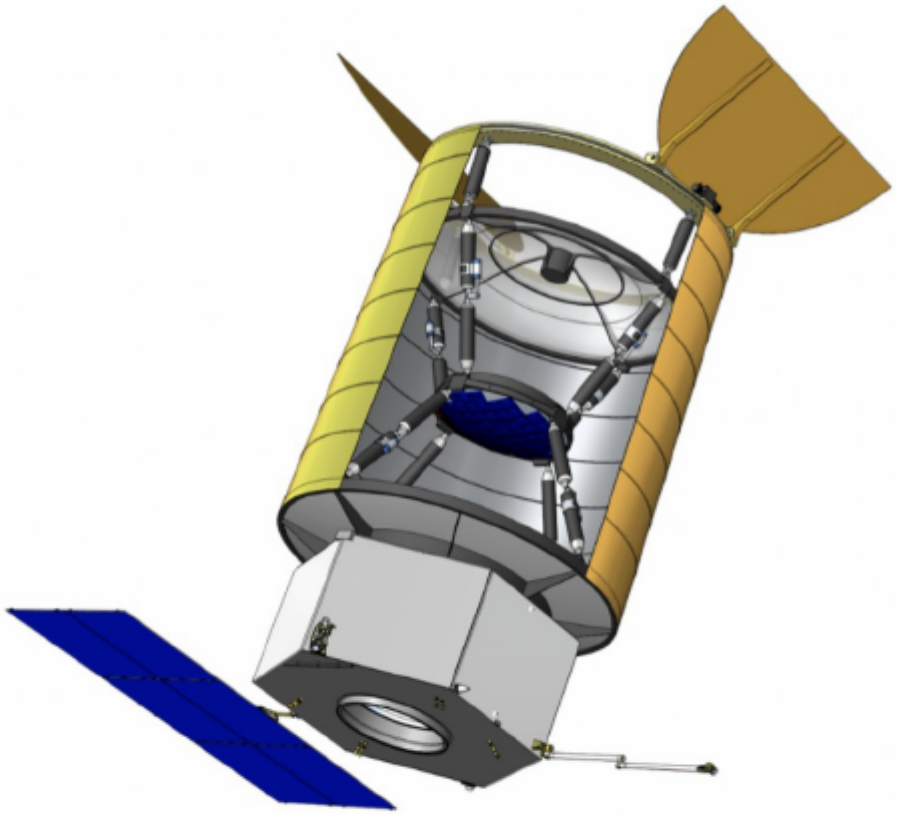
  - **Microbs**_F0/2/3: Multi-channel particle counter chip for microdosimetry and beam monitoring using LGAD sensors.

Networking and ASICs for other WPs

- **Design and production of several UMC110AE "service" ASICS**
- **Multiple MPWs and engineering runs with production ongoing, silicon expected in May and June 2023**

  - **ALCOR_EIC**: Mixed-signal 32-pixel SiPM readout chip for a dual-radiator Ring-Imaging Cherenkov (dRICH) detector at the future Electron-Ion Collider (EIC).
  - **ALCOR_3D**: Mixed-signal 32-pixel SiPM readout chip for 3D SiPM modules, implements matrix of bump pad openings on top of the 32-pixel matrix;
  - **ALCOR_UFSD**: Mixed-signal 32-pixel Low-Gain Avalanche Diode (LGAD) sensor readout chip.
  - **ALCOR**: prototype version performing test-beams with SiPMs (framework of EIC-NET dRICH) and LN 77K tests with SiPMs mounted on an single ALCOR test board (Astrocent) and on an octo-ALCOR board with 256 channels (INFN-BO).

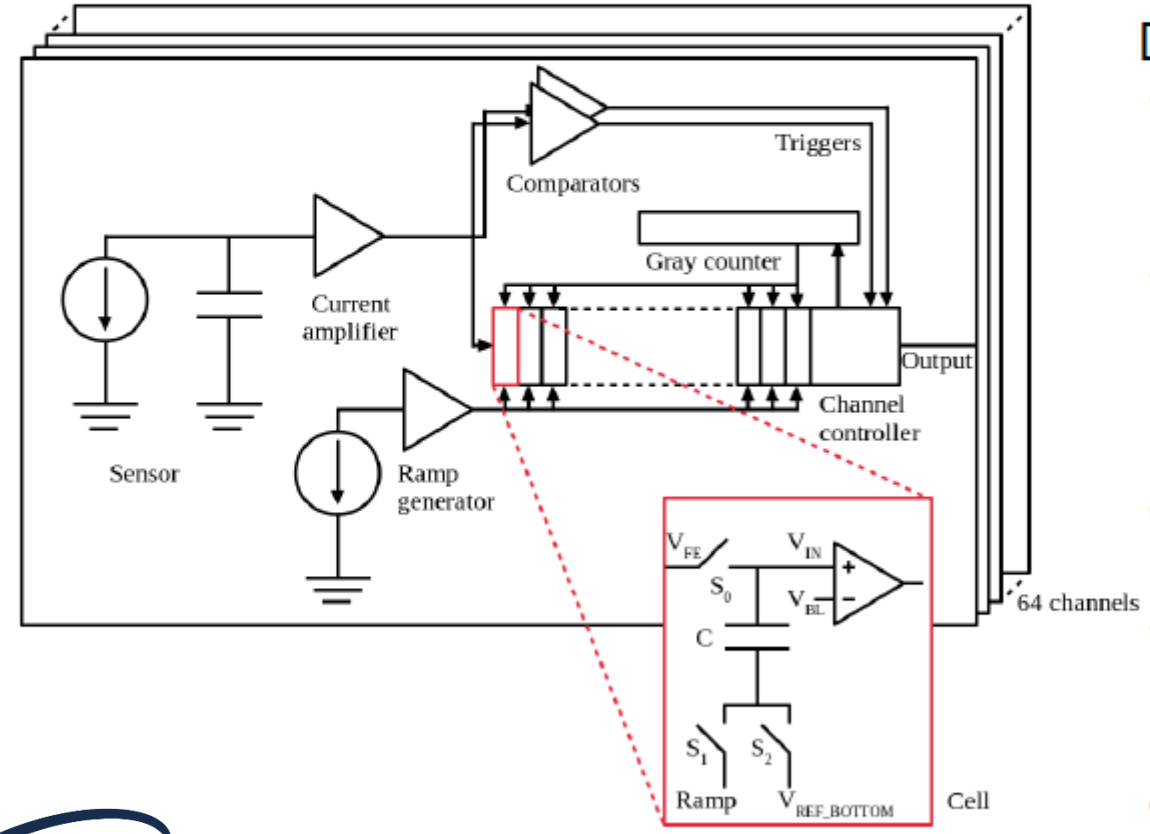
Research context



Angela V. Olinto, POEMMA and EUSO-SPB: Space Probes of the Highest Energy Particles, 2018

- Detection of **Extensive Airshowers** (EASs) generated by **Ultra-High Energy Cosmic Rays** (UHECRs) beyond 100 PeV and **Cosmic Neutrinos** (CNs) through Cherenkov radiation processes.
- The fast sampling of the signal is mandatory: 200 MHz.
- 64-channel ASIC implemented in a commercial 65 nm CMOS technology.
- A system to readout a camera plane composed by a matrix of Silicon Photo-Multipliers (SiPMs).

ASIC architecture



Design status:

- Mode:
  - Sparse
  - Imaging
- Segmentation:
  - 32 cells
  - 64 cells
  - 256 cells
- Resolution:
  - 8 - 12 bits
- Trigger:
  - Internally generated
  - Externally provided
- 8-channels readout

INFN TORINO

RADIOROC schematic

Trigger :

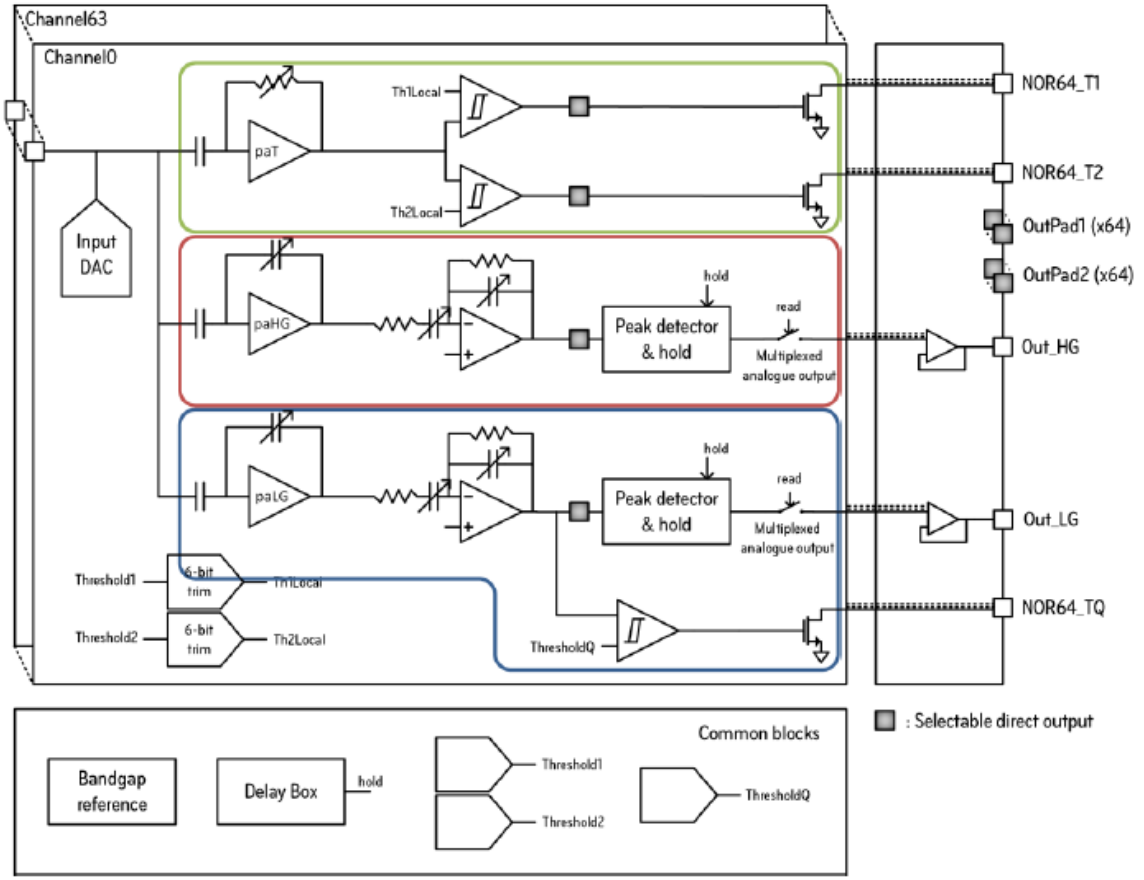
- Dual threshold
- Time resolution of 55 ps FWHM on a single pe (160 fC);
- Photocounting over 200 MHz ;
- TOT.

High gain charge measurement :

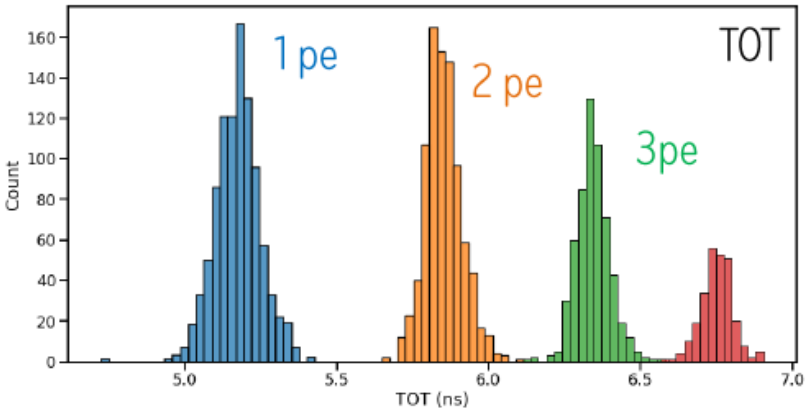
- SNR > 10 ;
- 1% linearity up to few hundreds of photo-electrons ;
- Gain 5 to 80 ;
- Shaping time 20 ns – 300 ns.

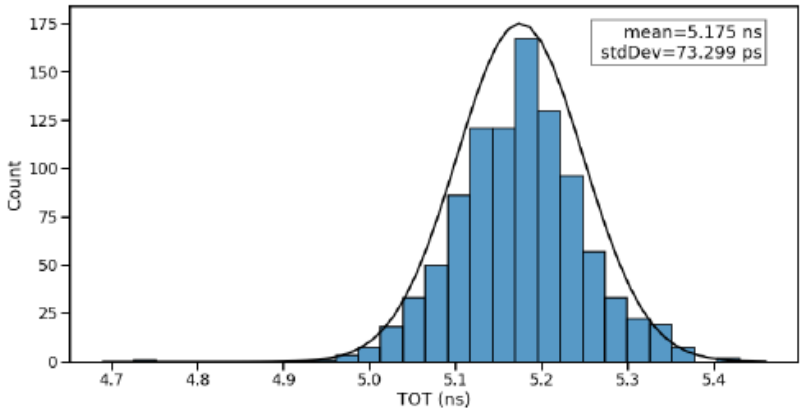
Low gain charge measurement :

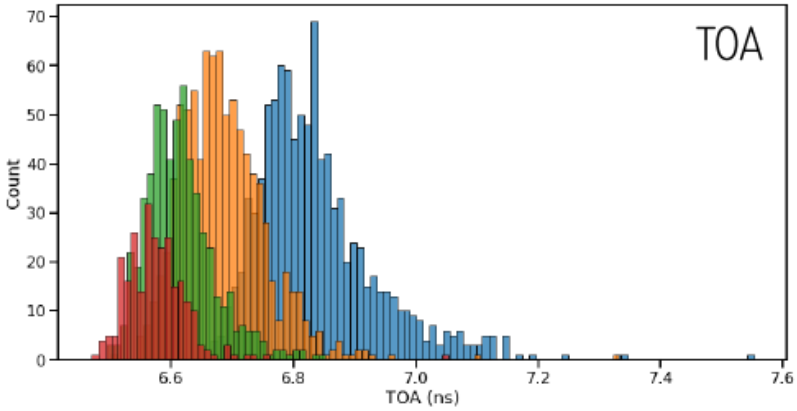
- Charge veto ;
- 1% linearity up to few thousands of photo-electrons ;
- Gain 0.5 to 8 ;
- Shaping time 20 ns – 300 ns.

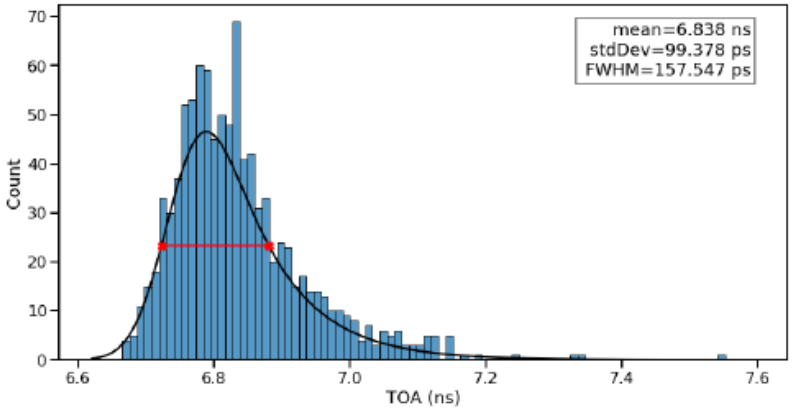


SPTR (SiPM + radioroc)





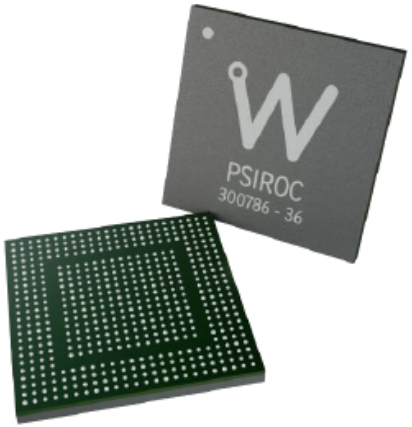


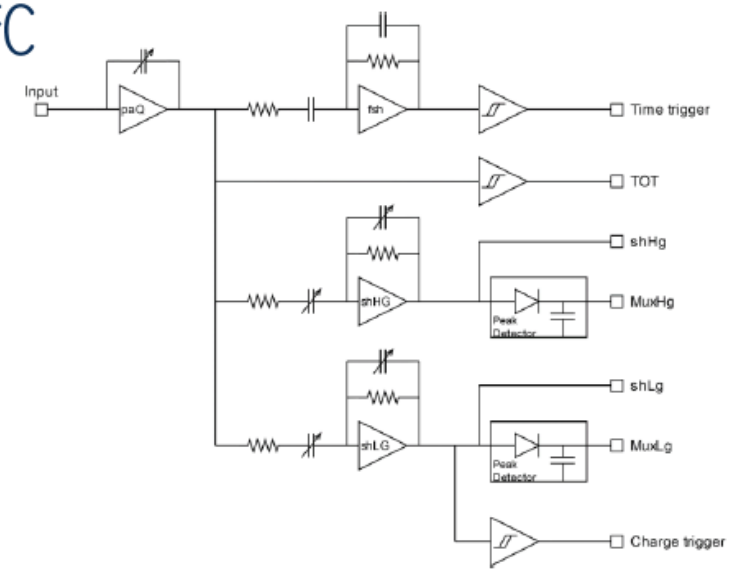


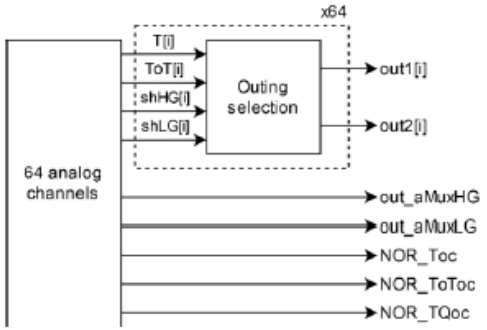
Electronics has a negligible effect, SiPM jitter is the limiting factor

Psiroc – read-out low gain detector

- Psiroc =radioroc + charge preamplifier + dual polarity
- APD / GEMs / Si strips, etc…
- Trigger on 0,5fC

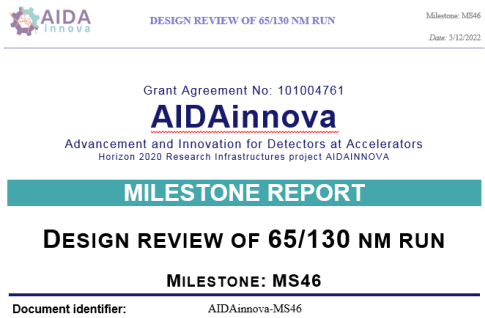






Deliverables/Milestones

- 2 Milestones and 2 deliverables
  - MS 11.1 and 11.2 (MS45 MS46) passed end 2022
  - D11.1 and 11.2 are the corresponding chips


AIDA innova DESIGN REVIEW OF 65/130 NM RUN Milestone: MS46 Date: 3/12/2022

Grant Agreement No: 101004761

AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

DESIGN REVIEW OF 65/130 NM RUN

MILESTONE: MS46

Document identifier: AIDAinnova-MS46

MS11.1	**Design review of 28 nm MPW**	**11.2**	**18**	**report**
MS11.2	design review of 65/130 nm run	11.3	18	report

Deliverables related to WP11	
D11.1: MPW 28 nm *The deliverable is a multi-project wafer fabrication with the different test ASICs in CMOS 28 nm*	24
D11.2: MPW 65/130 nm *The deliverable is a multi-project wafer fabrication with ASICs in CMOS 65 and/or 130 nm that can be used to readout detectors from the other WPs and in particular WP8*	24
D11.3: Measurement reports *Each of the ASIC fabricated in the 2 previous deliverables will have its design and performance documented in a report*	42

Summary

- Microelectronics is a key technology enabler for novel detectors
- 2 main pillars in AIDA INNOVA
  - Explore 28 nm technology performance for HEP
  - Provide readout ASICs in 130nm for other WPs
- 2 fabrications will occur in 2023 to match these objectives
  - Milestones MS45/46 and deliverables 11.2/11.3
- + Networking activity and sharing of expertise among participants
  - Several ASICs in co-design
- One industrial partner for technology transfer and spinoff