Advancement and Innovation for Detectors at Accelerators

WP6 Summary

Hybrid Pixel Sensors for 4D Tracking and Interconnection Technologies

WP6 Indico meetings: https://indico.cern.ch/category/13504/

Claudia Gemme, Anna Macchiolo
On behalf of the WP6 group

AIDAInnova Annual meeting
2023-04-26

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

WP6 Tasks and Task Leaders

- WP6 main deliverables:
  - Production of 3D and LGAD sensors both at FBK and CNM
    - Simulation to guide the design and interpret the results
    - Validation of sensors in laboratories and test beam
  - Develop interconnection techniques: Anisotropic Conductive Film (ACF) for single tiles, Wafer-to-Wafer for wafers

Objectives

Task 6.1. Coordination and Communication

See introductory section on page 29.

Task 6.2. Simulation and processing of common 3D and LGAD sensor productions

- Optimisation of processes for 3D and LGAD sensors for timing applications
- Simulations of various designs for 3D and LGAD sensors to compare and optimise the layout in terms of timing performance
- Simulations of surface and bulk radiation damage for 4D (tracking+timing) detectors toward more radiation tolerant solutions
- Processing of two common 3D sensor productions and two common LGAD productions by FBK/CNM
- Design and implementation of simulation software which is applicable to a large range of technologies and includes models for the description of effects from sensor level to readout electronics in semiconductor detectors

Task 6.3. Validation of common 3D and LGAD sensor productions

- Characterisation of the 3D sensors in terms of timing, radiation hardness, efficiency and uniformity via measurements in the laboratory and beam tests
- Characterisation of small pitch LGAD and inverse LGAD sensors (iLGADs) from the common production in terms of timing and efficiency via measurements in the laboratory and beam tests
- Feedback to the foundries for further process optimisation of 3D and LGAD sensors

Task 6.4. Development of interconnection technologies for future pixel detectors

- Development of suitable Anisotropic Conductive Films (ACF) material and die-to-die bonding process flows for small pixel pitches
- Production and post-processing of dedicated planar sensor wafers for ACF trials
- Test of the performance of sensor modules interconnected with ACF
- Production and test of ultra-thin assemblies interconnected with a wafer to wafer bonding technology
- Post-processing of sensor prototypes developed in Task 6.3

Task Leaders

T6.2
Gian Franco Dalla Betta
Giulio Pellegrini

T6.3
Gregor Kramberger
Ivan Vila

T6.4
Dominik Dannheim
Fabian Hügging

WP6 Milestones

Deliverable Number	Deliverable Title	Lead Beneficiary	Due Date (in months)	Means of verification
MS22	Wafer layout	FBK	18 ✅	Layout design file and report on the design choices, supported by simulations (Task 6.2)
MS23	Preliminary characterization of 3D and LGAD prototypes. Test set-up ready in the laboratories.	CSIC	23 **February 23**	Preliminary characterization on prototypes with the readout systems to be used with the final productions. (Task 6.3)
MS24	Completion of planar sensor productions for ACF	CNRS	18 ✅	Planar pixel sensor wafers delivered for interconnection tests (Task 6.4)
MS25	Availability of parts and definition of the technologies for wafer to wafer hybridization	UBONN	18 ✅	Wafers delivered to IZM and report on the technologies chosen for the interconnection (Task 6.4)

- MS23 Draft ready. After revision, by next week, it will be sent to the management.

WP6 Deliverables

Deliverable Number	Deliverable Title	Lead Beneficiary	Type	Dissemination level	Due Date (in months)	comments
D6.1	Completion of common productions	CSIC	Report	Public	30 Oct 2023	Including preliminary char. at foundries
D6.2	Final validation of timing performance of common productions	INFN	Report	Public	46	Before and after irradiations
D6.3	Test of the final ultra-thin hybrid assemblies from wafer to wafer bonding	Bonn	Report	Public	44	Module functionality, interconnection yield and strength
D6.4	Validation of the ACF for large and small pitch assemblies	CERN	Report	Public	45	Small pixel sizes from 25 to 55 μm

- First Deliverable D6.1 is coming soon, in October 2023.

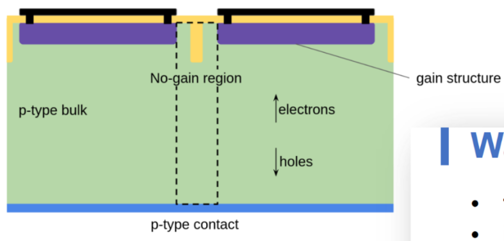
Task 6.2
Report from FBK

MS 22: M18 completed - wafer layouts
D6.1: due by Oct 2023 – completion of common production

Trench-Isolated LGAD (TI-LGAD) in FBK

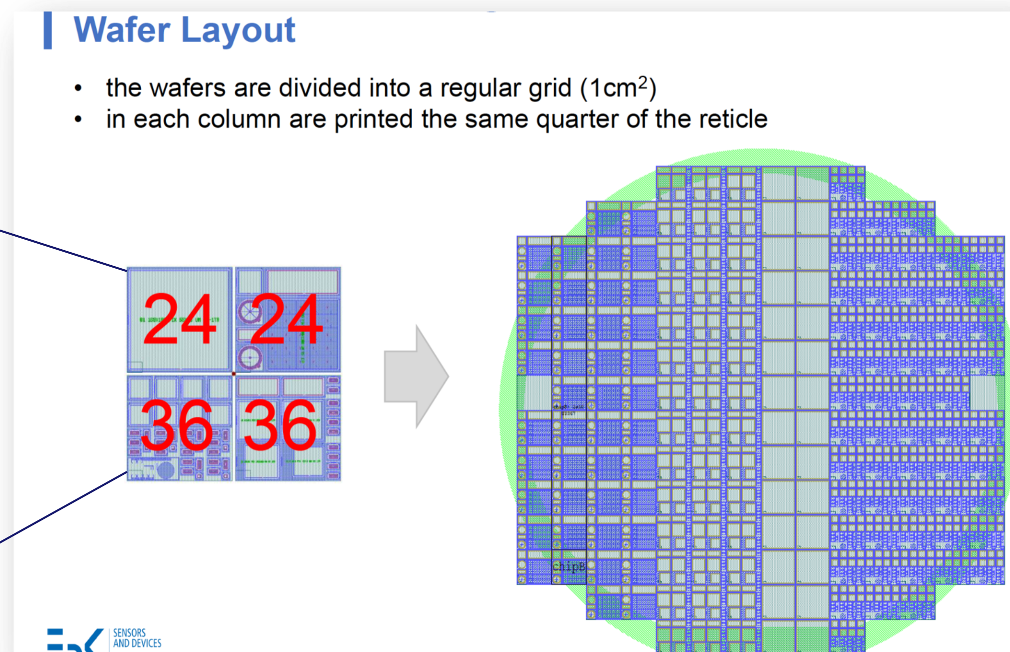
Giovanni Paternoster
Matteo Centis Vignali
Maurizio Boscardin

- ❑ The goal is to realize an LGAD compatible with small pitch (55micron or less) and with high fluences
  - ❑ Isolation made by trenches
  - ❑ Carbon co-implantation to increase radiationa hardness
- ❑ Previus exeperiece
  - ❑ Internal FBK batches
  - ❑ Batches in RD50



One full reticle (about 2x2 cm) in 4 quarter (about 1x1cm)
- Pixel & Strip
- PCM FBK
- 2x1 Test devices

In order to explore
- Pitch
- Border: 4 version
- Number of trenches : 1 or 2



Trench-Isolated LGAD (TI-LGAD) in FBK

Process

- **12 wafers**
- **Main process**
  - 45 µm, D2 , P2 and «high diffusion»

Split on

✓ Wafer thickness
✓ With or without carbon (it's the first time that we use carbon on TiLGAD)
✓ Trench Depth
✓ Trench Process

Note : two wafer per «main» split

Table splits

Wafer	Thickness	Carbon	Trench depth	Trench process
1	45	Y	D2	P2
2	45	Y	D2	P2
3	45	Y	D1	P2
4	45	Y	D1	P1
5	45	Y	D2	P1
6	45		D2	P2
7	45		D2	P2
8	45		D1	P1
9	55	Y	D3	P2
10	55	Y	D2	P2
11	55	Y	D2	P2
12	55		D2	P2

baseline ← (wafer 1)

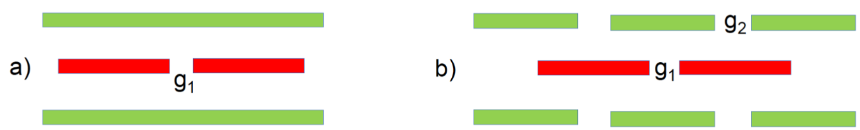
- Timescale:
  - 12 wafers, With and without carbon
  - Process in progress → To be completed in end September 2023

3D in FBK

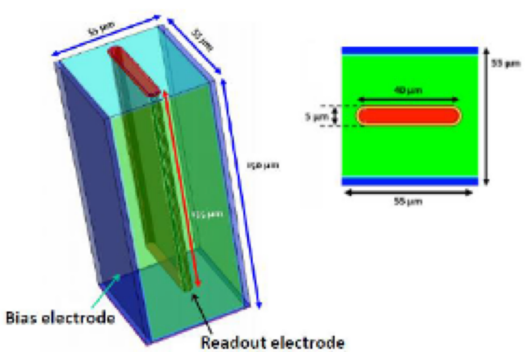
- Based on trench electrode
- Best performance for timing
- Develop in partnership with INFN Collaboration

Laura Parellada Monreal
Sabina Ronchin
Maurizio Boscardin
G.F Dalla Betta

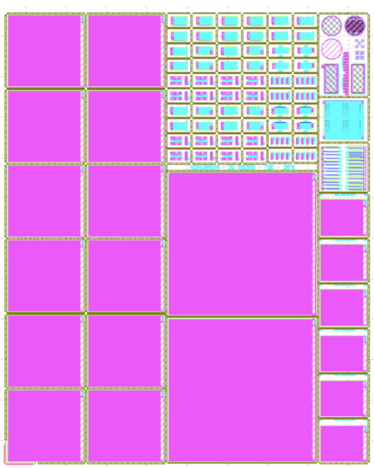
- 3D-trenched pixels only (no columns)
- Continuous ohmic trench (a) vs dashed ohmic trench (b)



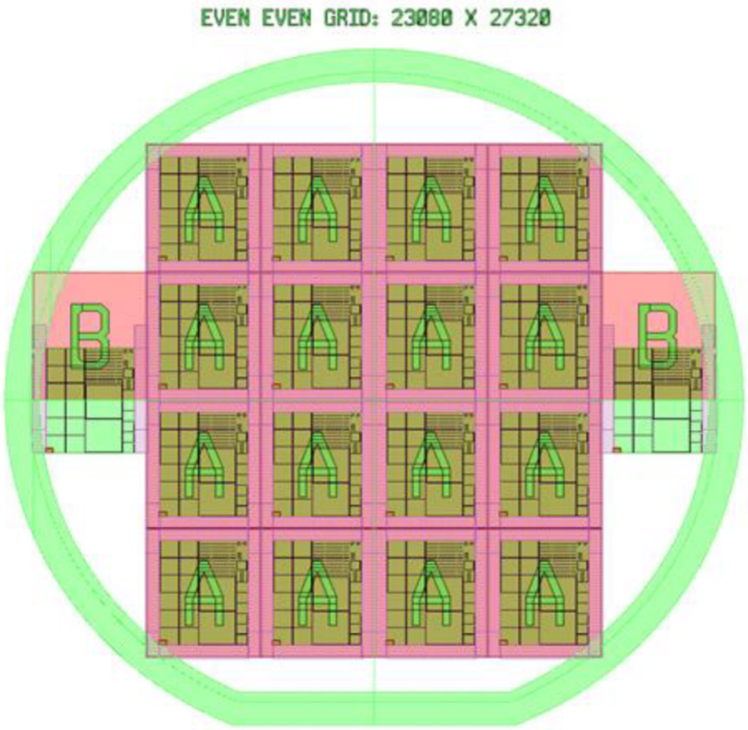
TimeSPoT

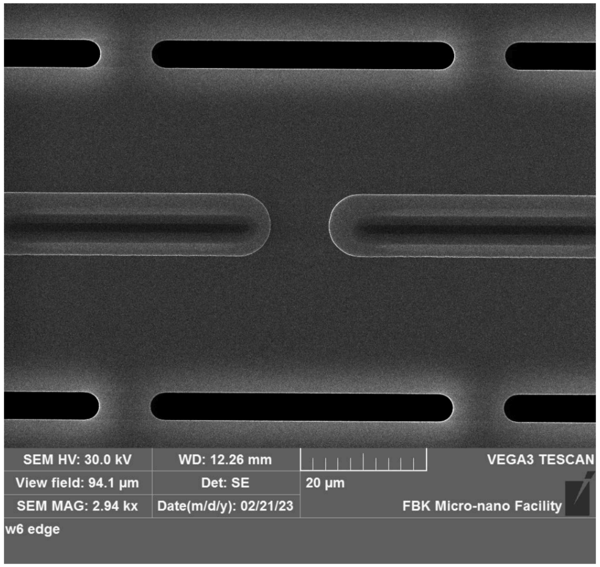


- **Pixel sensors (55 μm pitch)**
  - 32x32 pixels, multiplicity = 6 (3 std, 3 dashed)
  - 64x64 pixels, multiplicity = 12 (6 std, 6 dashed)
  - 128x128 pixels, multiplicity = 2 (1 std, 1 dashed)
- **Device test structures (55 μm pitch and 42 μm pitch, std and dashed)**
  - Groups of individual pixels
  - Strips
  - Diodes
- **Technological test structures**



3D in FBK





Trenches details
Check that the wafer bow is under control

- Timescale:
  - 12 wafers, 18 DIE on wafer
  - 3 wafers at p-hole filling: check the bow. 9 wafers ready to process: p-spray implanted
  - To be completed in end August 2023

Task 6.2
Report from CNM

MS 22: Due in M18, Completed - wafer layouts
D6.1: due by Oct 2023 – completion of common production
Slides *N. Moffat (CSIC)*

Current status of timing sensors runs at CNM

Run	Description	Clean Room Step
15543	150 mm **Timepix4 PiN**, Si (300 µm), 6PN1. **AidaInnova WP3**	Production completed (Waiting for UBM)
16020	150 mm **AC-LGAD**, Si (300 µm) and Si-Si (50/350 µm), 6LG4. **RD50**	Production completed (Waiting for UBM)
16069	100 mm **3D-DS Timing**, Si (285 µm), 240 µm depth columns, 10 µm columns diameter. **RD50**	Step 105/130 (Passivation Deposition)
16421	100mm **Timepix3 Trench iLGAD**, Epitaxial and Si-Si wafers, 4iLG3. **Engineering Run**. **RD50. AidaInnova WP6**	Step 16/65 (P+ Ohmic Contact Implantation, IBS France)
-	100mm **Timepix4 Trench iLGAD**, Epitaxial and Si-Si wafers, 4iLG3 **AidaInnova WP6**	Mask being drawn, Waiting for **TimeSpot1** Specifications

- AIDAinnova 3D run to be scheduled.

CNM third generation Inverse LGAD (iLGAD)

Run16421: **6 Wafers**, 100 mm, CNM1086 Mask Set

- **3 wafers**: **Epitaxial Wafers** (50/515 μm)
- **3 wafers**: **Si-Si Wafers** (50/350 μm)

TimePix3. 55x55 μm pitch, 256x256 pixels: **12 devices**

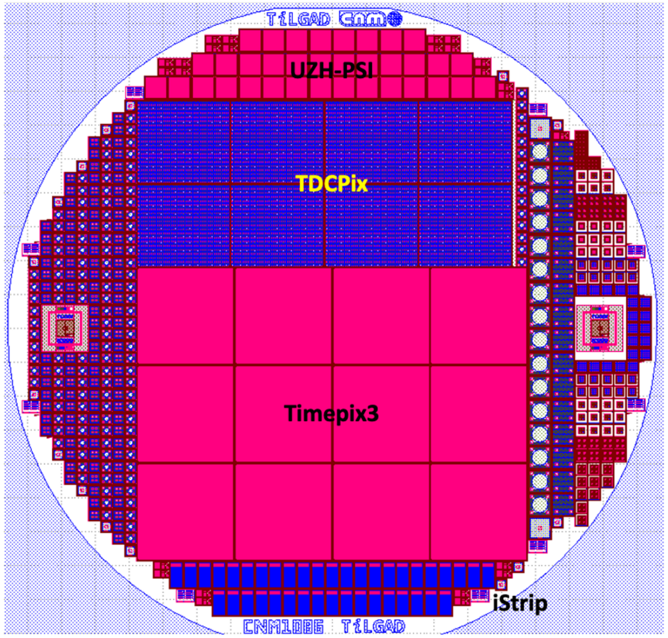
TDCPix. 300x300 μm pitch, 40x45 pixels: **8 devices**

UZH-PSI. 100x100 μm pitch, 30x30 pixels: **36 devices**

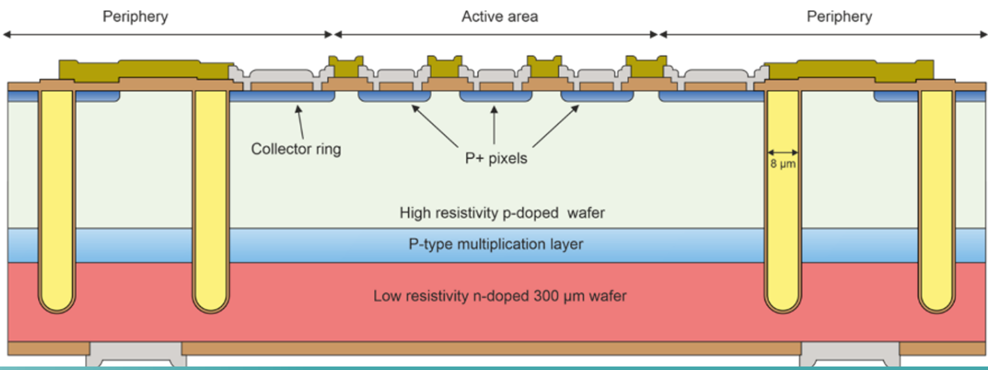
iStrip. 80 μm pitch, 20 strips: **40 devices**

Pad and Nikhef Test Devices to fill the gaps

Wafer Layout



Six months are needed for its Production and Electrical Characterization (**started in February**)



AIDAinnova WP6 CNM iLGAD production

RunXxxxx: **6 Wafers**, 100 mm, CNM1202 Mask Set

- **3 wafers**: **Epitaxial Wafers** (50/515 µm)
- **3 wafers**: **Si-Si Wafers** (50/350 µm)

TimePix4. 55x55 µm pitch, 448x512 pixels: **3 devices**

TimePix3. 55x55 µm pitch, 256x256 pixels: **6 devices**

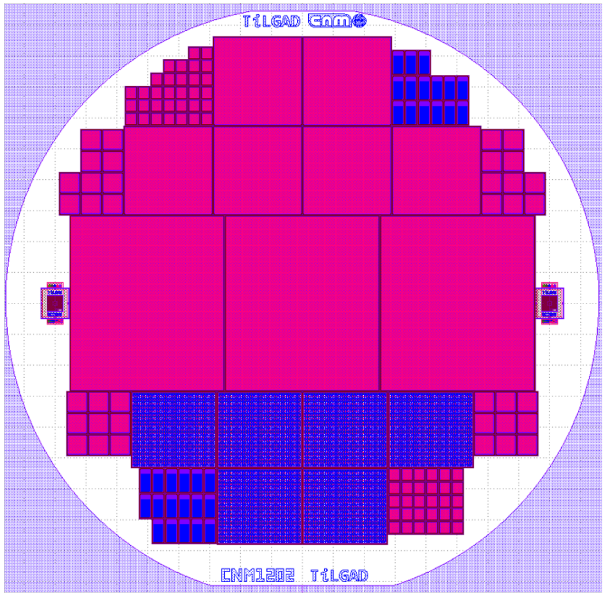
TDCPix. 300x300 µm pitch, 40x45 pixels: **6 devices**

TimeSpot1. 55x55 µm pitch, 32x32 pixels: **32+30 devices**

UZH-PSI. 100x100 µm pitch, 30x30 pixels: **20+18 devices**

iStrip. 80 µm pitch, 20 strips: **15+17 devices**

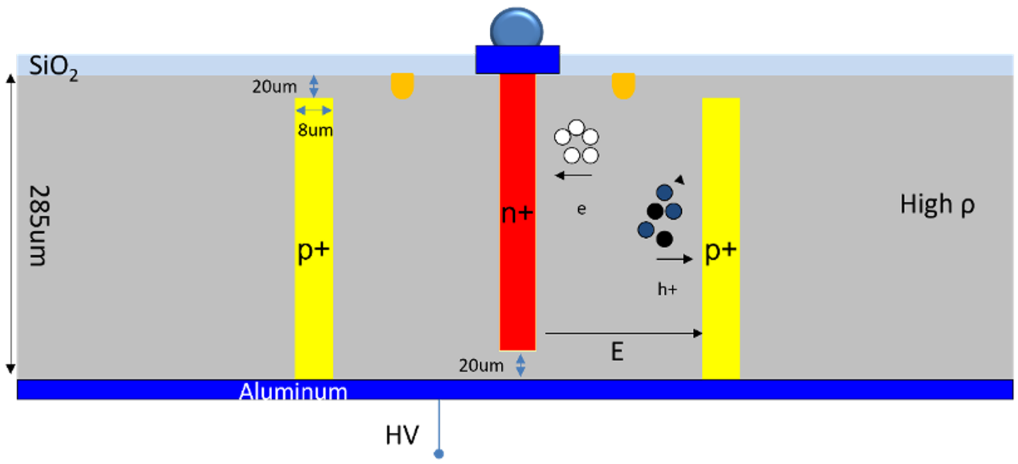
Pad and Nikhef Test Devices to fill the gaps



- Waiting for information on the floorplan of two read-out ASICs
- Six months are needed for production and electrical characterization

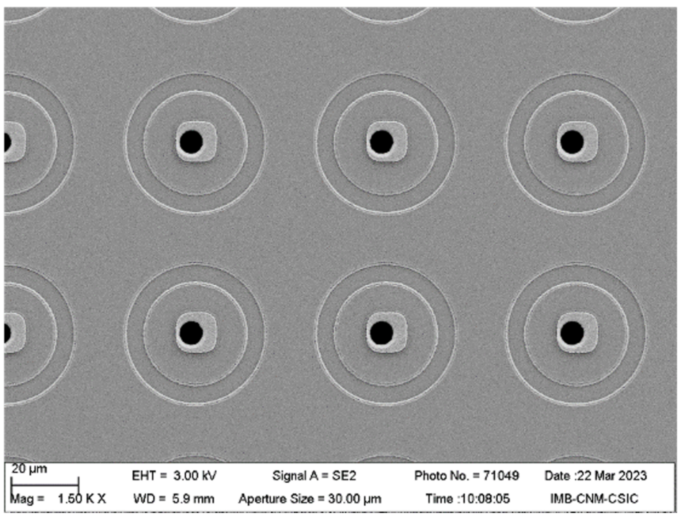
CNM 3D for timing

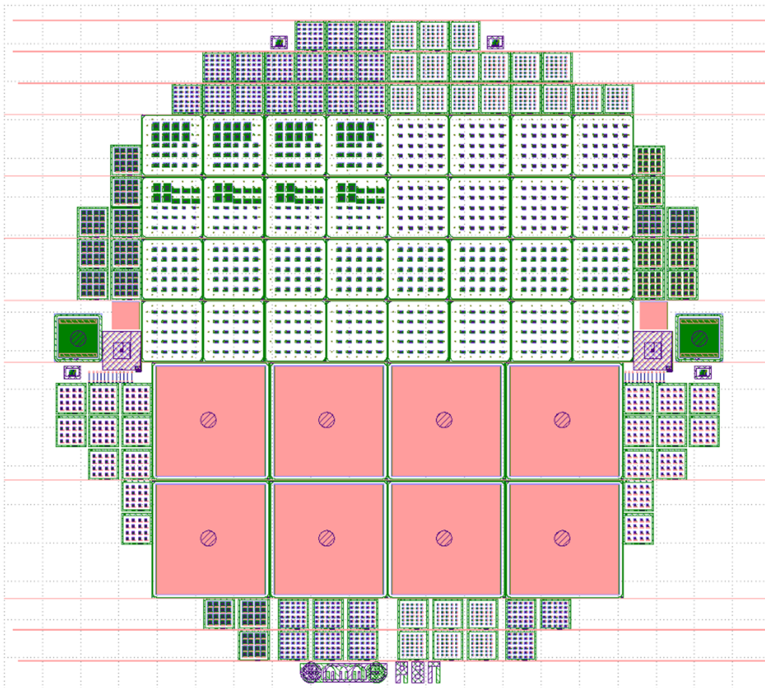
- Double sided technology,
- Wafer thickness : 285um +/-10um
- HRFZ silicon, p-type>5kOhm*cm
- P-stop isolation
- Holes diameter 8/10um
- Metal opening on the back



CNM 3D for timing: Ongoing run

Run16069: 3 **Wafers**, 100 mm, CNM987 Mask Set
Step 105/130
Medi**Pix3.** 55x55 μm pitch, 256x256 pixels: 8 **devices.**
Altiroc 1. 300x300 μm pitch, 40x45 pixels: 24 **devices.**
2 weeks are needed for to complete Production – Only requires the passivation layer.





Design of the AIDAinnova 3D production to be defined following the test of this on-going run

Task 6.2
Report from Simulation Studies

Slides *T. Croci,* F. Moscatelli, Passeri, A. Morozzi, P. Asenov, A. Fondacci, M. Menichelli, G.M. Bilei, V. Sola, M. Ferrero, J. Ye, A. Boughedda, G.-F. Dalla Betta

TCAD simulations of LGAD sensors

In collaboration with

INFN Torino : calibration/extension of the previously developed models by comparing the simulation findings with measurements carried out on different classes of LGAD detectors.

Comparison with experimental data, before and after irradiation (HPK2 production, by HPK).

"**PerugiaModDoping**"

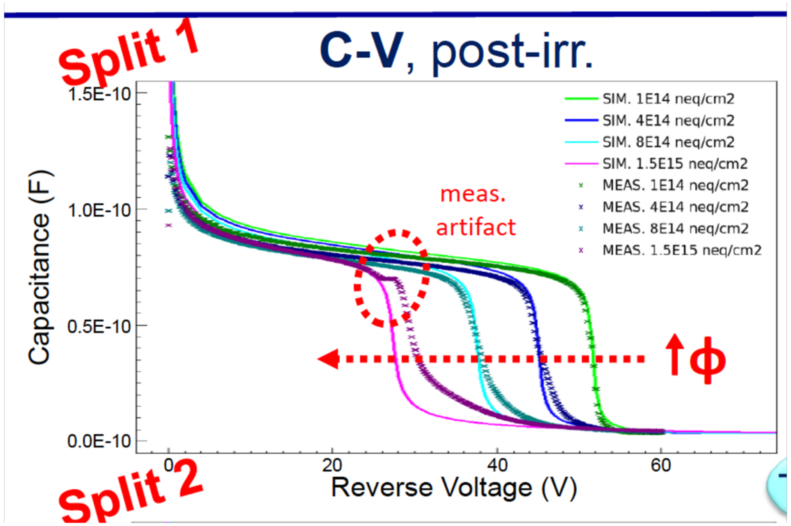
- **Torino analytical parameterization**
  - **Gain Layer** (Acceptor Removal)
  - **Bulk** (Acceptor Creation)
- "**Perugia0**" Bulk/Surface Radiation Damage Model

Surface damage (+ Q_{ox})

Type	Energy (eV)	Band width (eV)	Conc. (cm^{-2})
Acceptor	$E_C \leq E_T \leq E_C-0.56$	0.56	$D_{IT} = D_{IT}(\Phi)$
Donor	$E_V \leq E_T \leq E_V+0.6$	0.60	$D_{IT} = D_{IT}(\Phi)$

Bulk damage

Type	Energy (eV)	η (cm^{-1})	σ_n (cm^2)	σ_h (cm^2)
Donor	$E_C - 0.23$	0.006	2.3×10^{-14}	2.3×10^{-15}
Acceptor	$E_C - 0.42$	1.6	1×10^{-15}	1×10^{-14}
Acceptor	$E_C - 0.46$	0.9	7×10^{-14}	7×10^{-13}



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Acceptor	$E_C - 0.46$	0.9	7×10^{-14}	7×10^{-13}

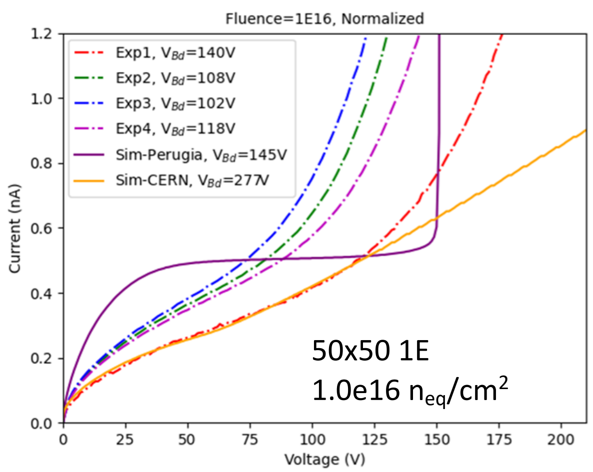
The new model has been verified for LGAD devices, by comparing TCAD simulations w/ measurements

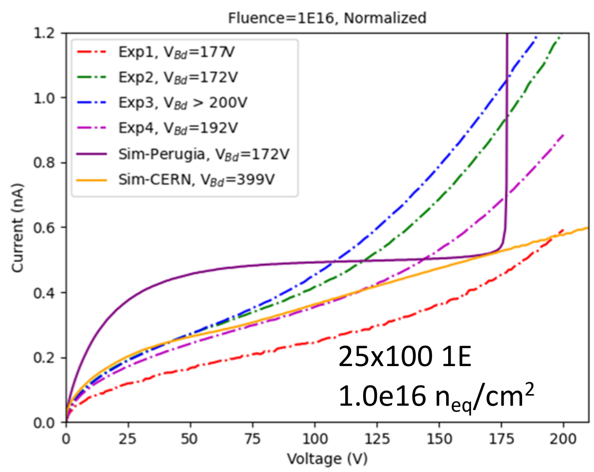
- UFSD2 production: static (DC), small signal (AC) and gain behavior well reproduced
- HPK2 production (DC and AC behavior well reproduced (but pay attention to the impact ionization model)
- To measure (β source) and to simulate gain behavior before and after irradiation

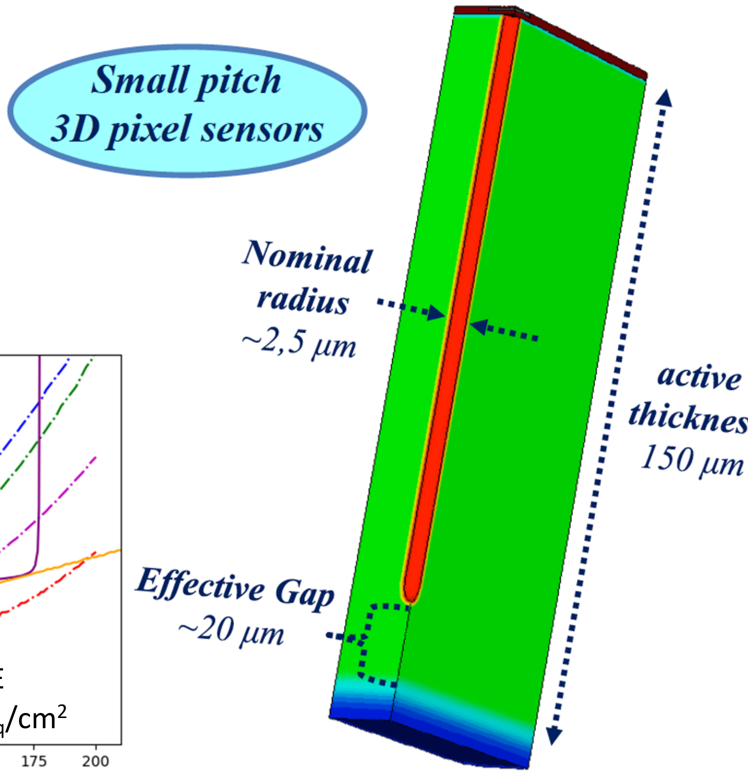
TCAD simulations of 3D sensors

- In collaboration with the University of Trento : validation of the previously developed model by comparing the simulation findings with measurements carried out on different classes of 3D detectors.
- Comparison with experimental data, before and after irradiation (FBK R&D, Batch 3)

- Perugia Bulk Damage Model can predict the breakdown quite accurately, despite the shape of the I V curves is quite different from the measured ones
- CERN Bulk Damage Model is better at predicting the leakage current, but largely overestimates the breakdown voltage







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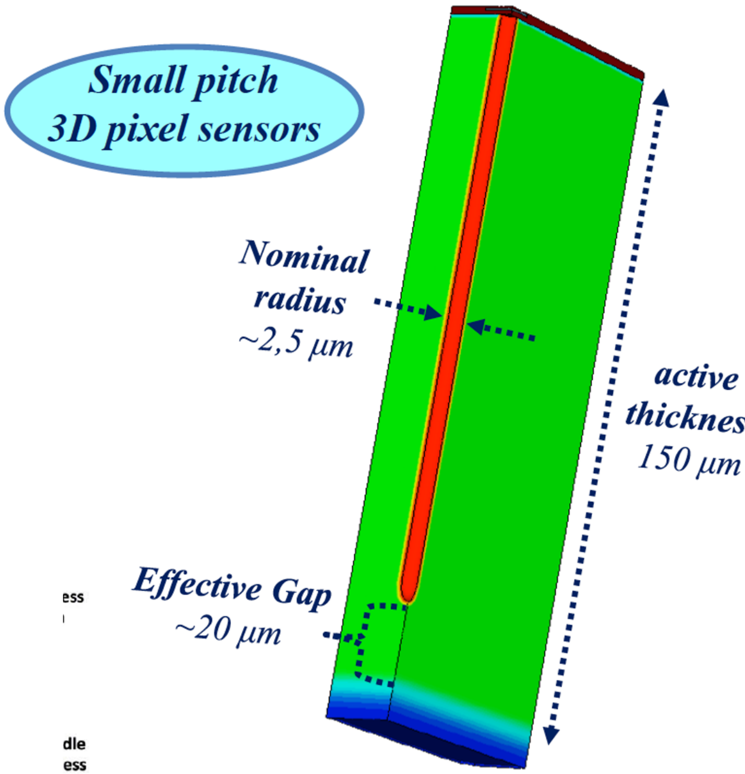
Validation of the new model *PerugiaModDoping* against the previous model:

measure DC behavior and laser response of 3D and trenched 3D detectors, before and after irradiation (up to the fluence of 2.5E16 n_eq/cm2)



Task 6.3
Validation and
Test beam organization

MS 23: validation on prototypes 3D and LGAD due in February, in preparation
Slides G. Kramberger, *Ivan Vial Alvarez*

Activity Recall and Related Milestones and Deliverables

Task 6.3. Validation of common 3D and LGAD sensor productions

- Characterisation of the **3D** sensors in terms of **timing, radiation hardness, efficiency and uniformity** via measurements in the laboratory and beam tests
- Characterisation of small pitch **LGAD** and inverse LGAD sensors (iLGADs) from the common production in terms of **timing and efficiency** via measurements in the laboratory and beam tests
- Feedback to the foundries for further process optimisation of 3D and LGAD sensors

MS & D #	Name	Due date (in months)
M23	Preliminary characterisation of 3D and LGAD prototypes.	23
D6.2	Final validation of timing performance of common productions	46

Final draft under review

Grant Agreement No: 101004761

AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

PRELIMINARY CHARACTERISATION OF 3D AND LGAD PROTOTYPES. TEST SET-UP READY IN THE LABORATORIES

MILESTONE: MS23

Document identifier:	AIDAinnova-MS23
Due date of milestone:	End of Month 23 (Mars 2023)
Report release date:	dd/10/2023
Work package:	WP6: [Hybrid pixels sensors for 4D Tracking and Interconnection Technologies]
Lead beneficiary:	[Short name of participant e.g. OEAW]
Document status:	Draft

Test beam preparation

- Test beam campaigns coordinated by Ivan and Gregor
  - At CERN two weeks from June 14th and one week from Aug 30th
  - One week at DESY in the second half of the year

- Community committed to support organization and provide devices.
  - Weekly meeting organized, https://indico.cern.ch/category/13504/
  - dedicated mailing list AIDAinnova-WP6-Test-beam-Preparation, link to subscribe

- Devices
  - TI-LGADs from UZH - more than 60 devices (small pad devices - compatible with CAEN was checked by UZH)
  - AC LGADs from CNM - all large pad devices (**CAEN digitizer**)
  - LGADs from CNM/FBK - (CMS/ATLAS design - compatible with CAEN digitizer)

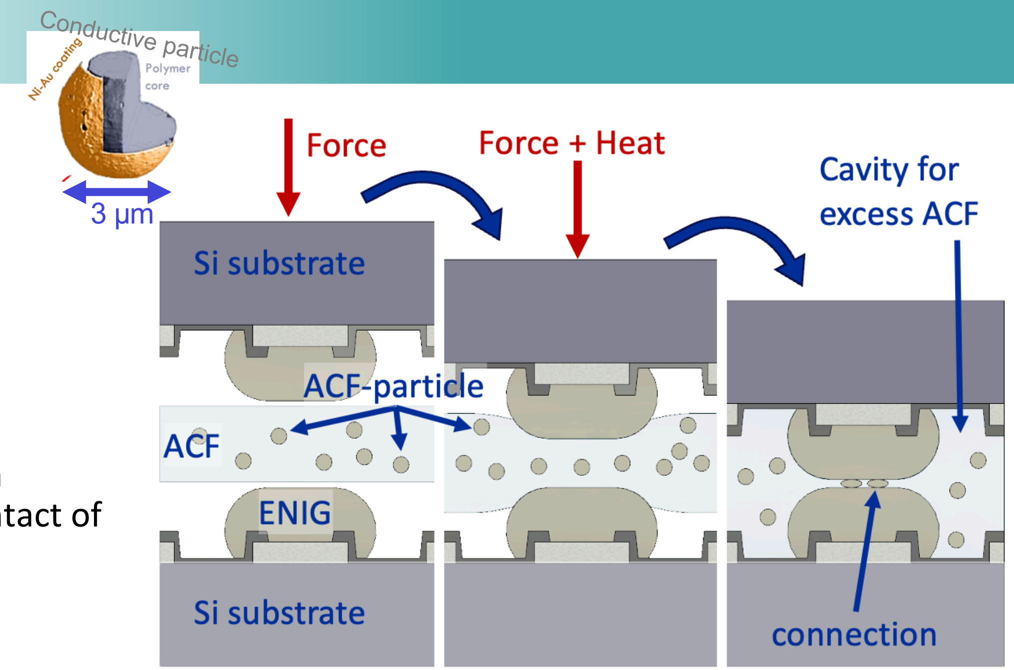
Task 6.4
Interconnections: ACF

MS 24: Due in M18, availability of sensors, Completed
Slides Giovanni Calderini (LPNHE), Dominik Dannheim (CERN), Rui de Oliveira (CERN), Janis Viktor Schmidt (CERN), Peter Svihra (CERN), Mateus Vicente (Univ. Geneva), Matteo Centis Vignali (FBK), Alexander Volker (CERN)

- **A**nisotropic **C**onductive **F**ilm/**P**aste (or **N**on-conductive)
  – **ACF/ACP** or **NCF/NCP**
  - Widely used for display production as strips

  → **Transfer to small pitch area application**
- Thermo-compression bonding process
  - Anisotropic / Vertical electrical connection via compressed conductive particles or direct contact of metal pads
  - Permanent mechanical bonding
- Specific topology

  → ENIG as Under Bump Metallisation (UBM)



Focus for this session

Preparation
- Electrical testing
- Visual inspection

ENIG (UBM)
- Nickel growth
- Pad topology

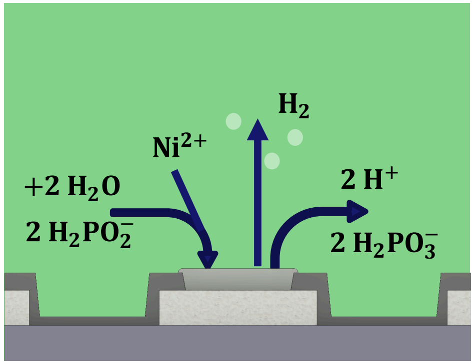
ACF bonding
- Lamination
- Flip-chip bonding

Testing
- Cross-section
- Electrical, source and Test-beam measurement

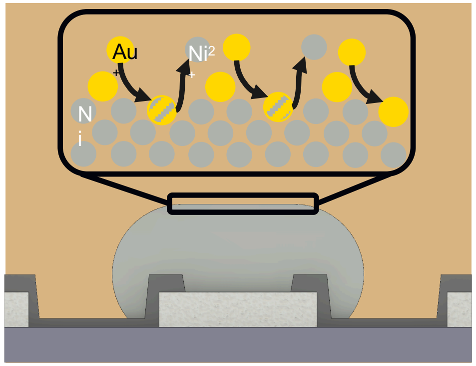
ENIG UBM plating need for increased height

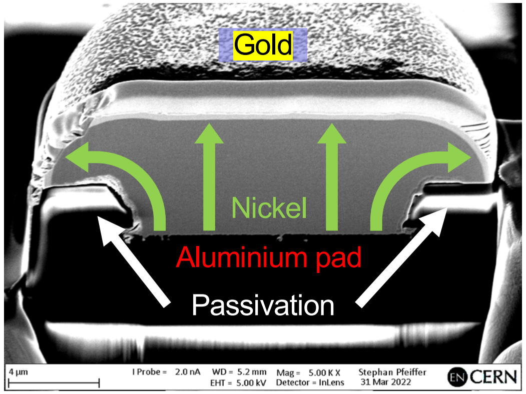
- Electroless Nickel
  - Self-catalytic reaction on pad surface
  - Performed on aluminium (activated surface)
    or on previous nickel deposits in a nickel bath
- Immersion Gold
  - Corrosion protection, very thin layer (< 1 µm)
- Ongoing optimisation of the process in EP-DT Micro-Pattern Technologies lab
  - Cleaning, oxide removal, nickel bath stability,…
  - Optimisation performed for different pad topologies

Electroless Nickel



Immersion Gold





ENIG UBM plating need for increased height

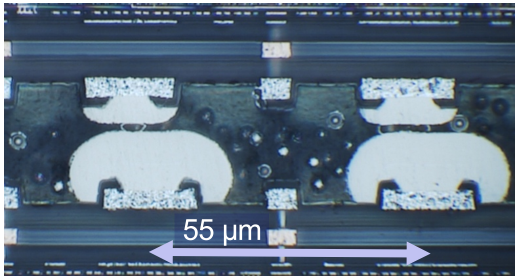
- Electroless Nickel
  - Self-cat…
  - P… su… or… ni…
- Imme…
  - Co… 1 µ…
- Ongoin… in EP-D… Techno…
  - Clea… stabil…
  - Optim… …ormed for different pad

Outlook for Improving the ENIG plating

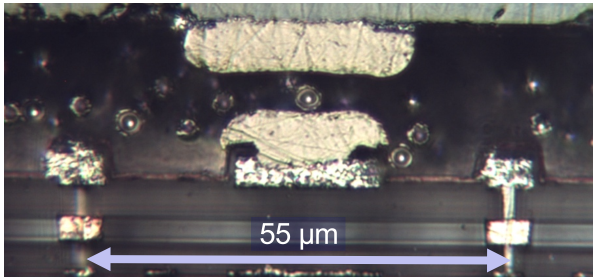
- Already very good yield for larger pads (above 80 µm pad size)
- Improvements of plating ongoing for smaller structures. Plating of 5 µm height uniform, higher still with unstable result
- Starting plating trials for CLICpix2 assemblies (25 µm pitch, real and daisy-chains)

- Cross-section

Cross-section Timepix3-Timepix3 ACF dummy sample

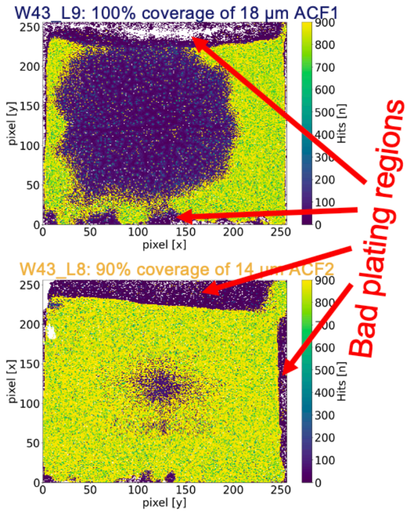


Cross-section Timepix3 ASCI-sensor ACF sample



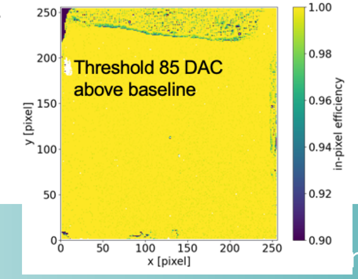
- Evaluation of plating height and different ACF materials using Sr90 exposure of electrical assemblies

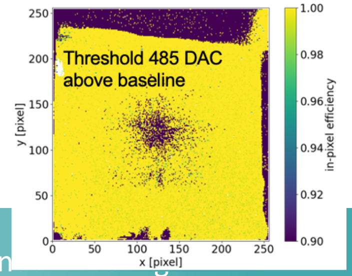
	Part. diameter [µm]	Thickness [µm]	Part. density [pcs/mm²]	Bonding pressure [Mpa]	Sheet/reel
ACF 1	3	18	71k	30-80	sheet
ACF 2	3	14	60k	50-90	reel



- Evaluation of in pixel efficiency at using 120 GeV pions:
  - at low threshold 99.96% in the "good" area 99.05% in the area with low plating
  - at higher thresholds Stable in the "good" area Fast drop in the area with low plating
  - Weak coupling in some areas

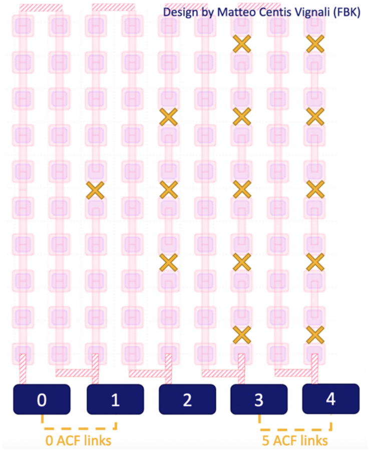
W43_L8 with 14 µm ACF2

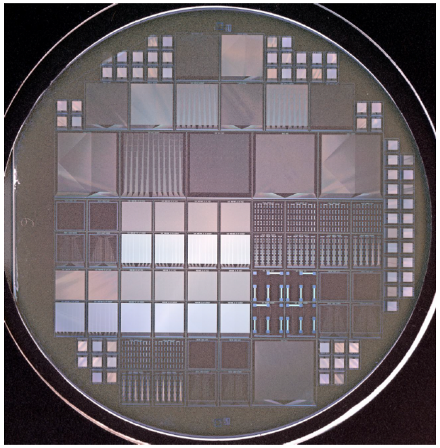




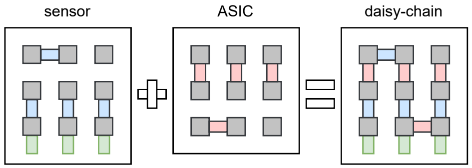
Daisy-chain devices Production

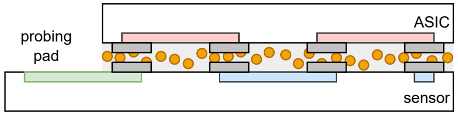
- Daisy-chain 6” quartz wafer with 625 µm thickness
  Designed and produced at FBK
- Study of ACF interconnection properties
  - Low-pitch and large-pitch reliability
  - Resistance measurements
  - Mechanical analysis
- Surface properties matched to ASICs
  - Al metal pads 2.5 µm thick
  - 950 nm thick passivation
- 4 out of 8 wafers at CERN (2 diced at FBK, 1 diced at CMi)





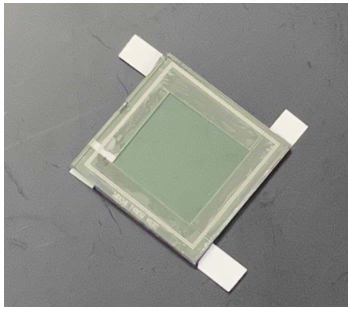
	pitch	size in mm	connections	per wafer	type	diceable
160x160 20um	20 um	3.2 x 3.2	25600	36	grid	no
CLICpix2	25 um	3.2 x 3.2	16384	34	grid	no
400x400 25um	25 um	20 x 20	640000	5	grid	yes
Timepix3	55 um	14 x 14	65536	4	grid	no
Timepix3 islands	55 um	14 x 14	65536	4	grid	no
RD53	50 um	20 x 20	160000	4	grid	no
RD53 islands	50 um	20 x 20	160000	2	grid	no
70x70 140um	140 um	20 x 20	2112	3	peripheral	yes
10x10 1000um	1000 um	20 x 20	400	3	grid	yes
3x3 4500um	4500 um	20 x 20	36	1	grid	yes



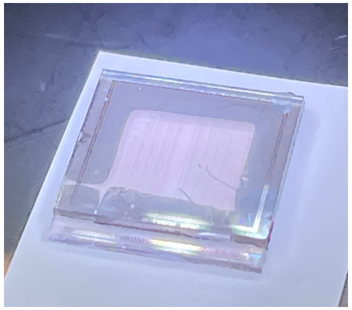


Daisy-chain devices Testing

lamination



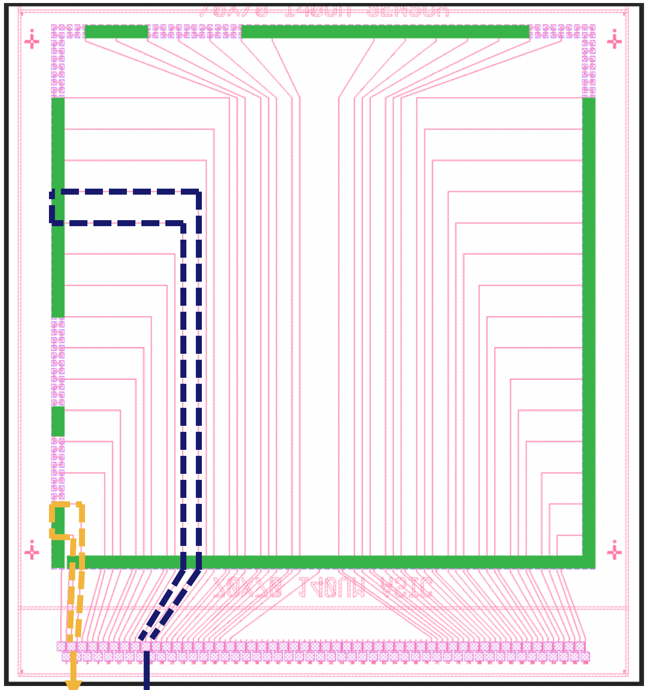
bonded



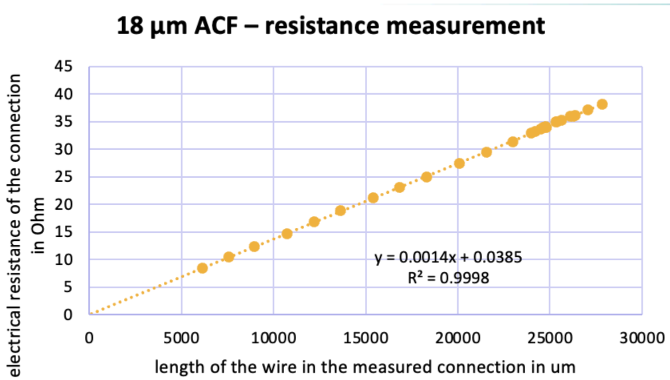
	Part. diameter [μm]	Thickness [μm]	Part. density [pcs/mm^2]	Bonding pressure [Mpa]	Sheet/reel
ACF 1	3	18	71k	30-80	sheet
ACF 2	3	14	60k	50-90	reel

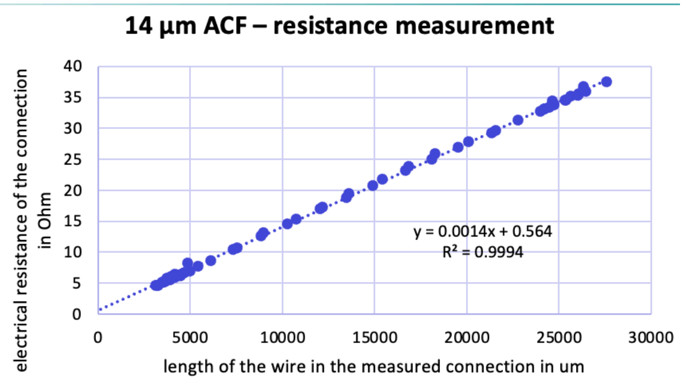
- Bonding peripheral-type device
  - Used sheet and 2 mm ACF film (18 μm / 14 μm thickness)
  - pad area 7744 μm^2
- Good connection yield
  - Missing connections due to ACF lamination / mechanical damage
  - 2-wire measurement of resistivity, dominated by metal line length

Verified connections



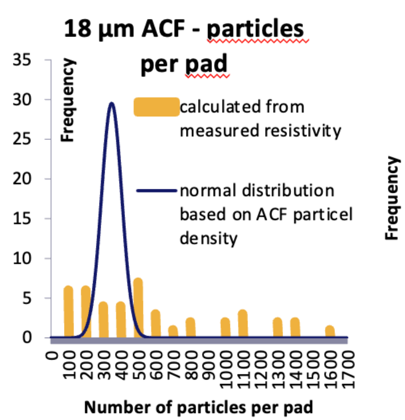
Daisy-chain devices Testing

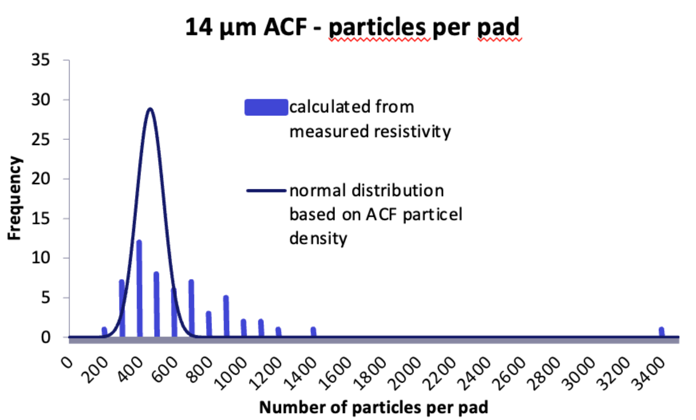




- **Linear offset (0.564 ± 0.075) Ω from 14 µm ACF**
- On average 8.7 connections in single chain
  => (0.065 ± 0.009) Ω per connection
- (60000 ± 10000) part. per mm^2
  => (464 ± 77) part. per connection
- **Single particle resistance**
  R = (30.2 ± 6.5) Ω

Identical calculation for 18 µm ACF

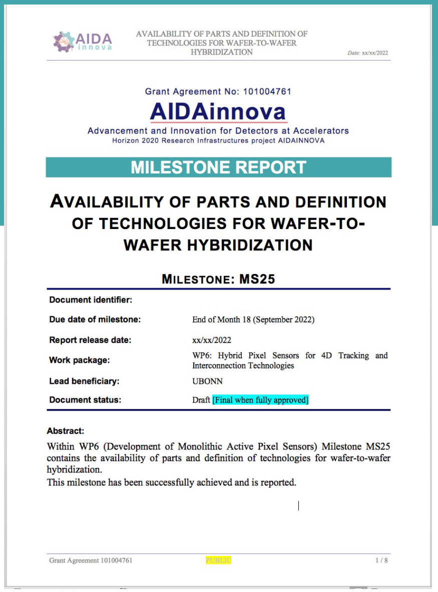




- **Based on calculated single particle resistance, recalculated number of particles per single connection**
  -> circular definition, but ballpark good enough to observe difference across the assembly

Outlook

- Studies of mechanical and electrical performance using daisy-chains
  Good resistivity results, need to investigate impact of temperature/humidity/radiation
- Further evaluation and improvement of bonding parameters
  e.g. Plating height, particle density, ACF thickness, ACF coverage


AVAILABILITY OF PARTS AND DEFINITION OF TECHNOLOGIES FOR WAFER-TO-WAFER HYBRIDIZATION

Date: xx/xx/2022

Grant Agreement No: 101004761

AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

AVAILABILITY OF PARTS AND DEFINITION OF TECHNOLOGIES FOR WAFER-TO-WAFER HYBRIDIZATION

MILESTONE: MS25

Document identifier:	
Due date of milestone:	End of Month 18 (September 2022)
Report release date:	xx/xx/2022
Work package:	WP6: Hybrid Pixel Sensors for 4D Tracking and Interconnection Technologies
Lead beneficiary:	UBONN
Document status:	Draft [Final when fully approved]

Abstract:

Within WP6 (Development of Monolithic Active Pixel Sensors) Milestone MS25 contains the availability of parts and definition of technologies for wafer-to-wafer hybridization.

This milestone has been successfully achieved and is reported.

Grant Agreement 101004761 PUBLIC 1 / 8

Task 6.4
Interconnections: Wafer-to-Wafer

MS 25: Due in M18, availability of parts, Completed - wafer layouts

D6.1: due by Oct 2023 – completion of common production

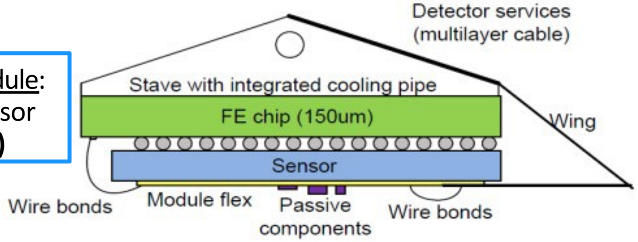
Slides F. Huegging, Y. Dieter, S. Zhang (Bonn), I. Gregor (DESY&Bonn), T. Fritzsch (IZM)

Thin hybrid pixel detectors with W2W

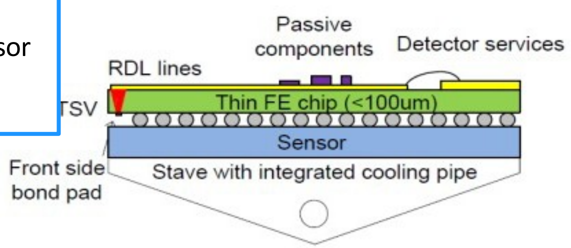
Interconnection technique aiming to keep the module hybrid approach, but allow to move to ultra-thin modules: *~20um pixel FE on 200 (300) mm CMOS and 50-100 um pixel sensors on 200 (300) mm CMOS sensors.*

- Separate development and optimization of sensors and FE electronics allowing for best performance of FE electronic and sensor.
- Fine pitch interconnection between FE and sensor pixel with a pitch down to ~20µm.
- Thinning of FE and sensor parts to the minimum.
- Can benefit from active CMOS sensor development by integrating some electronic already into the sensor

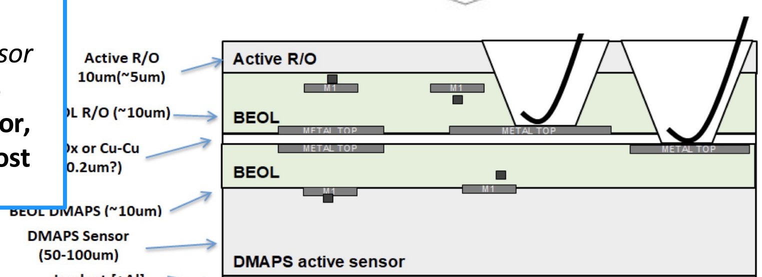
Standard hybrid pixel module:
150 µm FE & 150 µm sensor
2013 (ATLAS IBL & ITk)



TSV hybrid pixel module:
80 -100 µm FE & 150 µm sensor
2019 (AIDA 2020 proof of concept)



Ultra thin hybrid pixel module:
~20 µm FE &
50 -100 µm sensor
2025 (future tracking detector, esp. in innermost layers)



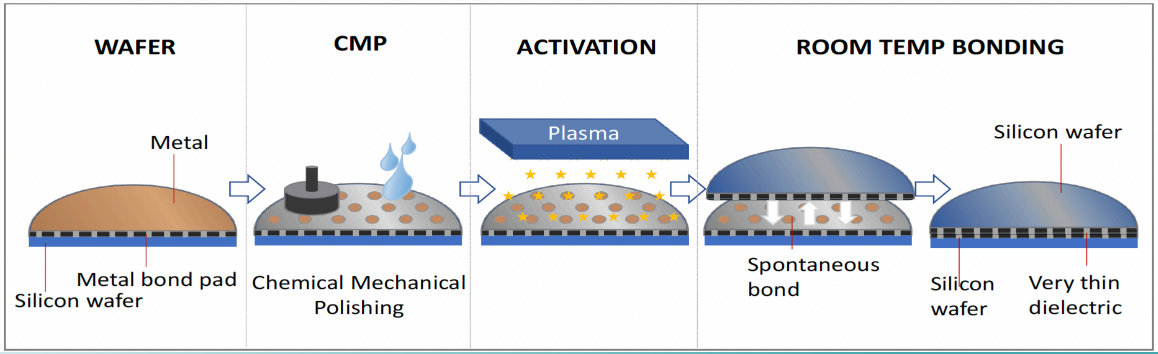
Thin hybrid pixel detectors with W2W

Slides: F. Huegging, Y. Dieter, S. Zhang (Bonn), I. Gregor (DESY&Bonn), T. Fritzsch (IZM)

Interconnection technique aiming to keep the module hybrid approach, but allow to move to ultra-thin modules: *~20um pixel FE on 200 (300) mm CMOS and 50-100 um pixel sensors on 200 (300) mm CMOS sensors.*

Technologies involved:

- Wafer-to-Wafer bonding between R/O and sensor wafer
- Thinning and backside processing of bonded wafer-wafer assembly:
  - Thinning on wafer level is easy, but might need backside process of the sensor backside, i.e. backside implantation and metallization
- Opening and connection to the R/O chip pads (I/0 and power) from the backside after thinning:
  - similar to the TSV pixel module project already demonstrated during AIDA-2020.

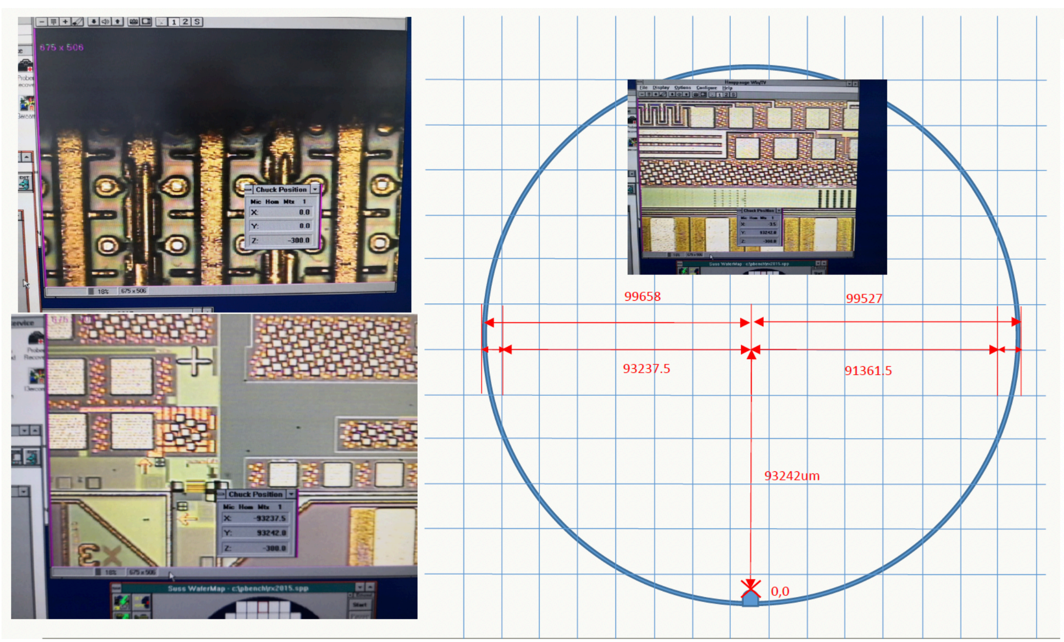


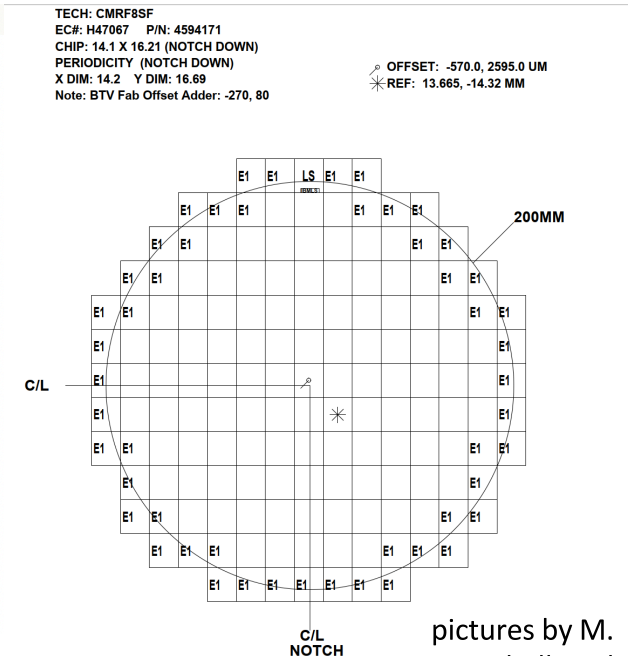
W2W in AIDAinnova

- **Parts for the proof of concept**:
  - Develop dedicated CMOS Sensor wafer compatible with a pixel FE chip wafer. Starting point: passive CMOS sensor development on 200 mm wafer with 110/150 nm process node from Lfoundry
  - Decided to use TimePix3 chip wafers (GF 130 nm on 200 mm wafers)
  - [initial idea was to have own FE development on the same wafer as the sensor, now backup option]
- Developing and optimization of **hybridization process** including thinning and interconnection from chip's backside at IZM.
  - Includes design and fabrication of development wafers (Dummy chains)
- Longer Term (beyond AIDAinnova): **Transfer process to more modern feature** size pixel chips (65nm or 28 nm on 300 mm wafers) for smaller pixel pitches and faster electronics

Proof of concept parts: the FE wafers

- TimePix3 wafers are at IZM they have been checked to be compatible with W2W bonding:
  - Several wafers have been measured to confirm the reticule stepping is the same for all wafers
  - Wafer topography have been checked in detail by IZM and TimePix collaboration

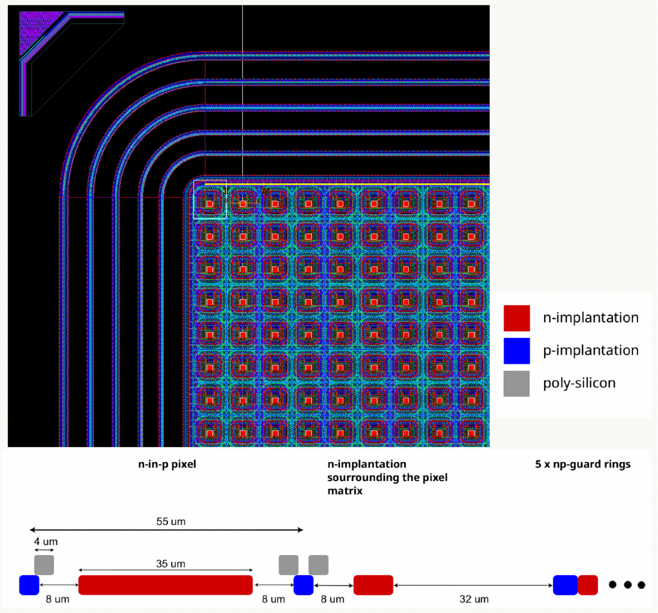


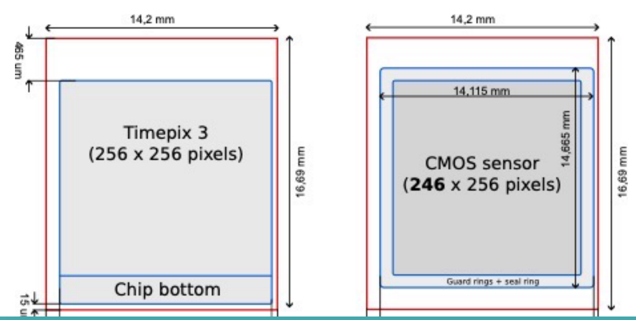


pictures by M. Campbell et al.

Proof of concept parts: the sensor wafers

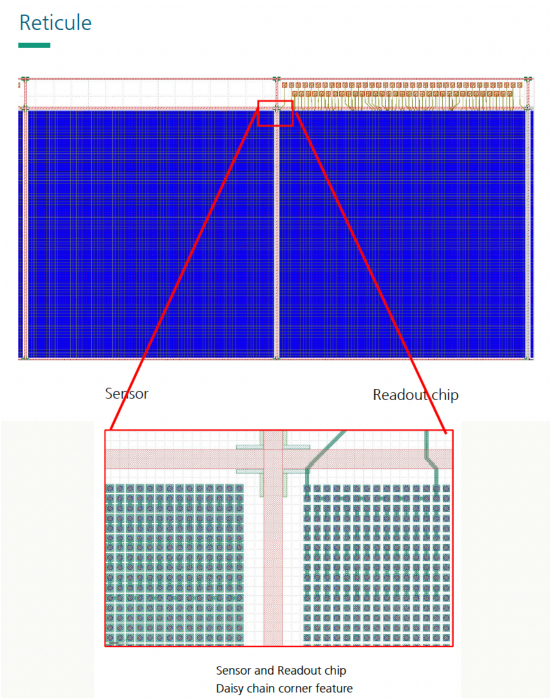
- Sensor layout is derived from former passive CMOS sensor with changes to fit the TimePix3 readout
  - Increase n-implant width from 30 um to 35 um in order to match 55 x 55 pixel
  - CMOS sensor has to fit into same reticule as TimePix3 chip
    - use only 246 pixels in horizontal axis, instead of 256. Smaller sensor pixel matrix is not a problem for sensor or TimePix chip
  - Few things still to be defined:
    - TSV etching through TimePix3 chip such that chip pads are accessible from chip backside
    - Sensor backside HV contact requires the usage of fully processed sensors incl. thinning, backside implantation and metallization for the W2W bonding process
  - Status:
    - Design ready only a few design rule checks missing.
    - Discussion with foundry about quote and details of the submission → Production to start soon.

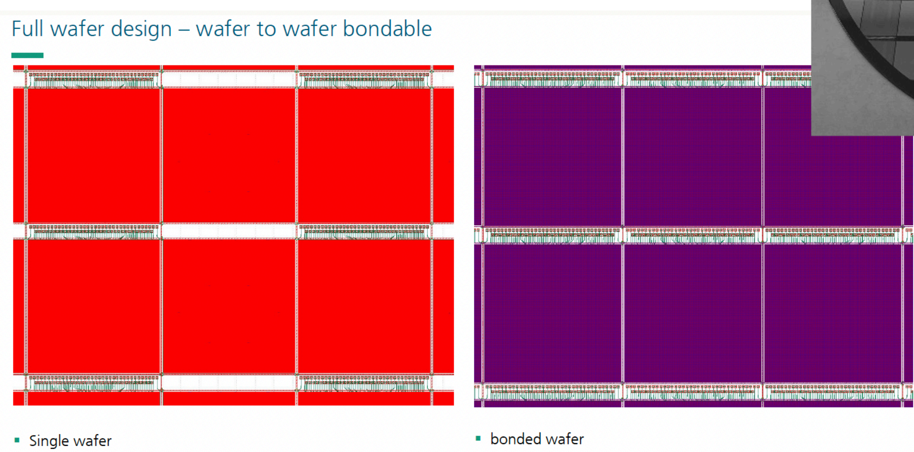


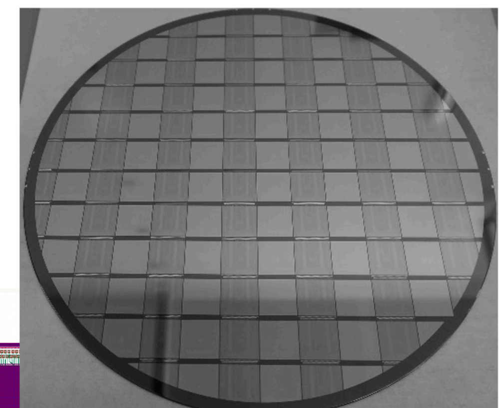


Hybridization Process @IZM: development wafers

- Work plan well defined at IZM includes the design and fabrication of so-called development wafers, hosting dummy chains to test the process.
  - Design input: MEDIPIX adapted test design used for Indium bump bonding process development
  - Wafers in hands, allowed to have the project Milestone approved in late 2022.

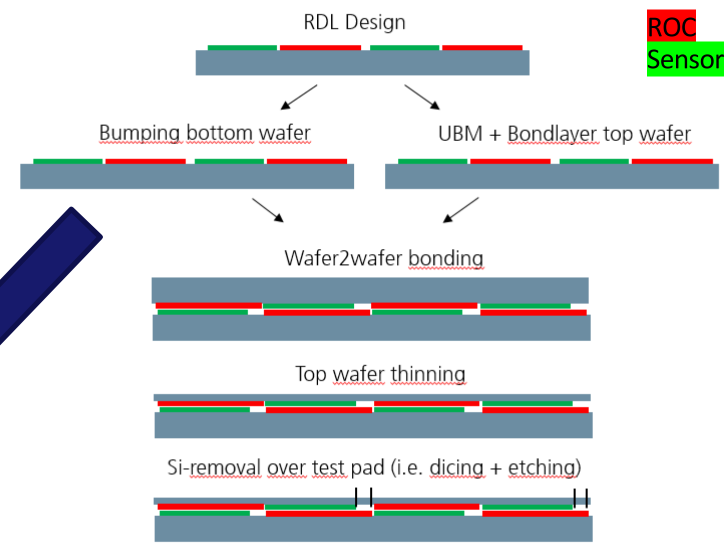


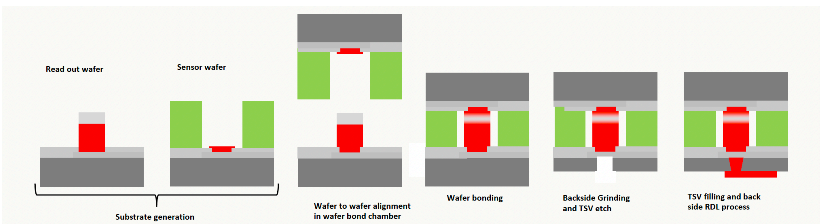


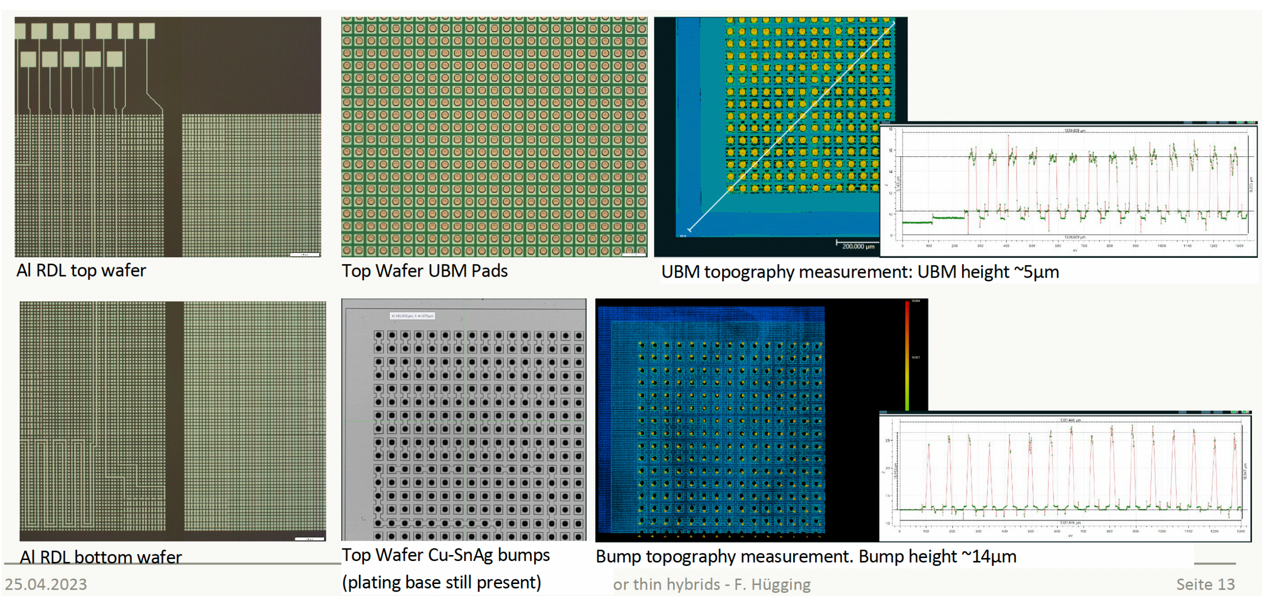


Hybridization Process @IZM: process flow

- The Cu/Sn wafer bonding is a well established process. The Cu/Sn bond will be supported by spin coated, photo-structured polymer layer which is joined simultaneously
- Depending on total wafer stack thickness a mechanical support during TSV formation and backside RDL process will be required







Al RDL top wafer

Top Wafer UBM Pads

UBM topography measurement: UBM height ~5µm

Al RDL bottom wafer

Top Wafer Cu-SnAg bumps (plating base still present)

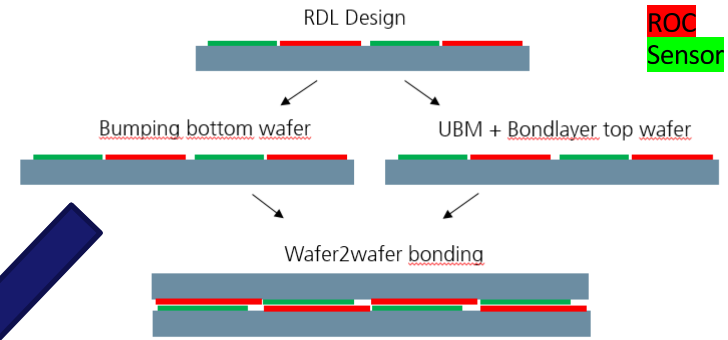
Bump topography measurement. Bump height ~14µm

Current status:

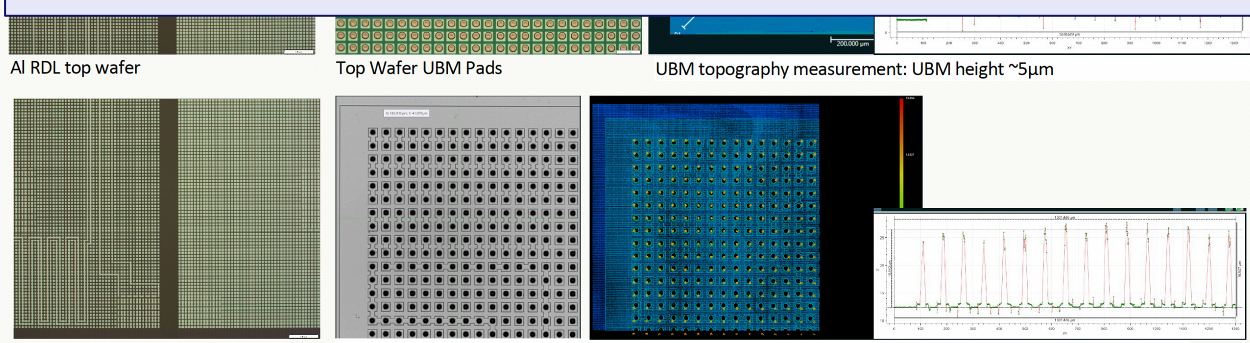
- Top wafer UBM metallization finished + topography scan ongoing
- Bottom wafer in pillar bumping process
- Polymer material screening as material which was intended to use is not available anymore (R&D stopped) → 2 alternative polymer materials identified which are currently under test

Hybridization Process @IZM: process flow

- The Cu/Sn wafer bonding is a well established process. The Cu/Sn bond will be supported by spin coated, photo-structured polymer layer which is joined simultaneously
- Depending on total wafer stack thickness a mechanical support during TSV formation and backside RDL process will be required



- Overall Status/Timescale:
  - W2W technology definition is completed, process developments wafers in hand, process development at IZM is ongoing and should be completed in ~ 1 year.
  - Real parts: readout wafers in hand, sensor design almost completed, production to start soon: needed in 9-12 months (but should be available in late 2023).
  - Task Deliverable due by Dec 2024.



Al RDL top wafer | Top Wafer UBM Pads | UBM topography measurement: UBM height ~5µm

Al RDL bottom wafer | Top Wafer Cu-SnAg bumps (plating base still present) | Bump topography measurement. Bump height ~14µm

- Bottom wafer in pillar bumping process
- Polymer material screening as material which was intended to use is not available anymore (R&D stopped) → 2 alternative polymer materials identified which are currently under test

- Thank you for your attention!