

WP3: Test beam and DAQ infrastructure

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- **Task 3.1 Coordination and Communication (M. Stanitzki & M. Wing)**
- **Task 3.2 Upgrading the EUDET-style beam telescope infrastructure (A. Herkert)**
 - Upgrade of the EUDET-style beam reference telescopes with the more recent ALPIDE sensor
 - Integration of new AIDAinnova next generation sensors into current telescopes
 - Development of a common cold-box for test-beam facilities
- **Task 3.3 Sub-ns timing capabilities for the EUDET-style telescopes (M. van Beuzekom & D. Cussans)**
 - Integration of a TimePix4 plane into EUDAQ2
 - Picosecond timing support in the AIDA trigger logic unit (TLU)
 - Include a plane based on low gain avalanche detectors (LGAD) in the EUDET-style telescopes
- **Task 3.4 Development of DAQ software for next generation beam tests (L. Huth)**
 - Development of EUDAQ2 software to support picosecond timing of next generation sensors
 - Development of versatile online monitoring for EUDAQ2
- **Task 3.5 Development of common DAQ hardware (D. Dannheim)**
 - Development of a Caribou-based common readout board to support sensor R&D
 - Development of the VMM3 common readout board to support gas detector R&D

Milestones and Deliverables

MS #	Milestone name	Lead beneficiary	Due Date (in months)	Means of verification
MS8	Telescopes upgraded with ALPIDE sensor	12 - DESY	27	New telescope in test-beam facilities (Task 3.2)
MS9	Timepix4 timing layer in telescopes	23 - NWO-I/Nikhef	36	Upgraded telescope in all beamlines (Task 3.3)
MS10	Monitoring software developed	39 - UCL	30	Use in beam tests (Task 3.4)
MS11	Common readout boards designed	1 - CERN	23	Prototype developed (Task 3.5)
D #	Deliverable name	Lead beneficiary	Type	Due Date (in months)
D3.1	Common cold box delivered	1 - CERN	Report	30
D3.2	New TLU produced	38 - UNIVBRIS	Demonstrator	39
D3.3	Telescopes upgraded with new layers	12 - DESY	Demonstrator	46
D3.4	New software developments available for use	39 - UCL	Report	39
D3.5	Common readout boards delivered	1 - CERN	Report	42

ALPIDE based telescope upgrade status:

- All legal and administrative steps completed:
 - Import license at hand
 - ALICE agreed on providing sensors, 30 prepared
- First sensors for prototyping at DESY
- Could already provide an ALPIDE telescope to users
 - Transparent EUDAQ2 integration
 - Based on single sensor SoC boards
- 2nd generation of telescope under development
 - Cost-conscious design, single based SoC for all layers, designed at DESY, long term support
 - MS8 (M27) can only be partially fulfilled

ALPIDE (MIMOSA) telescope

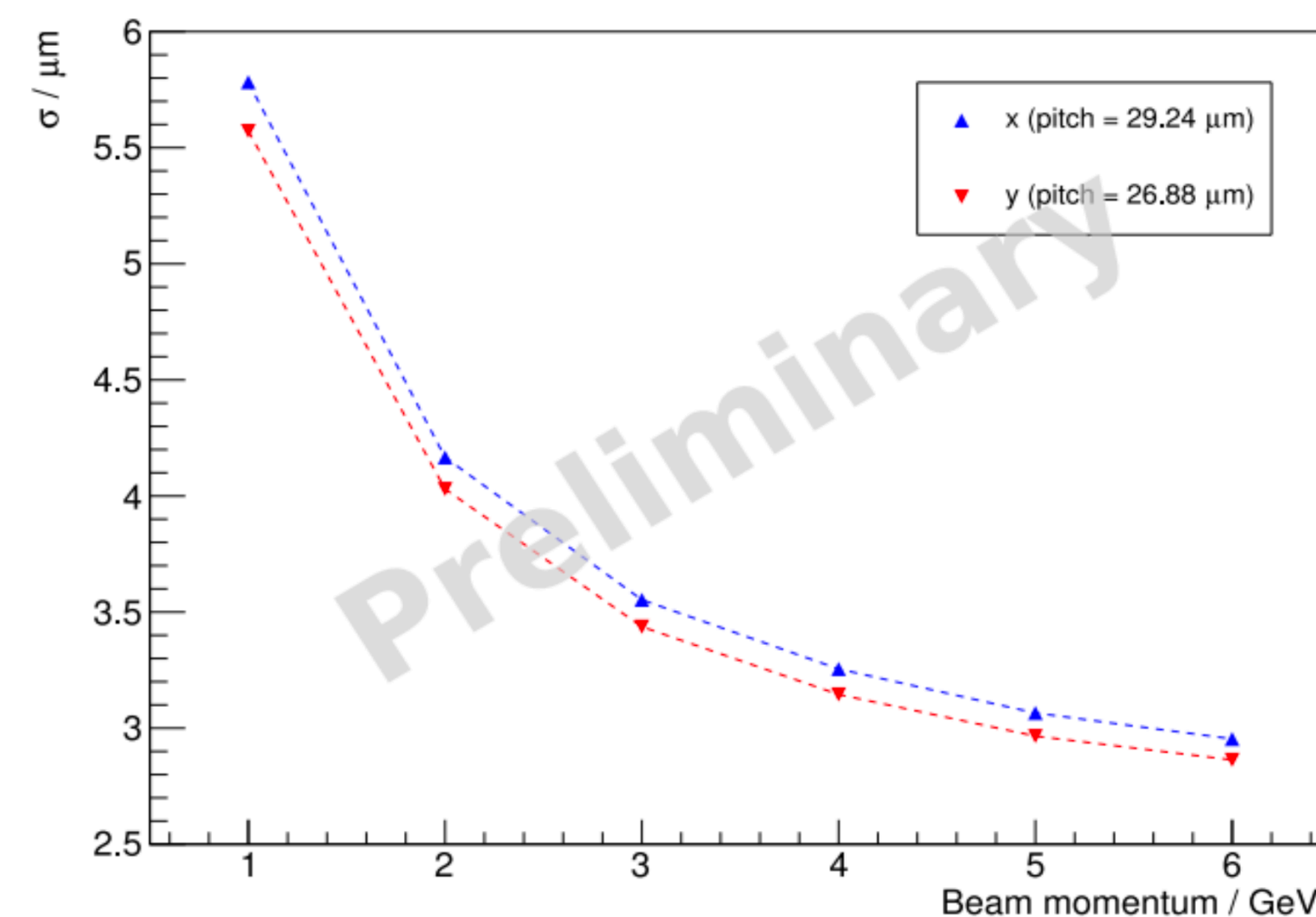
10k (~1.5k) triggers/s with single tracks

35k (~1.5k) triggers/s

10 μ s (~230 μ s) integration time

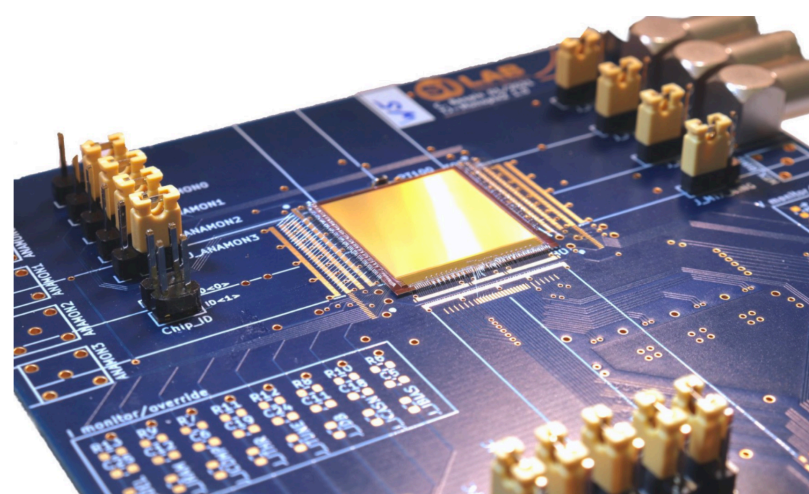
~3 μ m (~2 μ m) spatial resolution

Track resolution at DUT position

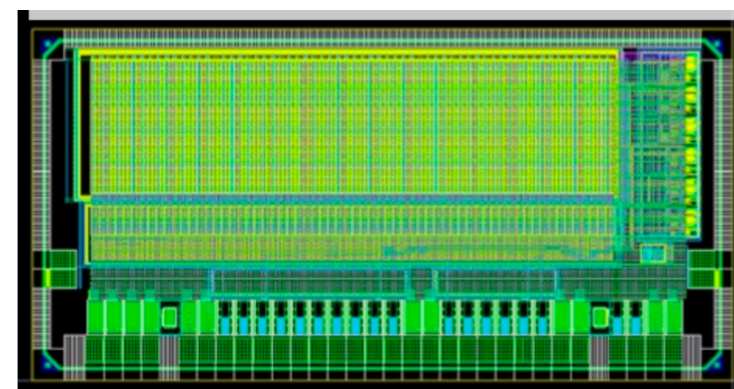


Telescope with next generation pixel sensors

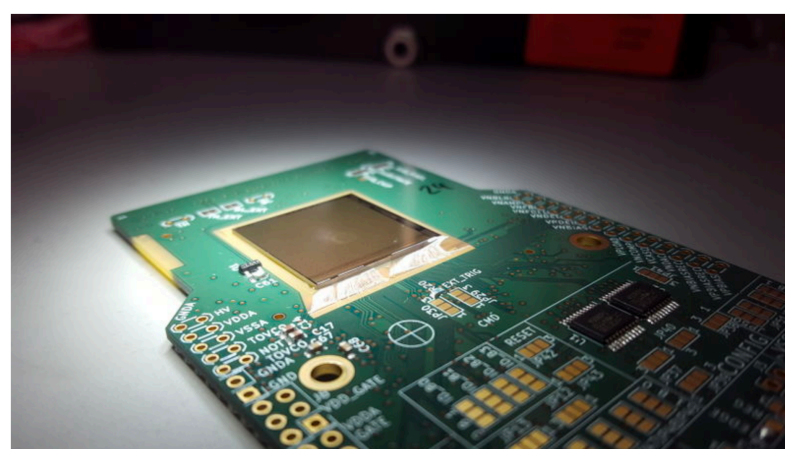
- Potential candidates from
 - WP5
 - 65nm developments in TPSCo
 - early R&D stage
 - HV MAPS → Up to now larger pixel pitches $>25\mu\text{m}$
- End of project deliverable
- No decision on technology made yet



by SILAB, Bonn



by CERN, DESY, IFAE



by Mu3e collab.

[Talk by A. Herkert](#)

Common Cold Box for all telescope users

- Avoid duplication of work
- Position independent plug and play solution
- Managed by A. Rummler @ CERN
- Discussed within ATLAS (Aboud Falou / IJCLab) → Preliminary agreement to get the design done within his group
- Design parameters discussion ongoing
- Slowly moving towards critical path

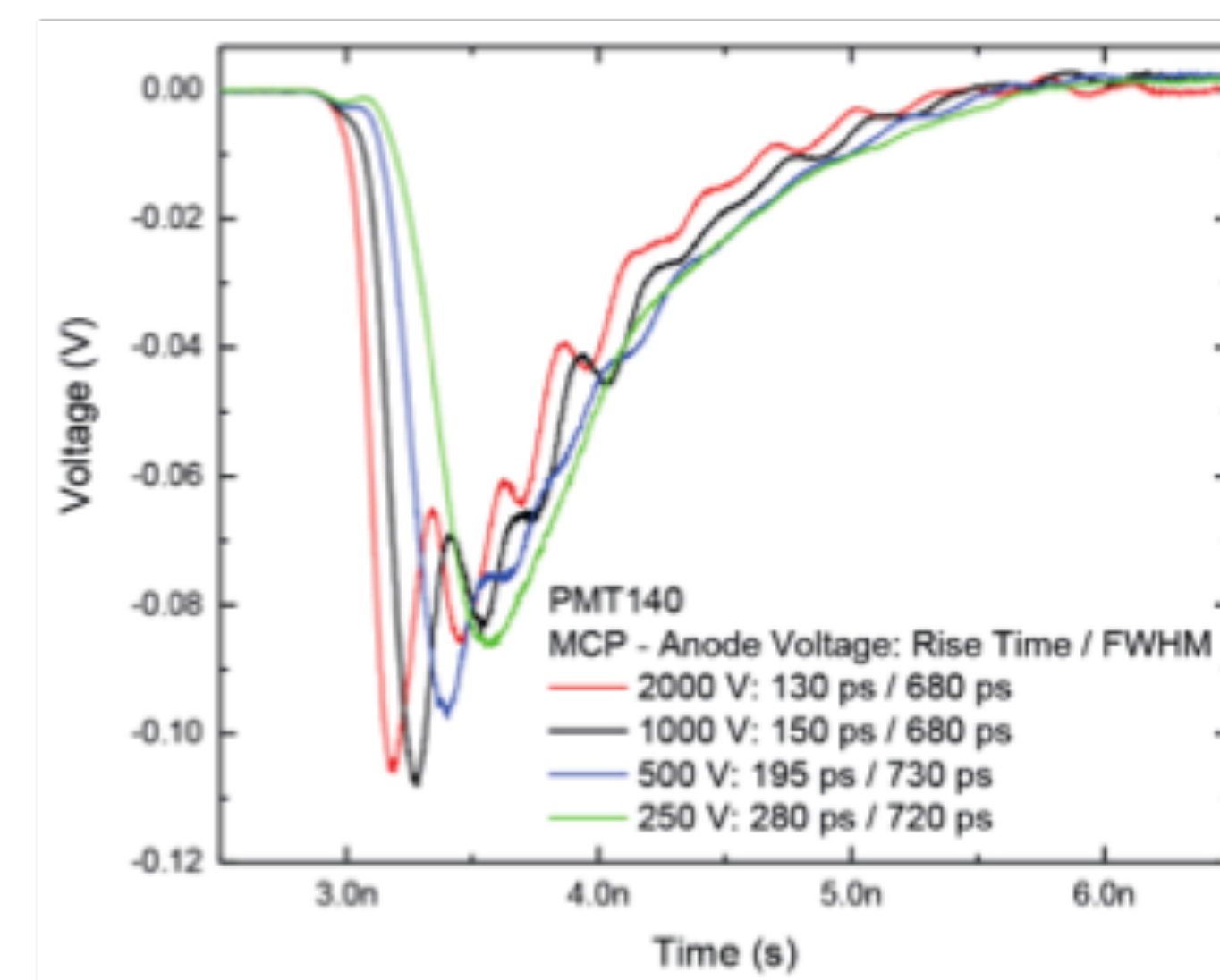
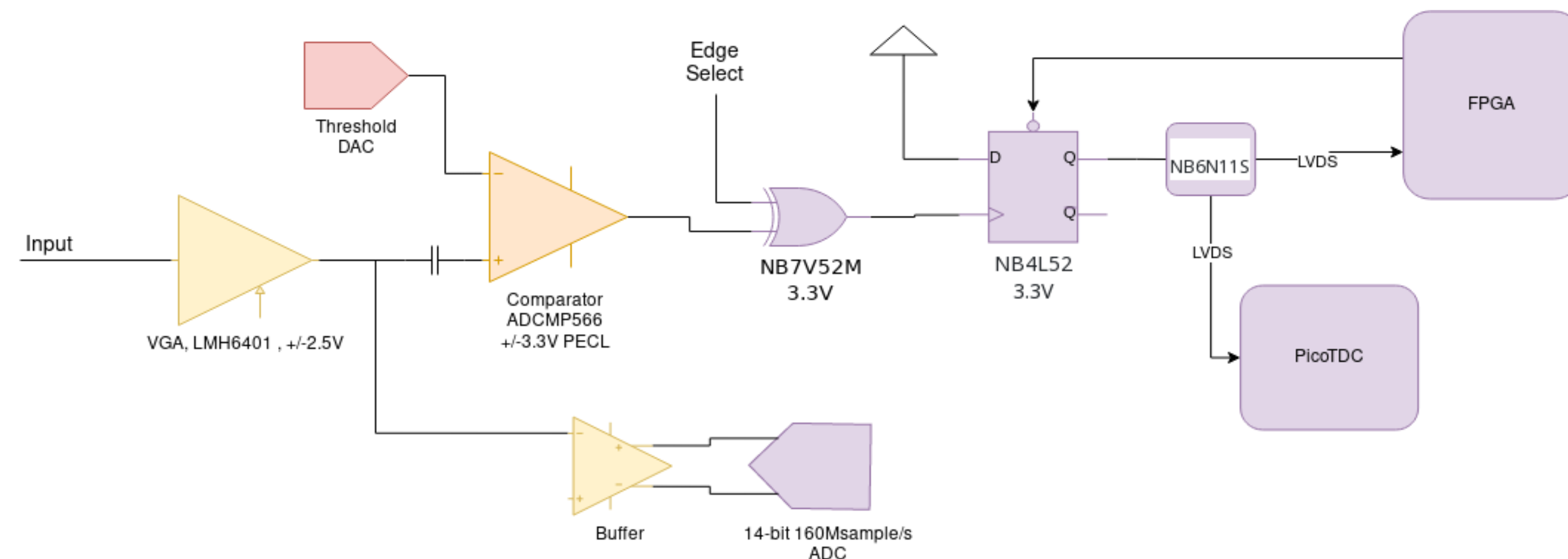
Testing pico-second detectors requires pico-second time reference

- **Timing specification:**
 - Clock jitter < 10ps RMS
 - Timing-stamping of input signals $O(10\text{ps})$ RMS
 - c.f. $O(1\text{ns})$ for AIDA-2020 TLU
- **Backwards compatible with AIDA-2020 TLU**
 - Same signals on DUT connections
 - trigger/busy/DUT-clk in EUDET-mode
 - Global-clk, trigger, busy, shutter, T0 in AIDA-mode
 - Small change to data format – timestamp will need more bits
 - Extend ProtoDUNE timing system
 - Interfaces to DUT still under discussion
 - Clock jitter of 12ps measured (**DOI** 10.1088/1

[Talk by D. Cussans](#)



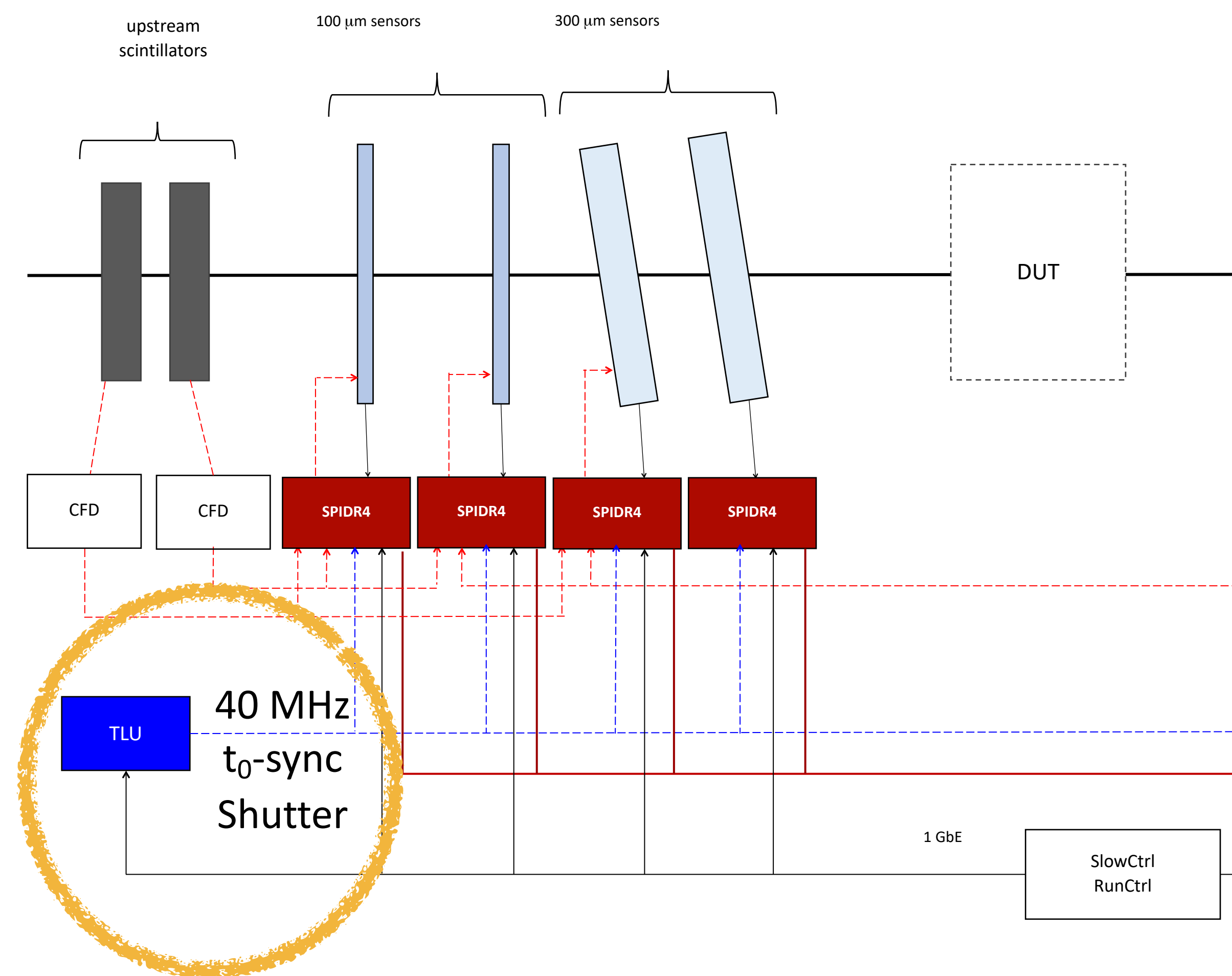
- Precise trigger input circuitry required:
 - ~ 4GHz -3dB bandwidth to comparator
 - Adjustable gain
 - ADC for pulse-by-pulse time-walk correction.
- Baseline timing detector:
- Either MCP-PMT or LGAD
- For testing anticipate using Cherenkov light and high speed photo-detector:
 - Used for “TORCH” LHCb upgrade beam-tests
 - MCP-PMT single photon jitter 66ps FWHM <http://www.photek.co.uk/pdf/datasheets/detectors/DS006%20Photomultiplier%20Tube%20Datasheet%20issue%202.pdf>
 - Reports of single particle timing < 10ps RMS



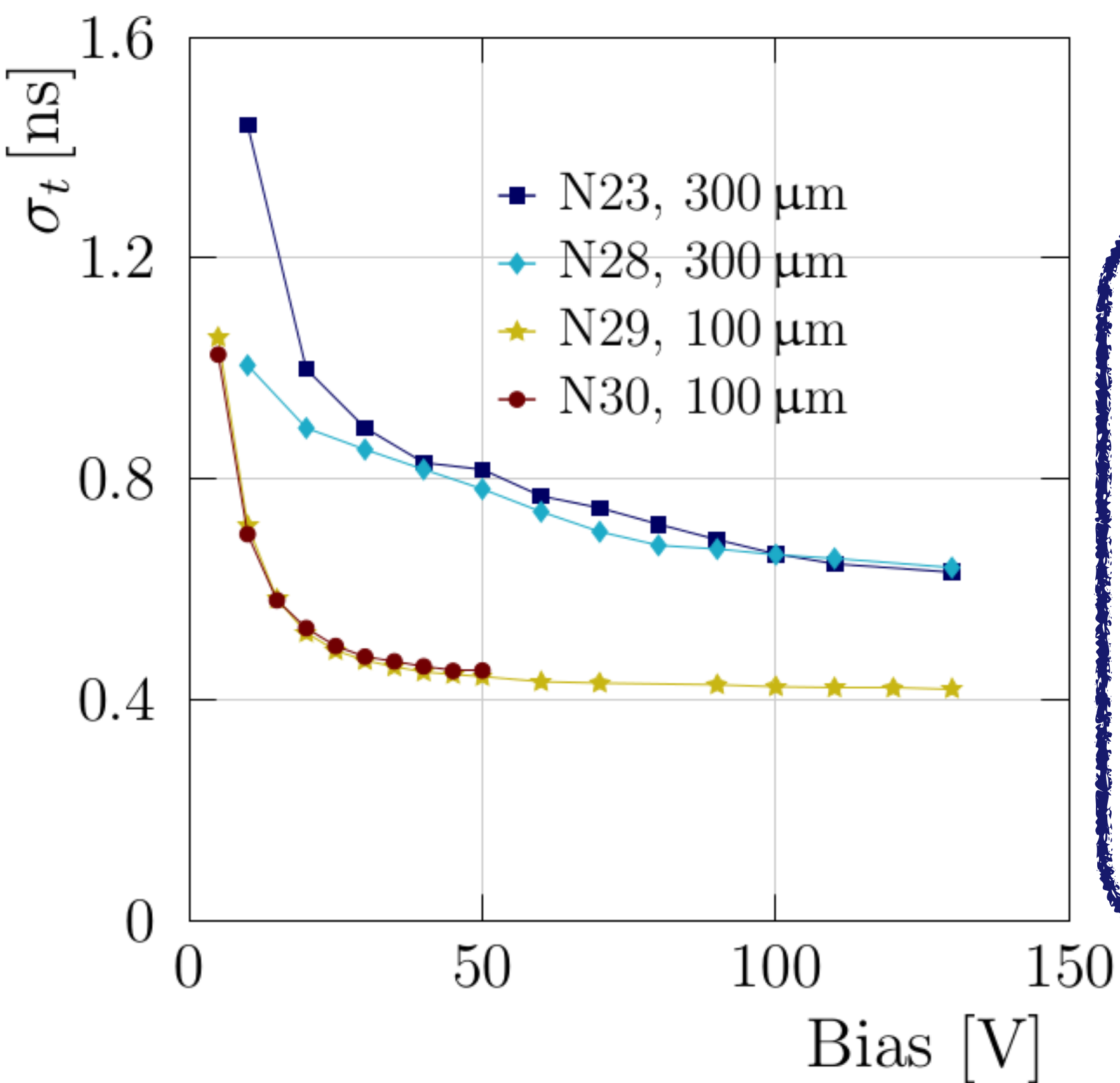
<http://dx.doi.org/10.1016/j.nima.2016.06.087>

Fast pixelated track timing plane based on Timpix4

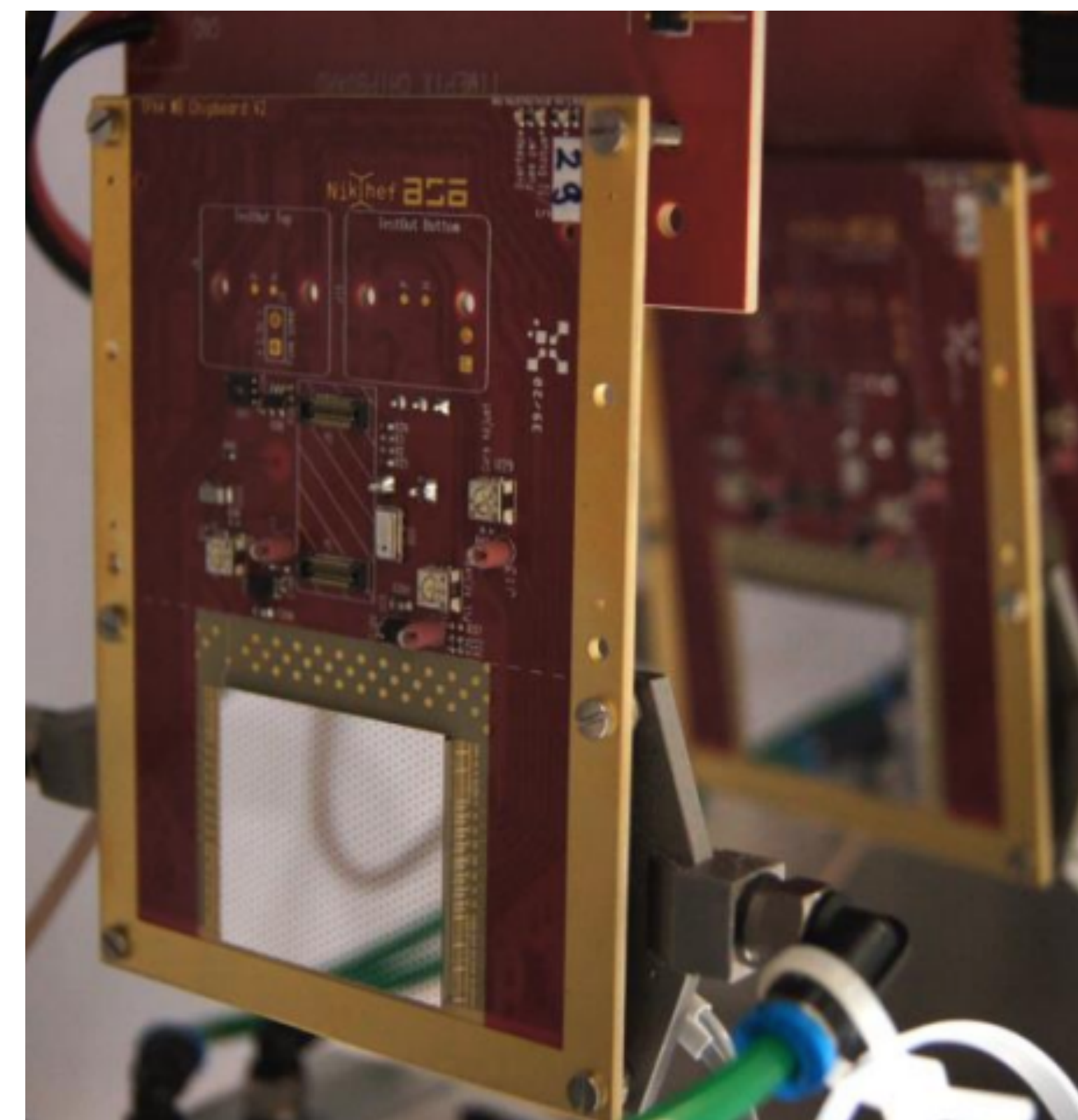
- ASIC available and functional
- 512 x 448 pixels at 55x55 μm^2 pitch
- 195 ps TDC bins \rightarrow 100ps should be possible
- 10Gbit/s default readout
- 8 layer telescope used in beam
- Design of synchronisation highly aligned with current TLU
- **Missing software integration into EUDAQ**



Standard AIDA 2020 TLU interface signals



- Sub-ns timing achieved
- Aiming for 100ps timing
- ➔ require faster sensor (eg LGAD)
- EUDAQ2 integration last missing step
- On track



[K. Akiba et al., 'Reconstruction of charged tracks with Timepix4 ASICs', Journal of Instrumentation, vol. 18, no. 02, p. P02011, Feb. 2023.](#)

[Talk by M. van Beuzekom](#)

- Development of EUDAQ2 software to support picosecond timing of next generation sensors
- Development of versatile online monitoring for EUDAQ2



[Talk by A. Loeschke](#)

2. EUDAQ2 .ini file

```
[Monitor.my_mon]  
CORY_PATH = /path/to/corry
```

3. EUDAQ2 .conf file

```
[Monitor.my_mon]  
CORY_CONFIG_PATH=corryconfig.conf  
CORY_OPTIONS=-v INFO  
DATACollectors_TO_MONITOR = my_dc0, my_dc1  
CORRESPONDING_EVENTLOADER_TYPES = Ex0raw, Ex1Raw
```

Status:

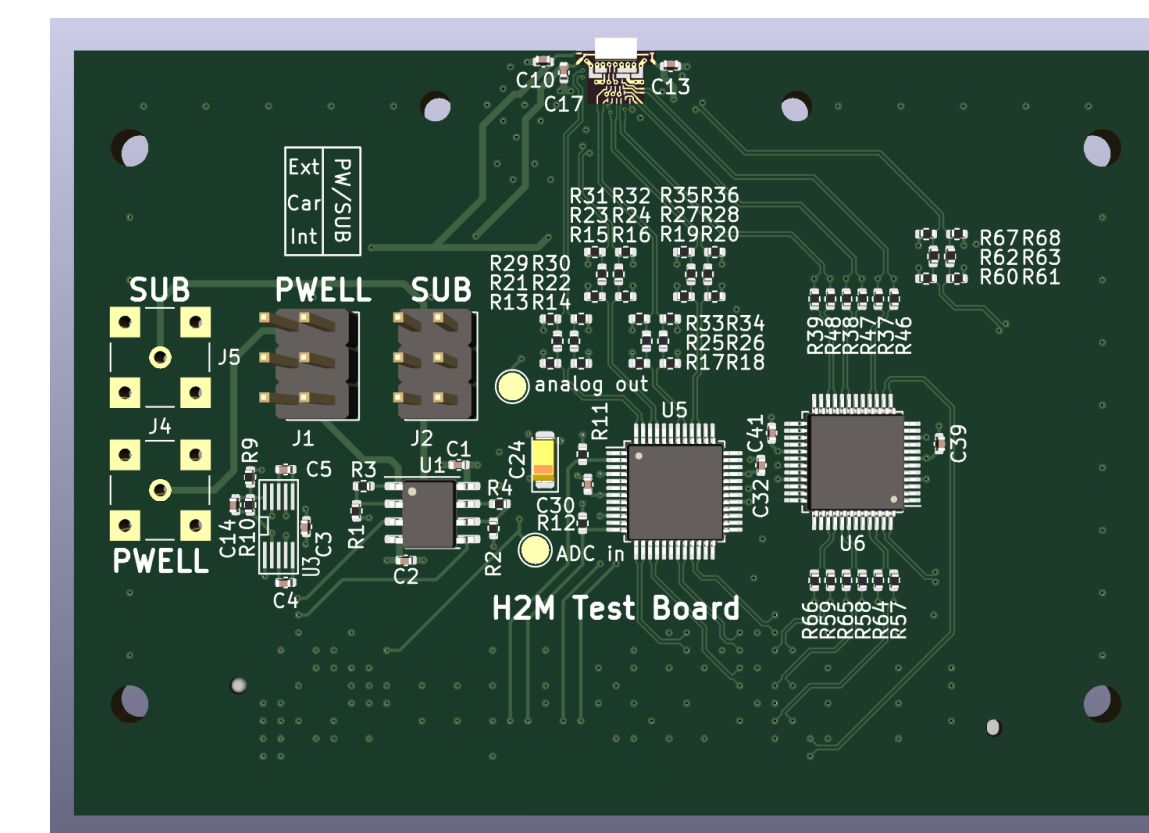
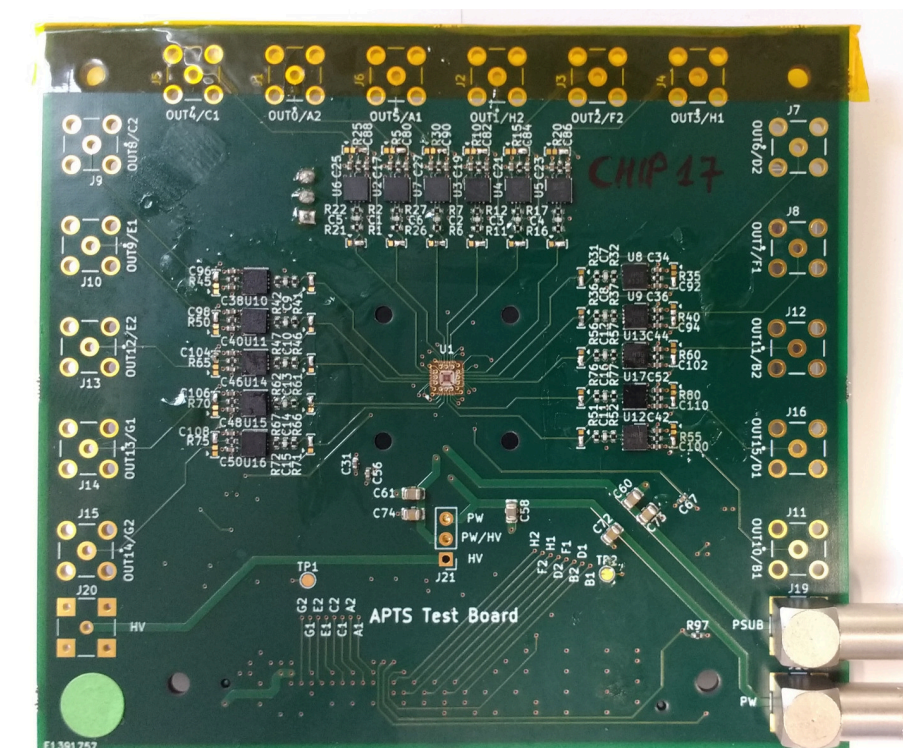
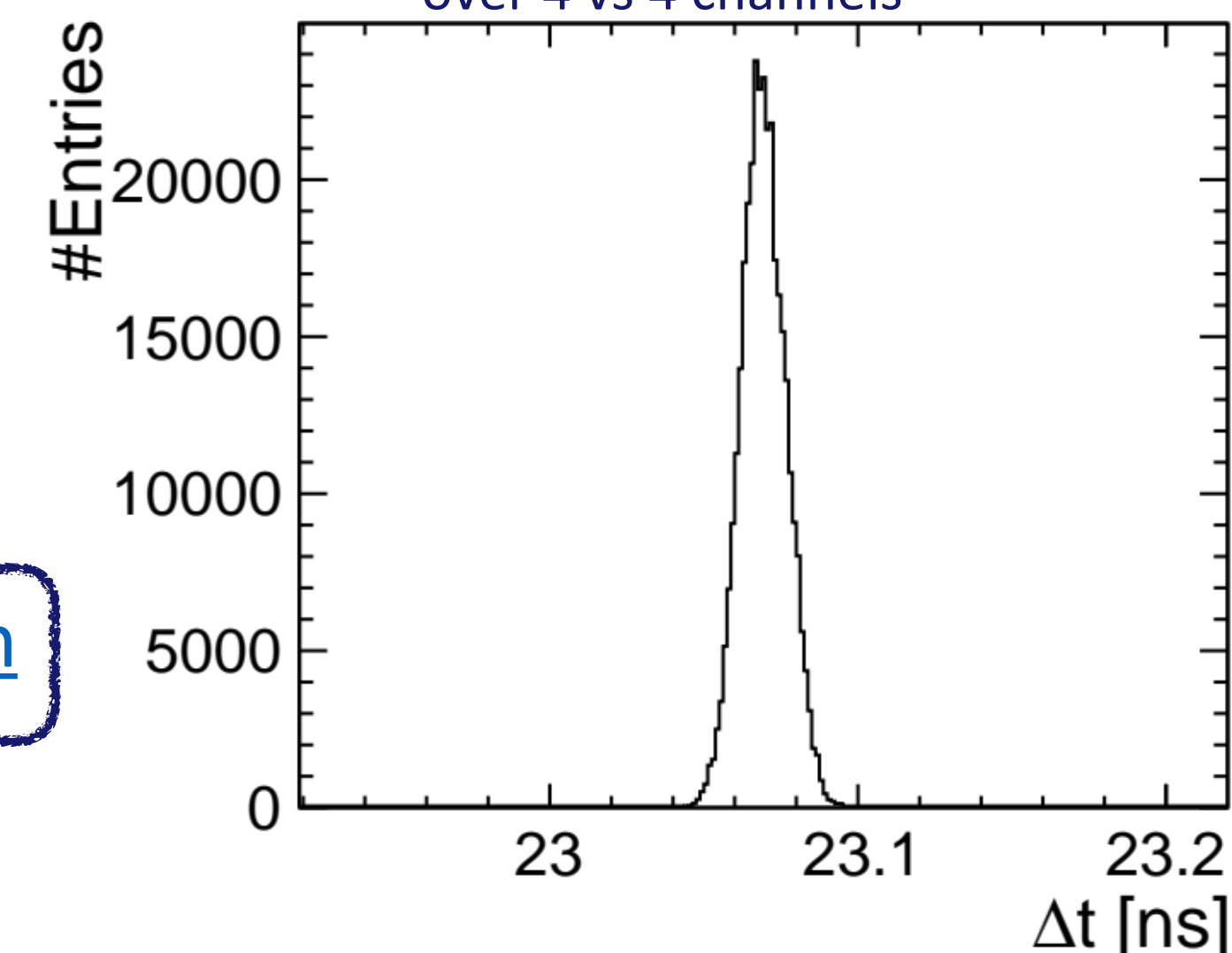
- Integration written and working → Third type of online monitor
- Default way of EUDAQ configure → Easy to use
- First tests to be done with beam next week (@DESY)
- Minor convenience features to be added
 - Reading data from different computers on the network
 - Skipping events to have real online feedback

- Based on modular hardware, firmware and Peary software
- Successfully used by several AIDAInnova / RD50 institutes for various pixel projects
- Support from EP R&D, RD50 (HW-production), and BNL OMEGA group, Carleton University, ORNL (HW-design)

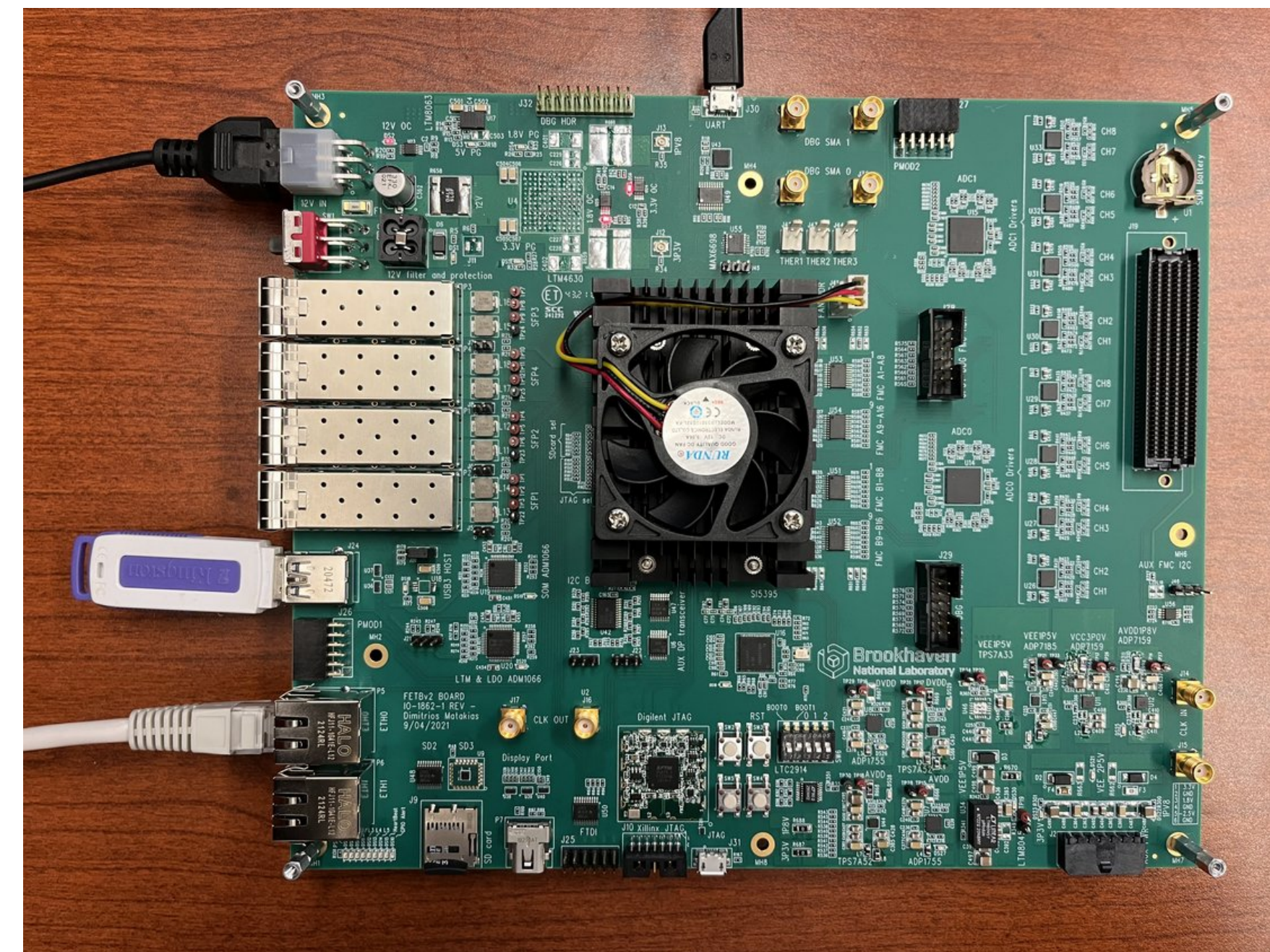
[Talk by E. Buschmann](#)

- Recent progress:
 - Integration of 65 nm test chips (DPTS MLR1, APTS MLR1) and tests in lab and beam
 - Integration of fast sampling ADC on Carboard for APTS readout
 - Development of sub 10 ps resolution TDC on Caribou FPGA for chips with asynchronous readout
 - Integration of new 65 nm H2M MLR2 chip ongoing
 - Development of Caribou 2.0 ongoing

TDC time resolution avg delay over 4 vs 4 channels



- Outlook:
 - Caribou 2.0 based on SOM platform: reduced cost, improved performance
 - Active design effort by Carleton, BNL, ORNL
 - First prototypes expected in 2023
- Milestones and Deliverables:
 - MS11 [M23]: Common readout boards designed (CERN)
 - Achieved with Carboard v1.4 together with VMM3 ✓



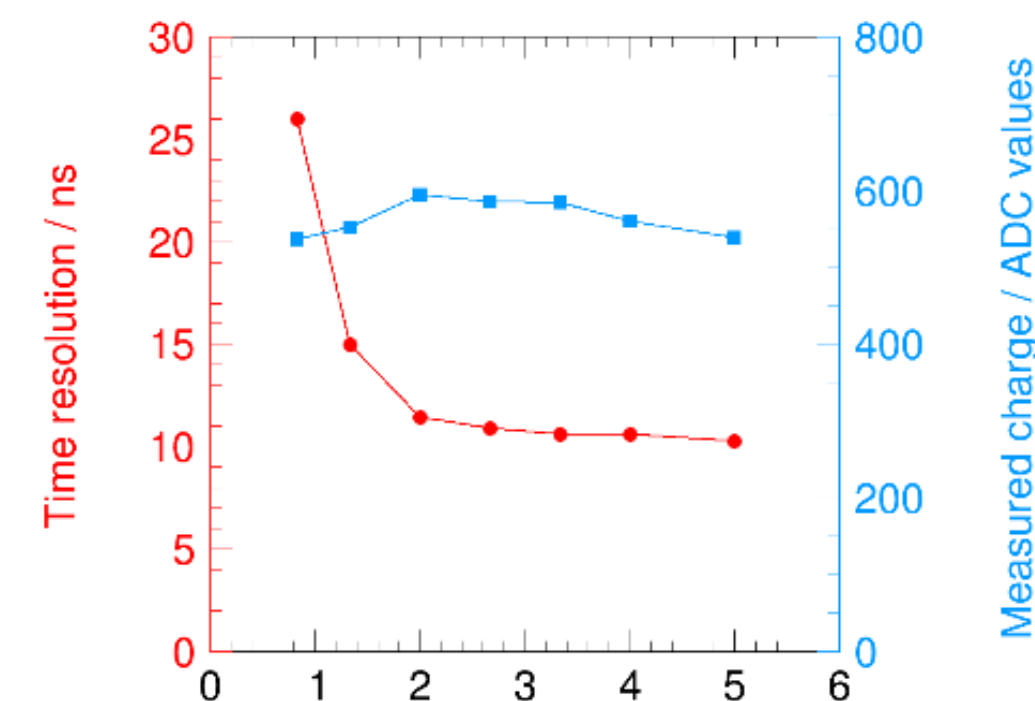
Pre-prototype for Caribou 2.0

Based on the RD51 Scalable Readout System. Scalable from laboratory test bench up to test beam and medium size experiments.

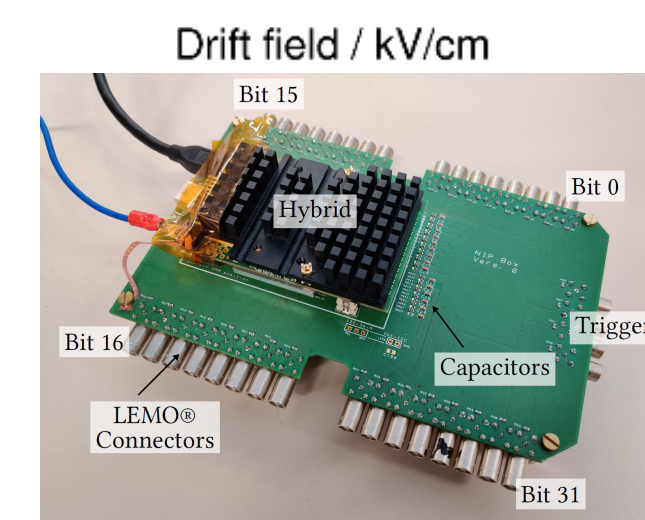
Recent progress:

- Complete beam telescope with three triple-GEM tracking detectors and scintillators for timing: Multiple DUTs at the same time, full characterization (energy, space and time) with single front-endelectronics.
- Signal injector board developed:
- Operation stability and DAQ efficiency:
 - Beam telescope used as **tracking system in NA61/SHINE** physics run for neutrino target interactions.
 - 5 weeks without DAQ failure.
 - Integration of **self-triggered telescope** into externally triggered NA61/SHINE via injector board.

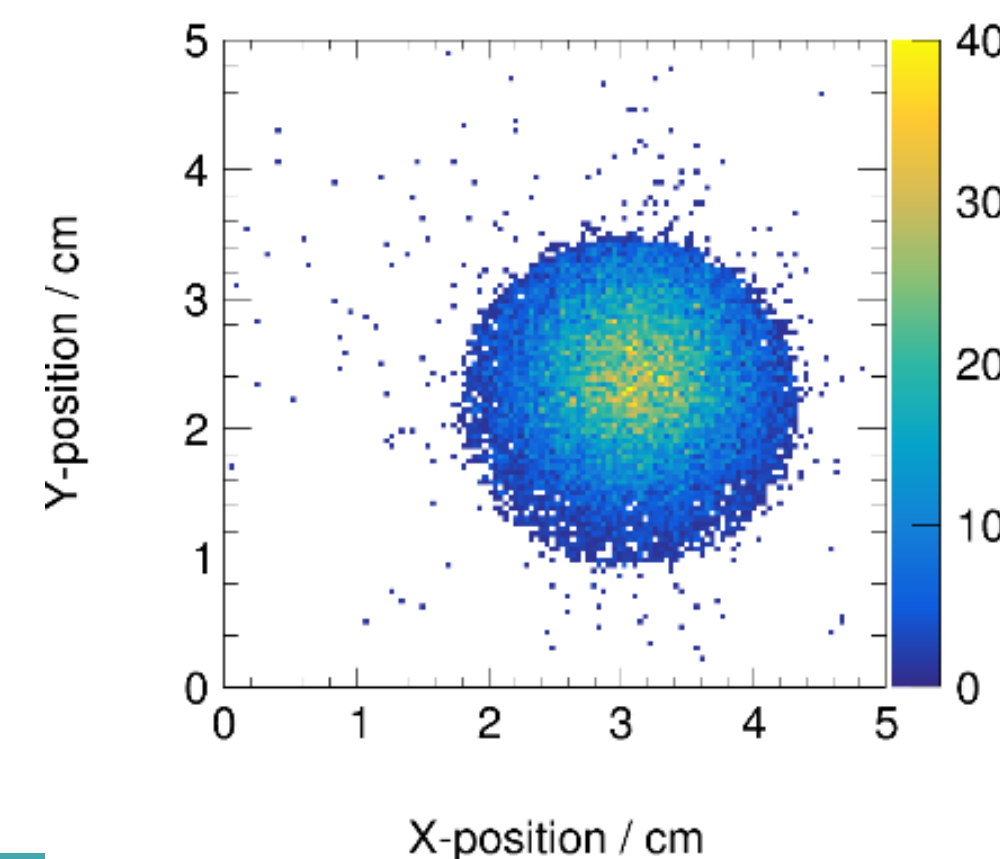
[Talk by L. Scharenberg](#)



Time resolution and charge collection in μ RWELL



Signal injector board



Matched events from NA61 and VMM3a/SRS telescope

Future plans:



- Implement **externally triggered mode** for readout electronics (requires firmware adaption)
- Development of **different powering scheme**. Read out beam telescope with **large lever arm (~ 50 m)**
- Integration into EUDAQ

Milestones and Deliverables:



- MS11: Common readout boards designed [M23], prototype developed
- D3.5: Common readout board delivered [M42], report
- Third production in delivery, fourth production expected in 2024 with hardware available for gaseous detector community and test beams at CERN

- WP3 is performing well
- All suffered the past pandemic:
 - Chip delivery crises
 - COVID induced travel restrictions
- Currently all milestones/ deliverables achieved in time
- Three more to come until the next AIDA annual meeting:
 - MS8 may be delayed due to restart of R&D
 - MS9: DAQ ready, EUDAQ integration missing
 - MS10 is done, needs testing efforts
 - D3.1 moving towards critical path

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