WP11 2nd annual meeting

A. Rivetti (INFN) Ch de La Taille (CNRS)

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

Objectives

- **Task 11.1. Coordination and Communication [CNRS+INFN]**

- **Task 11.2. Exploratory study of advanced CMOS (28 nm)**
  - INFN PV, AGH, CNRS CPPM, UBONN
  - Explore advanced 28 nm CMOS for future trackers AGH, CNRS CPPM
  - Design and test front-end prototypes INFN PV, UBONN

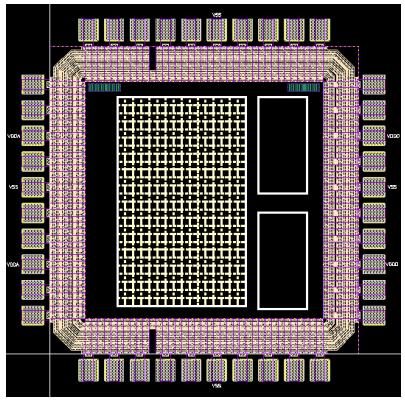
- **Task 11.3. Networking and ASICs for other WPs (65/130 nm)**
  - AGH, CNRS OMEGA, IP2I, DESY, INFN (BA, BO, PV, TO) Uni Heidelberg, WEEROC (industry)
  - Cold and timing ASICs in 65/130nm CMOS : CNRS OMEGA, IP2I
  - MPGD readout ASICs : INFN (BO, TO)
  - Silicon and SiPM readout ASICs for future colliders and timing applications : AGH, CNRS OMEGA, DESY, UniH, WEEROC

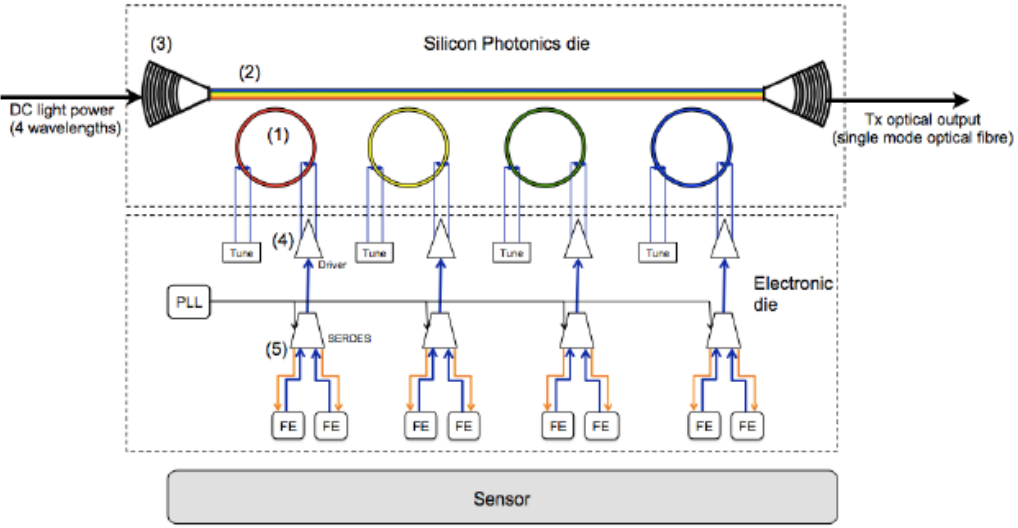
tasks 11.2 (28 nm)

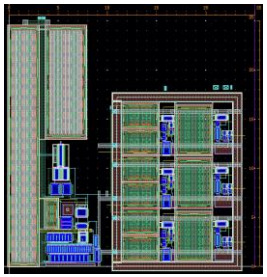
- AGH : study ADCs and PLLs and participate to next LPGBT
  - Ultra-low power ADC 10bits 100 MHz <1 mW
- CPPM : test vehicles for SEU/SET and TID studies
- Ubonn : study FPGA implementation for next generation chips and digital blocks
- INFN PV : work in synergy with FALAPHEL INFN project, further studies of analog front-ends and IP blocks
  - Two different Analog Front Ends are being investigated :
    - ToT A/D conversion
    - Flash A/D conversion

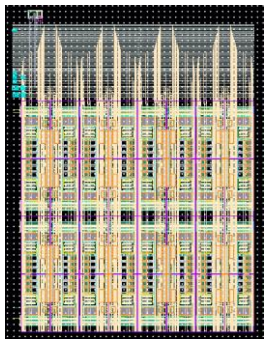
Results/highlights 11.2 28nm

- Several blocks are ready or being finalized for MPW submission
  - Test chip for SEU studies (CNRS CPPM)
  - Low noise preamplifier (INFN PV)
  - Flash ADC block (INFN PV)
  - Ultra-low power SAR ADC (AGH)
- MPW in october 2023
- Design review in nov 2022 = Milestone MS45







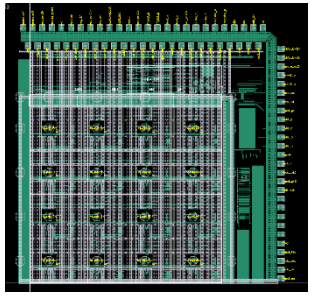


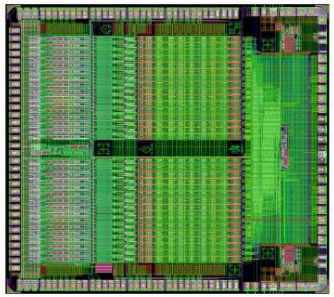
Tasks 11.3 (130 nm)

- AGH : FLAME/FLAXE readout ASIC for LUMICAL, new 10 ps TDC development
- CNRS IP2I : plan to do cryogenic tests on low dropout regulator prototype
- CNRS OMEGA : AC LGADs timing chip readout in 130 nm
- DESY/Heidelberg : study of SiPM Tile boards with KLAUS5/6 readout
- INFN BA/PV : MPGD 32ch readout ASIC in 130n 12b ADC + 100ps TDC, dual polarity, variable peaking time.
- INFN BO/LNF/TO : uRwell readout chip, based on TIGER chip. Test uRwell chambers with APV and TIGER. Design dedicated chip in 130n.
- INFN TO : engineering run in UMC110n for timing detectors
- WEEROC : SiPM readout for timing and LIDAR applications.

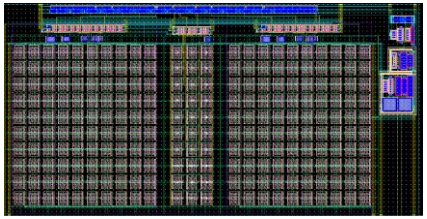
Highlights 11.3 130nm

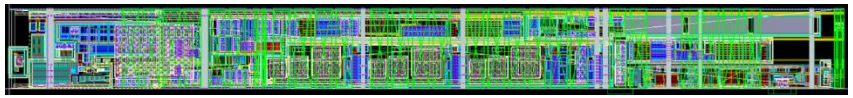
- Several chips designed for the other AIDA INNOVA workpackages
  - 10 ps TDC (AGH)
  - FLAXE (AGH) : Si/GaAs readout
  - EICROC (OMEGA/AGH/CEA) : LGAD readout
  - LIROC (WEEROC) : SiPM timing
  - PSIROC (WEEROC) : Si readout
  - Fabrication january 2023





- More chips still in design
  - MPGD and RPD readout (INFN BA/PV)

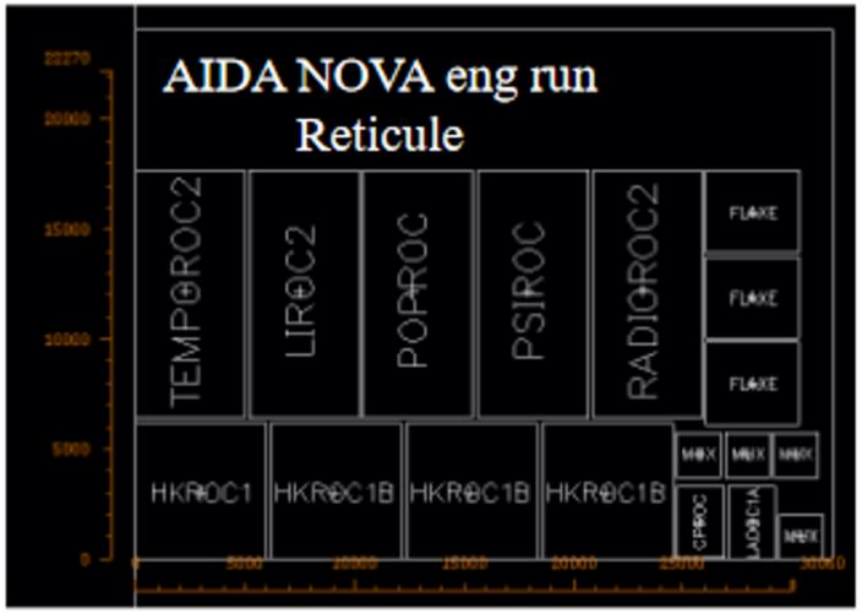




AIDA engineering run

- AIDA participation in a 130nm engineering run constitutes D1.1
  - ~25% of the reticle area = 25% of the total cost (250k€)

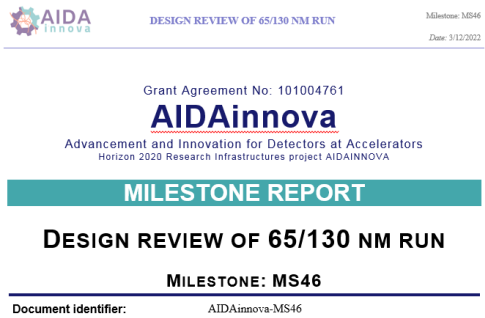
- 4 chips from AIDA-INNOVA partners on this run
  - FLUXE (AGH)
  - EICROC (OMEGA/AGH/CEA)
  - LIROC (WEEROC/OMEGA)
  - PSIROC (WEEROC)
  - Submission scheduled jan 2023
  - Several hundreds of chips will be available



- Chips reviewed in november 2022
  - Constitutes Milestone MS46

Deliverables/Milestones

- 2 Milestones and 2 deliverables
  - MS 11.1 and 11.2 (MS45 MS46) passed end 2022
  - D11.1 and 11.2 are the corresponding chips


AIDA innova — DESIGN REVIEW OF 65/130 NM RUN — Milestone: MS46 — Date: 3/12/2022

Grant Agreement No: 101004761

AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

DESIGN REVIEW OF 65/130 NM RUN

MILESTONE: MS46

Document identifier: AIDAinnova-MS46

MS11.1	**Design review of 28 nm MPW**	**11.2**	**18**	**report**
MS11.2	design review of 65/130 nm run	11.3	18	report

Deliverables related to WP11	
D11.1: MPW 28 nm *The deliverable is a multi-project wafer fabrication with the different test ASICs in CMOS 28 nm*	24
D11.2: MPW 65/130 nm *The deliverable is a multi-project wafer fabrication with ASICs in CMOS 65 and/or 130 nm that can be used to readout detectors from the other WPs and in particular WP8*	24
D11.3: Measurement reports *Each of the ASIC fabricated in the 2 previous deliverables will have its design and performance documented in a report*	42

Summary

- Microelectronics is a key technology enabler for novel detectors
- 2 main pillars in AIDA INNOVA
  - Explore 28 nm technology performance for HEP
  - Provide readout ASICs in 130nm for other WPs
- 2 fabrications will occur in 2023 to match these objectives
  - Milestones MS45/46 and deliverables 11.2/11.3
- + Networking activity and sharing of expertise among participants
  - Several ASICs in co-design
- One industrial partner for technology transfer and spinoff