28 nm CPPM Activities

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CPPM/IN2P3 - Aix-Marseille Univ, France

2st AIDAinnova annual meeting
WP11.2 : Exploratory study of advanced CMOS (28 nm)
24-27 April, 2023

Outline

- Introduction: the context of this activity
- Bloc design
  - SET Testing structures
  - Ring oscillators for the TID tolerance test
  - Small pixel matrix: fast charge amplifier
- Current status and perspectives

Introduction

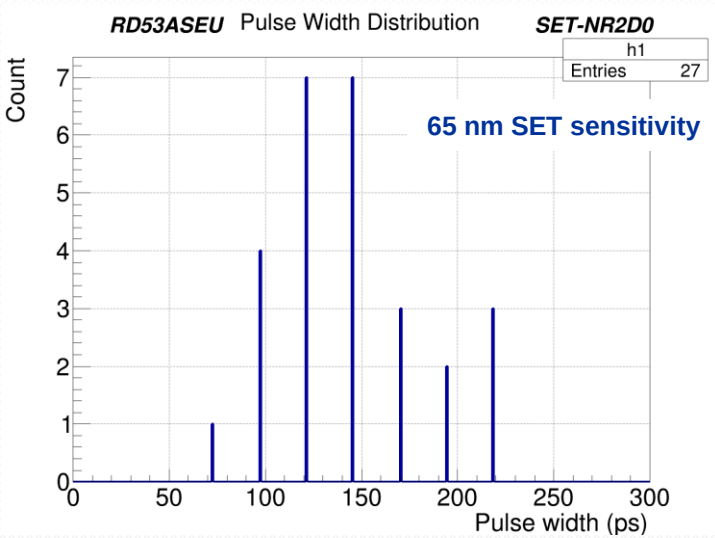
- R&D around **hybrid pixels** for **future upgrades** with the 28nm CMOS technology
  - The **radiation tolerance** of the 28nm process up to 1-2 Grad
  - **Time measurement** with a resolution better than 50ps
  - Small pixel size -> **25µm × 25µm**
- RD53 collaboration shows a strong interest in these developments for the future upgrades of ATLAS and CMS trackers
- The project is part of the R&D project DEPHY initiated by Marlon Barbero (CPPM) and can be extended to the other IN2P3 labs interested in the 28 nm process
- 28nm CMOS mini@sic of 2 mm x 1 mm submitted December 2022
- **Basic design kit** from IMEC used for the design
  - 28 nm HPC+
  - No difficulties with the analog design at the transistor level
  - Lot of time and effort to develop a methodology for digital designs using the **digital flow**
- This work is done in relation to the **CERN R&D Program** on Technologies for **Future Experiments**
- Different test structures implemented in the chip prototype
  - TID qualification
  - SEU/SET testing
  - 4D tracking -> Fast charge amplifier for pixel Front end

SEE/SET Testing

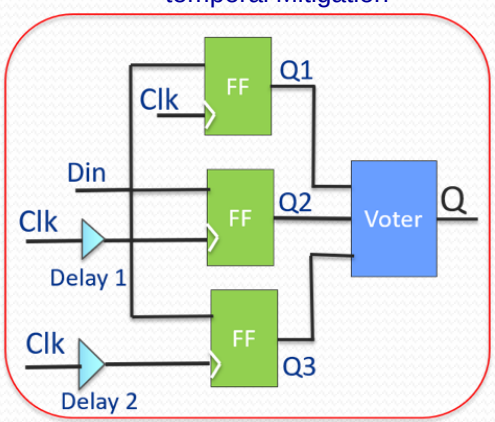
- The SEE mitigation is a major challenge for the next generation of pixel chips because of the luminosity increase
- SET propagation through combinatorial logic and generate SEU in memories, FIFO and state machines …
- SET sensitivity increases with process advance and with speed

- SET test structures implemented in the prototype chip will allow characterizing the 28nm CMOS process for SET tolerance

- **Objectives :**
  - Measure the SET cross-section
  - Measure the SET pulse with a **good resolution < 20 ps**
  - Measure the effect of the std cell size
- Allows for example to define the delay to be imposed for the triplication with time mitigation



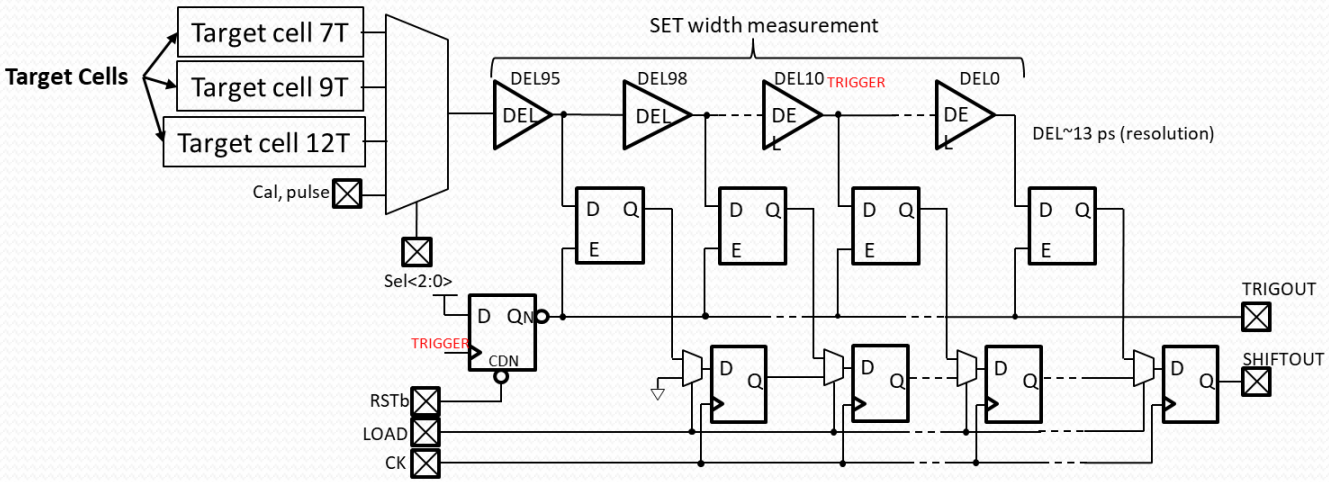
SEU tolerant design with temporal Mitigation

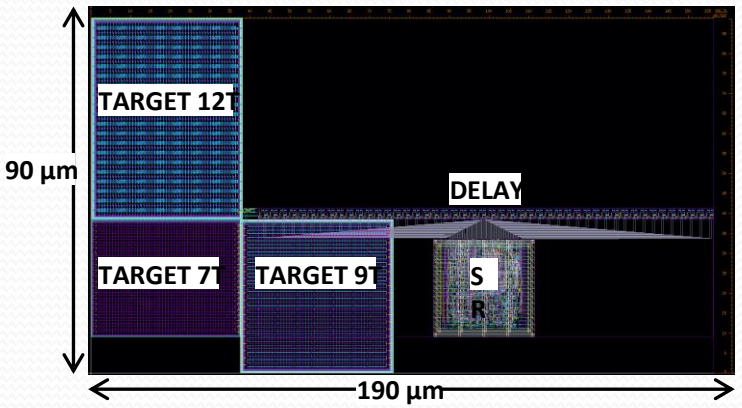


SET Bloc design

Designer : Denis Fougeron

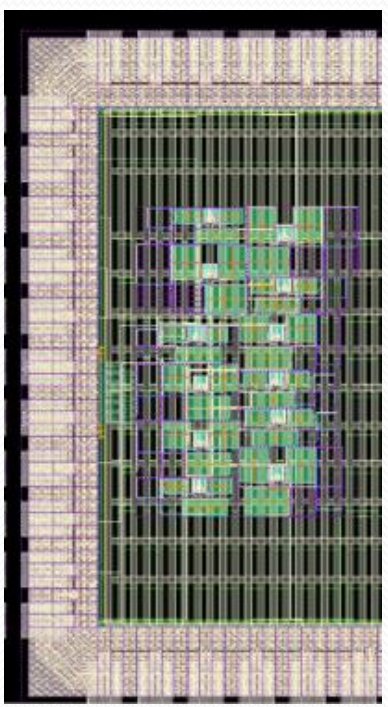
SET sub-bloc synoptic





Layout example for INVD4 cell

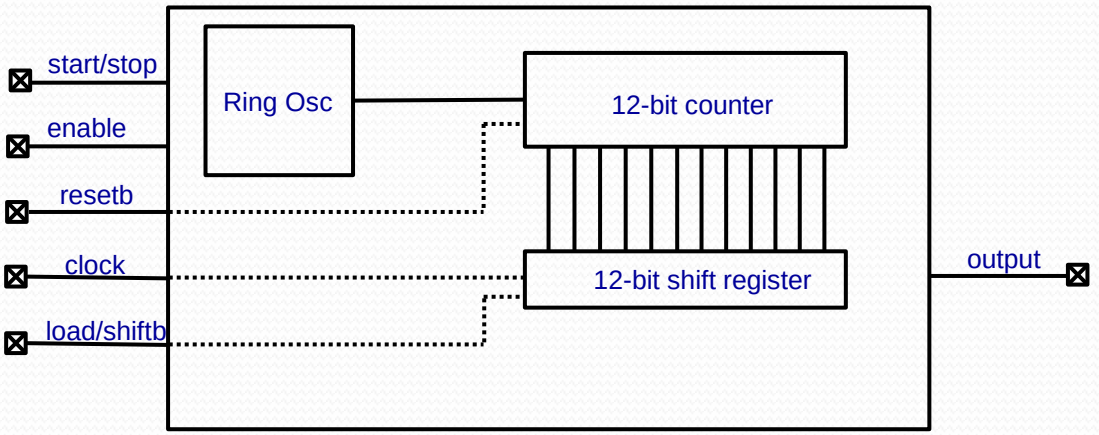
- Each sub-bloc contains
  - 3 target cells made up of thousands of basic cells + 1 calibration input
  - Circuit for SET width measurement 96 delay cells (13ps/cell) -> from a few ps to 1 ns
  - Shift register to send the data to the output when a trigger signal occurs
- 31 SET sub blocs
  - 24 uses SVT target cells (7T, 9T, 12T) -> **Effect of the cell size**
  - 7 uses LVT or HVT target cells -> Effect of **the device options**
- The whole bloc contains 6 inputs / 13 outputs
- In addition to SET testing, this constitutes a sub-block of the TDC required in the pixel front end



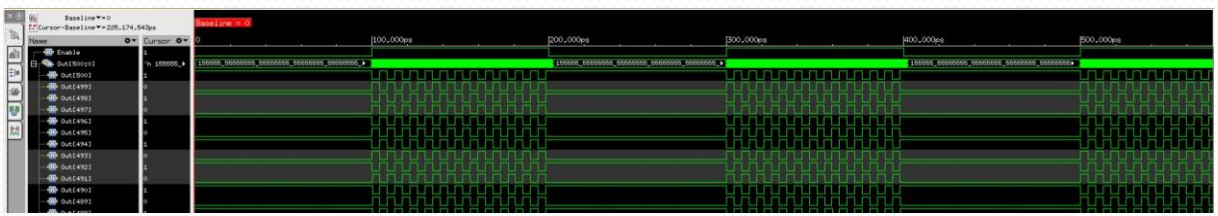
Ring Oscillator Design

Designer : Eva Joly

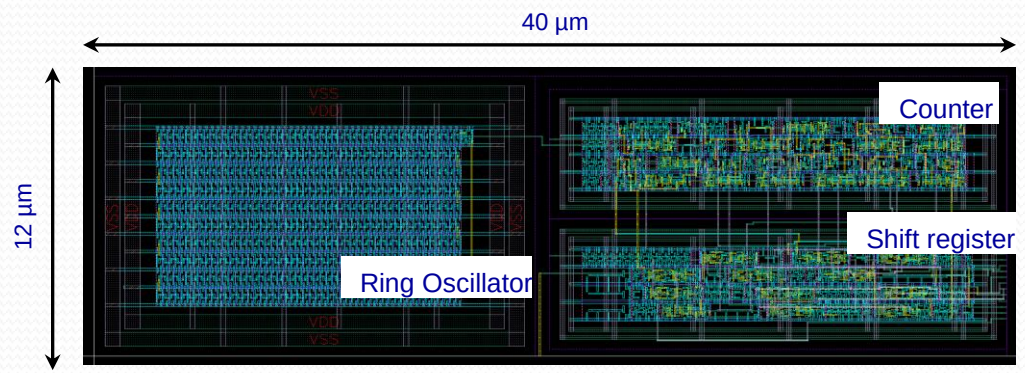
- Study the **effect of TID** on the performances of **digital standard cells**
  - Timing of combinatorial cells
  - Leakage currents and static power
- 96 ROsc sub-bloc
  - Cell size (7T, 9T,12T) -> **cell size** effects
  - Driving (D0, D2, D4) -> **cell driving** effects
  - SVT, LVT, HVT -> **device threshold** effects
- Design based on the **digital flow**



ROsc sub-bloc synoptic



Basic cells	Frequency (MHz)
INVD0	154
INVD2	222
NAND0	118
NAND2	143
NOR0	111
NOR2	139



Simulation

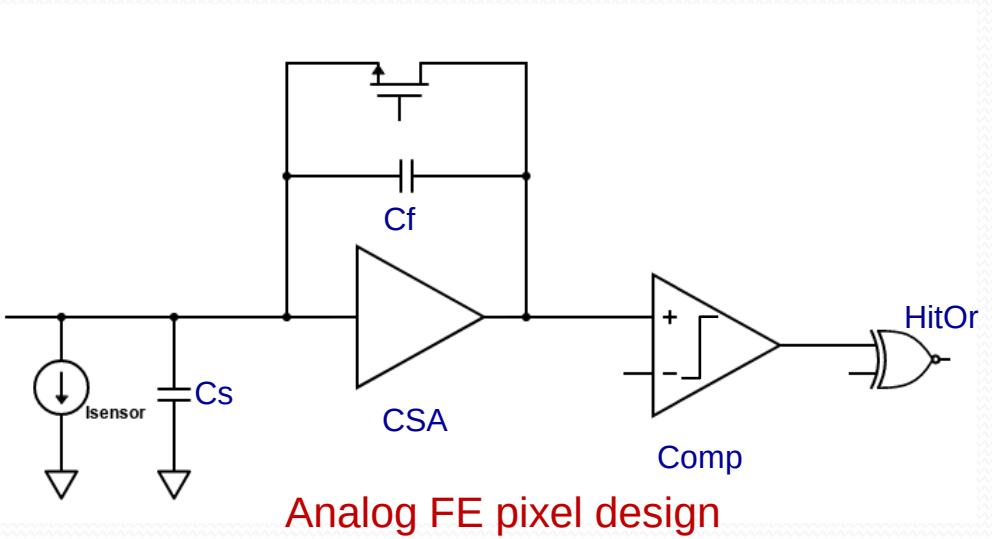
Manual layout

Synthesis

Fast amplifier design

- Study the limits to **time resolution** in the analog front- end designed with the **28 nm CMOS** process
- Effects of the Current bias, power supply, Bandwidth, Noise …
- Design and test a **pixel array of 36 × 12 cells** where only the analog part is considered and implemented
- The time resolution of a detector:

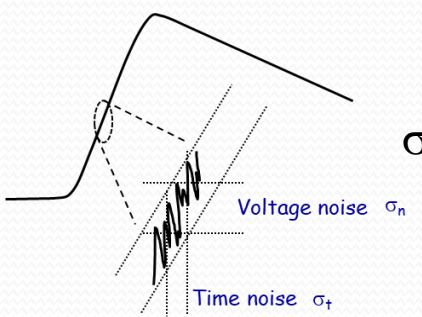
$$\sigma^2_{total} = \sigma^2_{jitter} + \sigma^2_{timewalk} + \sigma^2_{Landau} + \sigma^2_{TDC}$$



Analog FE pixel design

Minimizing the front-end jitter corresponds to :

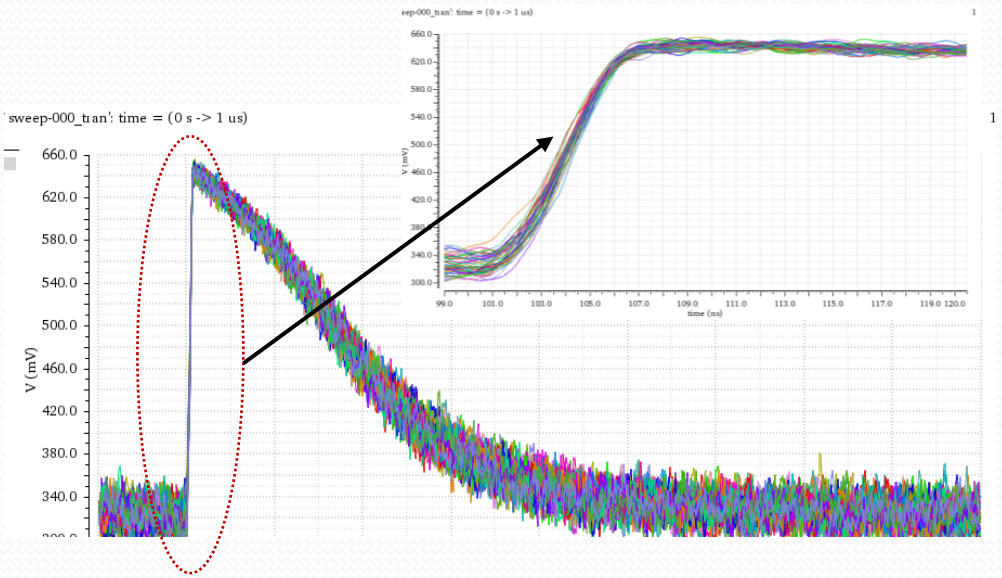
- Low RMS noise of the charge amplifier (CSA)
- High output voltage
- Small rise time → High bandwidth



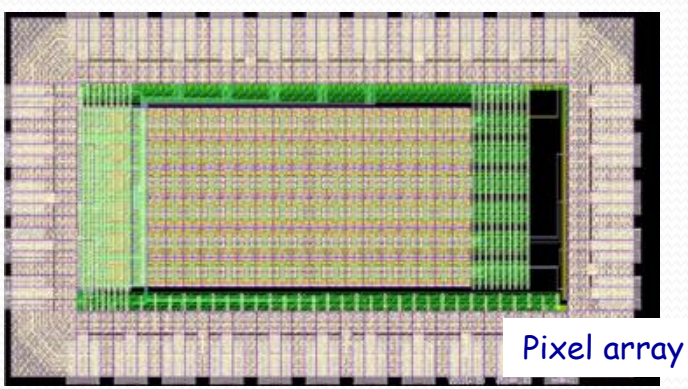
$$\sigma_{jitter} = \frac{\sigma_{noise}}{dV/dt} = \frac{t_r}{\left(\frac{S}{N}\right)}$$

Analog FE pixel prototype

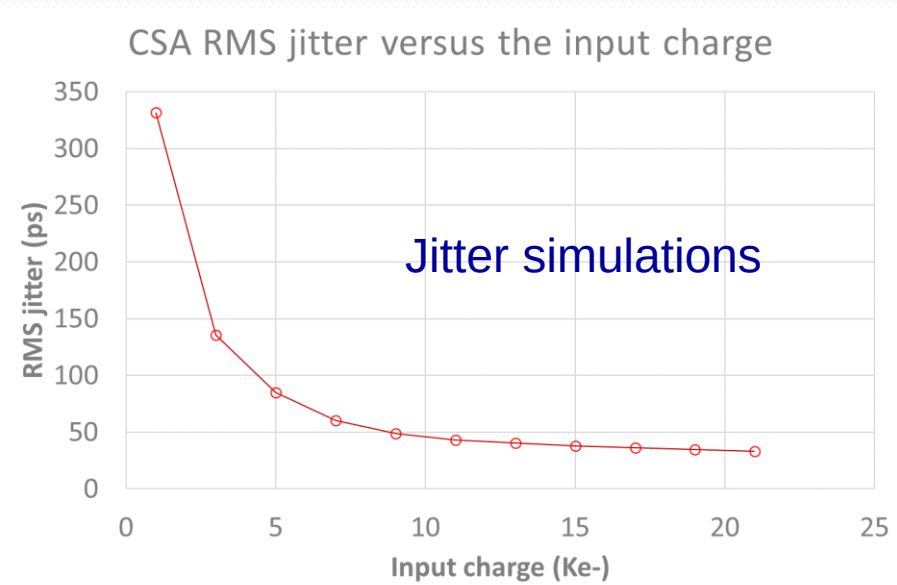
- For each pixel :
  - The charge amplifier current bias can be set in the range of 2µA-20µA
  - MOM capacitance connected to each preamplifier input -> test for different input capacitance values
- Large bandwidth buffers (> 1GHz) implemented and connected for a few pixels for direct jitter measurement
- Simulations for I_{CSA} = 5 µA
  - dV/dt = 100 mV/ns
  - RMS noise = 97 e- RMS for Cin = 100fF
  - Jitter < 100 ps RMS for input charge > 4 ke-
  - Jitter < 40 ps RMS for charge > 10 ke-
- Each pixel contains : CSA + Discriminator + 6 bit DAC
  - Size : 20 µm × 12 µm



50 superimposed transient noise simulations

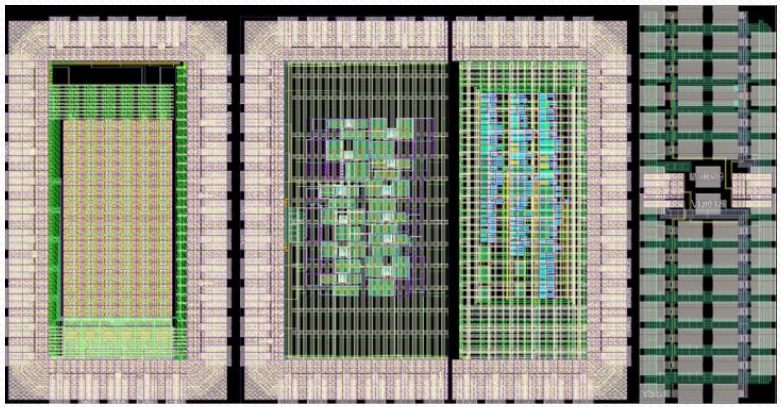


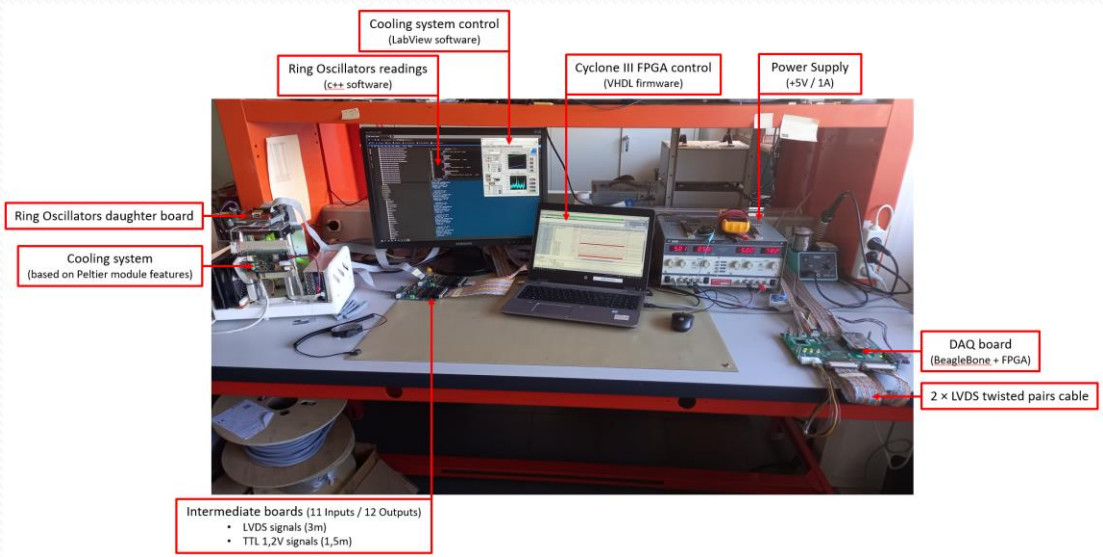
Pixel array of 36 × 12 pixels



Design progress

- The chip prototype submitted in December 2022
- People involved in this Design:
- It has just been shipped by IMEC through CERN
- Test set-up is under preparation
  - Adaptation of the set-up based on the BB board
  - Design of chip test boards
- Functional tests (Q3-2023)
- Irradiation test (TID + SEE) Q4-2023
- The signing of 3-way 28nm NDA was finally done
  - The CERN PDK will be used for future designs
- A new submission planned for Q1-2024
  - Dedicated to pixel array performances improvement





Thank you for your attention

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