28 nm analog front-end designs at University of Bergamo/INFN Pavia

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Bergamo/Pavia 28 nm activities in INFN projects

Falaphel (started in 2021)

- Development and integration of Silicon Photonics modulators with high speed, rad-hard electronics in 28 nm

INFN Padova, Pavia, Pisa, Scuola Superiore S. Anna di Pisa, UniPisa, UniMilano (P.I. Fabrizio Palla)

IGNITEd INFN Istituto Nazionale di Fisica Nucleare (started in 2023)

INFN Ground-up iNITiative for µElectronics developments

- develop a nominal-size, detector-grade ASIC (≈1-2 cm^2) in CMOS 28 nm technology, coupled to a Silicon Photonics integrated device for high-bandwidth data communications (4D tracking, rad-hard, low threshold operation,…)
- address the requirements of the inner trackers of the next generation of upgrades at colliders
- establish an operative and coordinated network for the exchange of competences at a national level and for a common R&D strategy in microelectronics

INFN Bari, Bologna, Cagliari, Firenze, Genova, LNF, Milano, Milano Bicocca, Padova, Perugia, Pavia, Pisa, Trento, Torino (P.I. Adriano Lai)

Front-end specifications and design in 28 nm CMOS

- Developing two analog front-end architectures, to be integrated in a pixel readout cell
  - Analog cell area reduced with respect to current 65 nm designs, room for more complex pixel logic
  - Reduced power consumption, 0.5 W/cm^2 → 6.25 µW/channel (analog+digital)

- **Time-over-Threshold (ToT)** based front-end → preamp + DC coupled comparator, with ToT A/D conversion of the signal + threshold tuning DAC

  Specs mostly **derived from RD53, but targeting operation at a lower threshold**

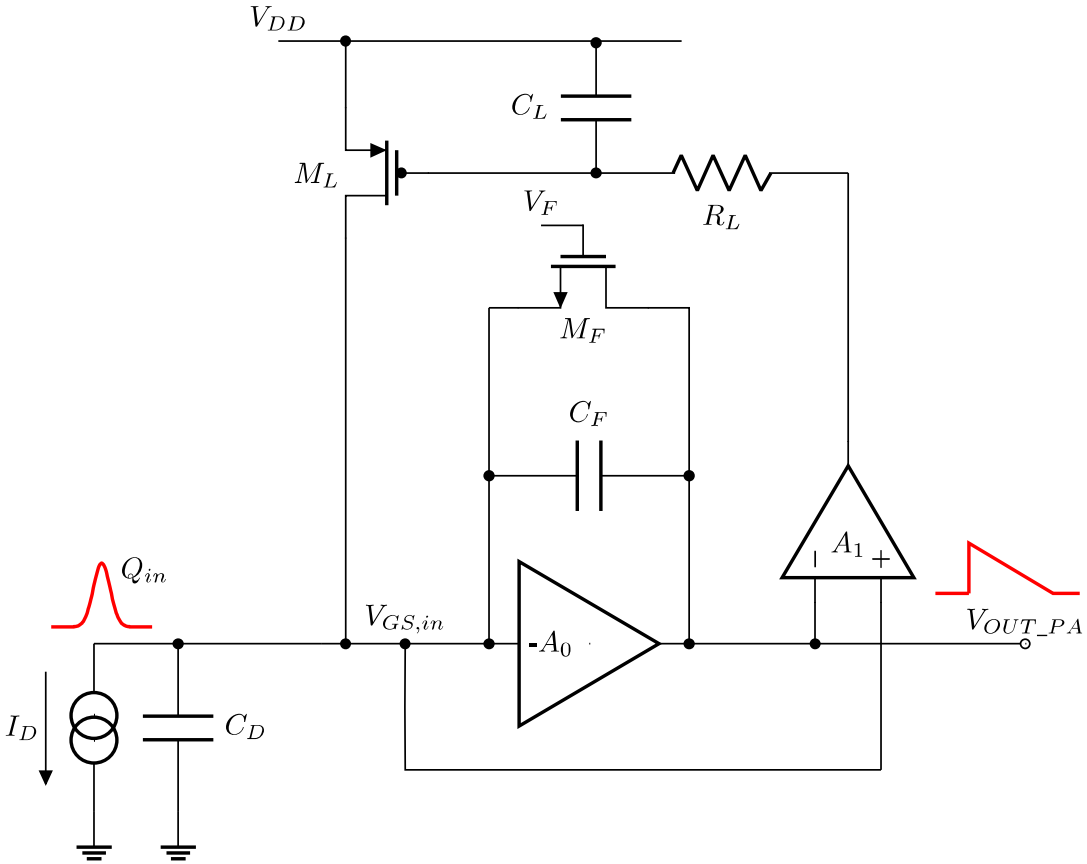
  (< 500 electrons)

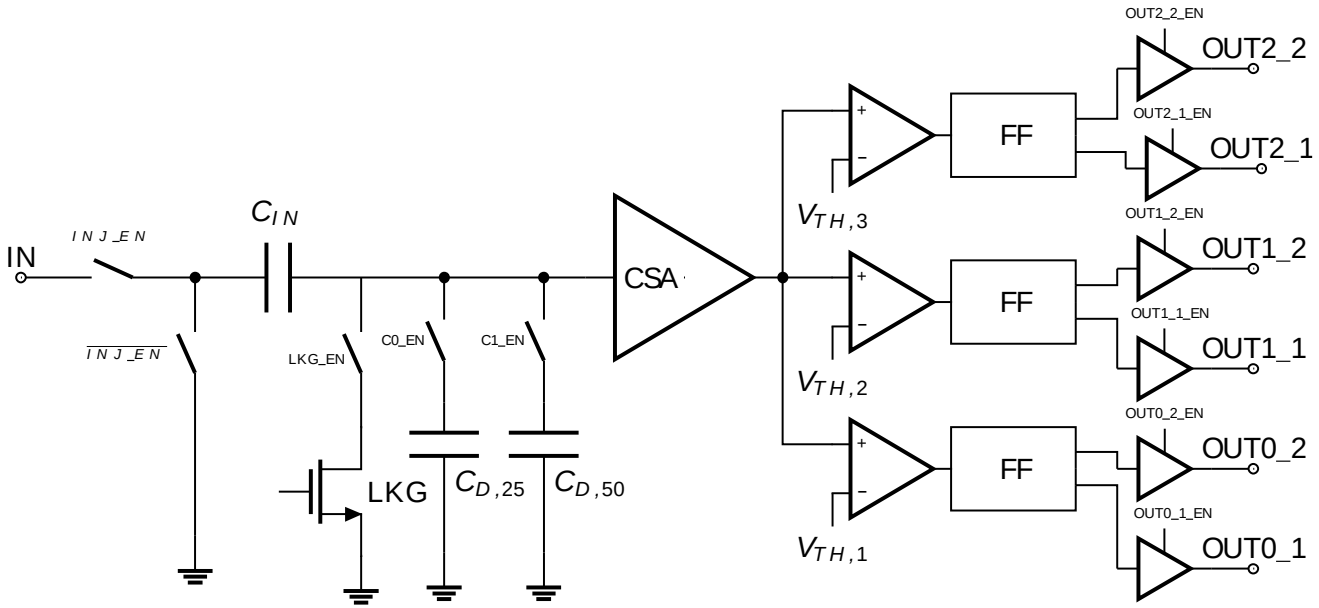
- **Flash ADC** based front-end → preamp + AC coupled bank of auto-zeroed comparators implementing a 2-bit flash A/D conversion

  Zero dead-time analog channel for high rate applications

  (non negligible probability of having hits in adjacent bunch crossings)

Flash ADC based front-end



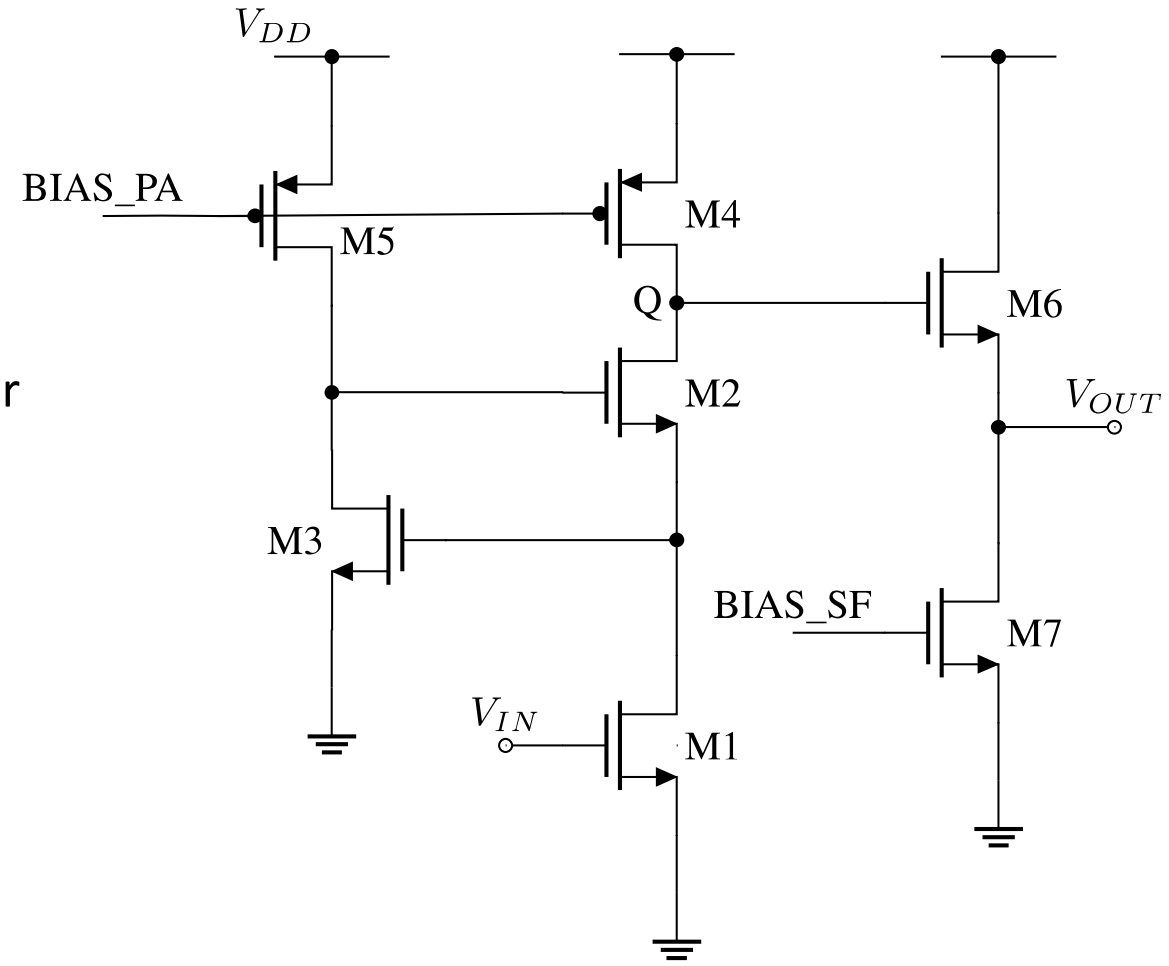


- **Equivalent noise charge @ preamp output** about 65 e rms for Cd =50 fF at – 20 °C
- Compensation of at least 50 nA sensor leakage current

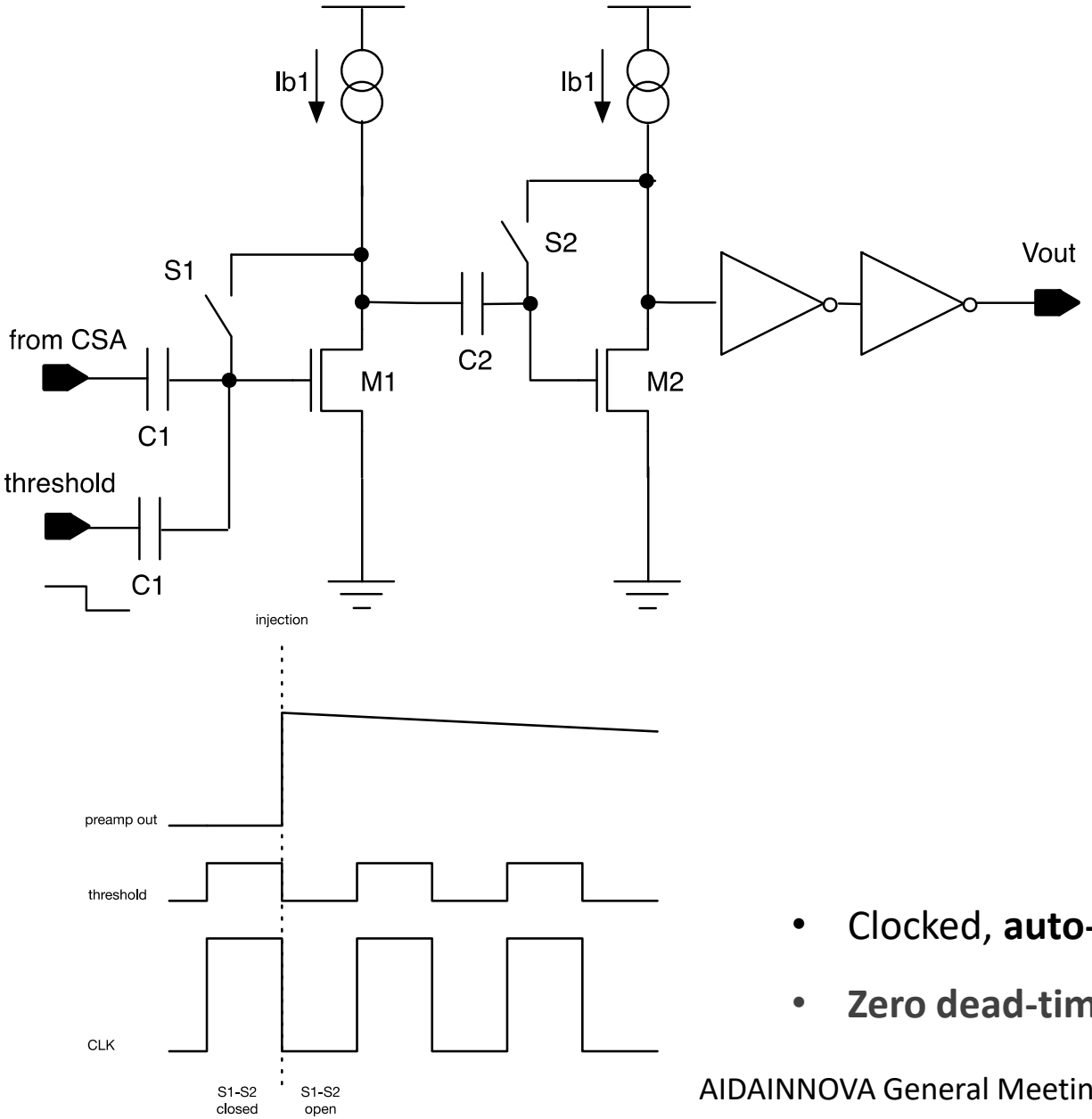
- AC coupled comparators implementing a **2-bit flash ADC**
- **Auto-zeroed comparators**, operated with 40 MHz clock. The implementation is ideally insensitive to device threshold voltage mismatch → threshold tuning DAC not required
- Overall **current consumption**: 5.4 uA → 4.9 µW **power consumption** @ V_{DD}=0.9 V
- Elementary cell size: 25 x 50 µm^2 (analog+digital)
- Minimum **in-time threshold**: 600 e-

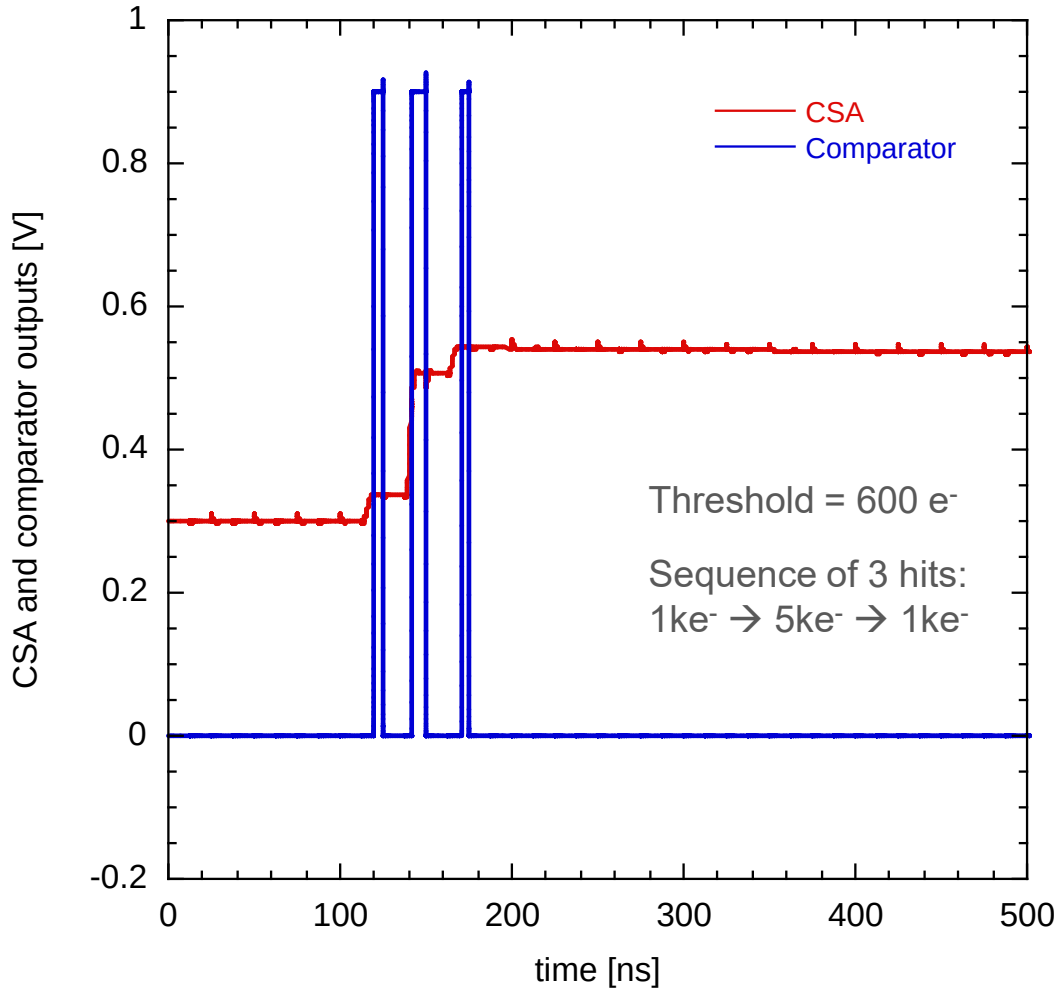
Flash ADC based front-end: preamplifier gain stage

Regulated cascode + source follower buffer
(input transistor W/L = 4.5 / 0.3)



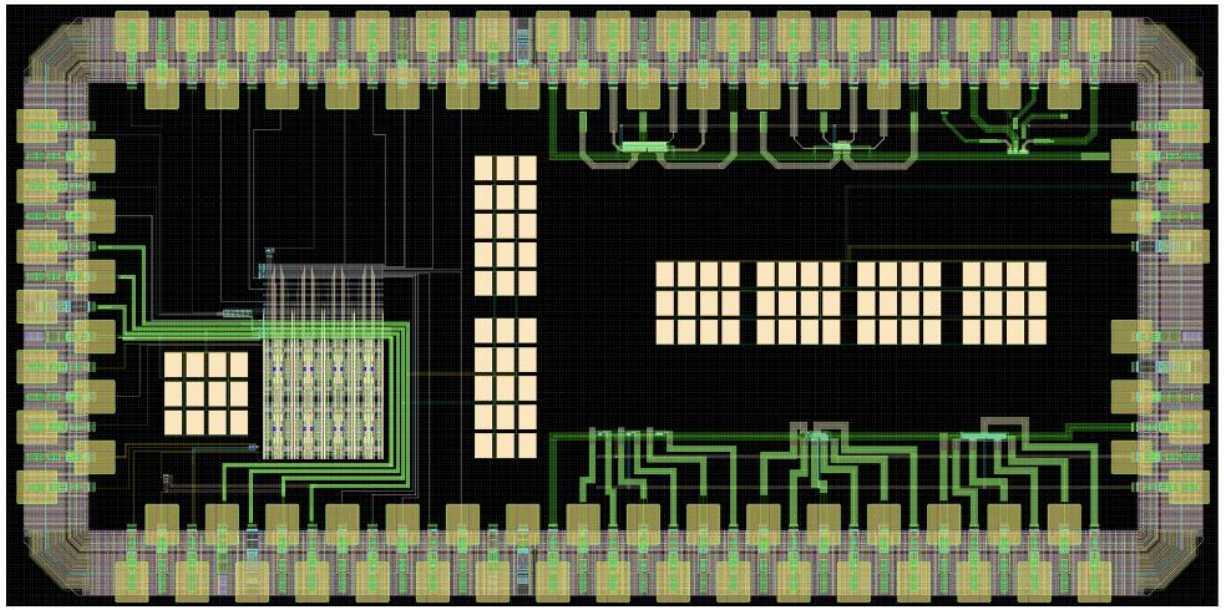
Flash ADC based front-end: comparator

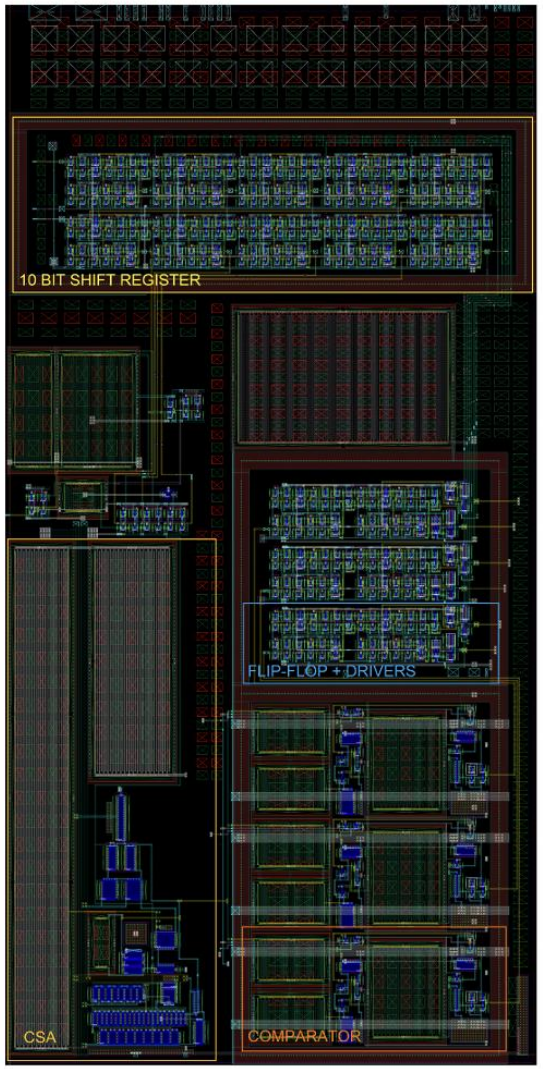




- Clocked, **auto-zeroed** comparator featuring low power consumption (700nW)
- **Zero dead-time**, low threshold dispersion (< 35 e r.m.s.)

Flash ADC based front-end





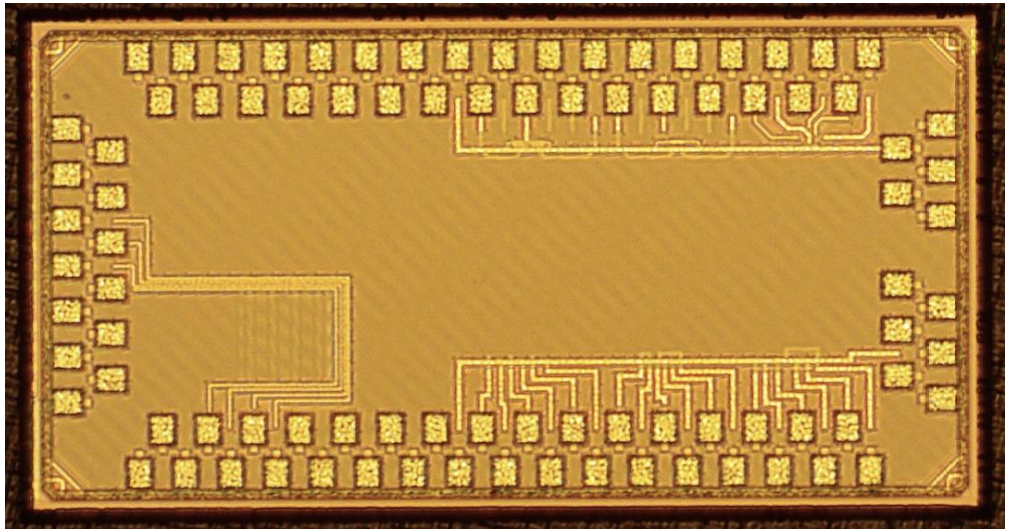
25 x 50 µm^2 pixel cell

Each pixel in the matrix is equipped with auxiliary circuits including:

- Two capacitors (25 and 50 fF) emulating the detector cap, which can be independently connected to the preamp input
- Detector leakage emulator circuit
- Injection circuit

- **Prototype chip including a 4x8 readout matrix** has been submitted in a mini@sic run in October 2022
- Simple digital configuration and readout (shift registers)
- Analog bias generated on the PCB (no on-chip DACs)

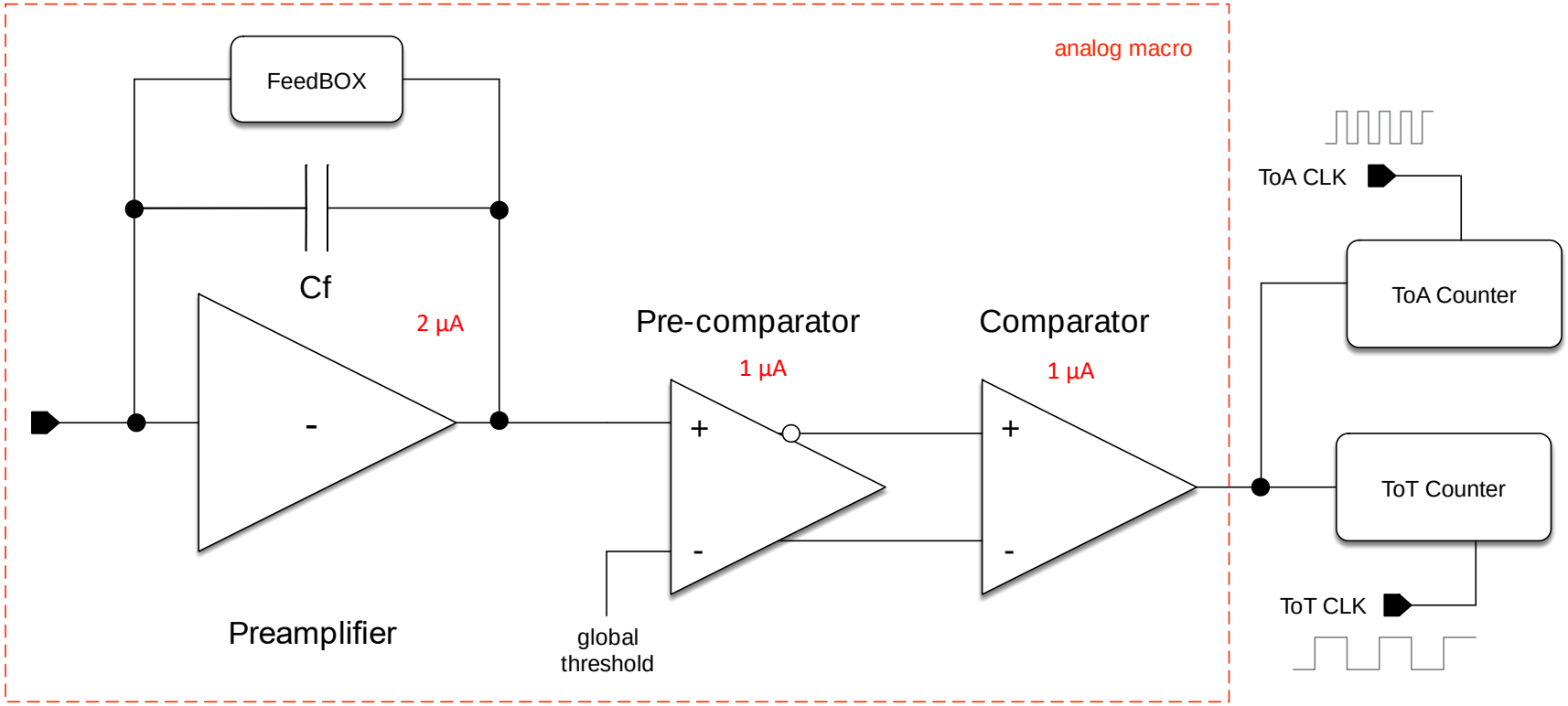
Flash ADC based front-end



- We received 100 bare chips including a 4x8 matrix of 25x50 pixels with **Flash-ADCs**
- Prototype chip includes standalone NMOS and PMOS transistors for static and noise characterization
- **Testing beginning now**

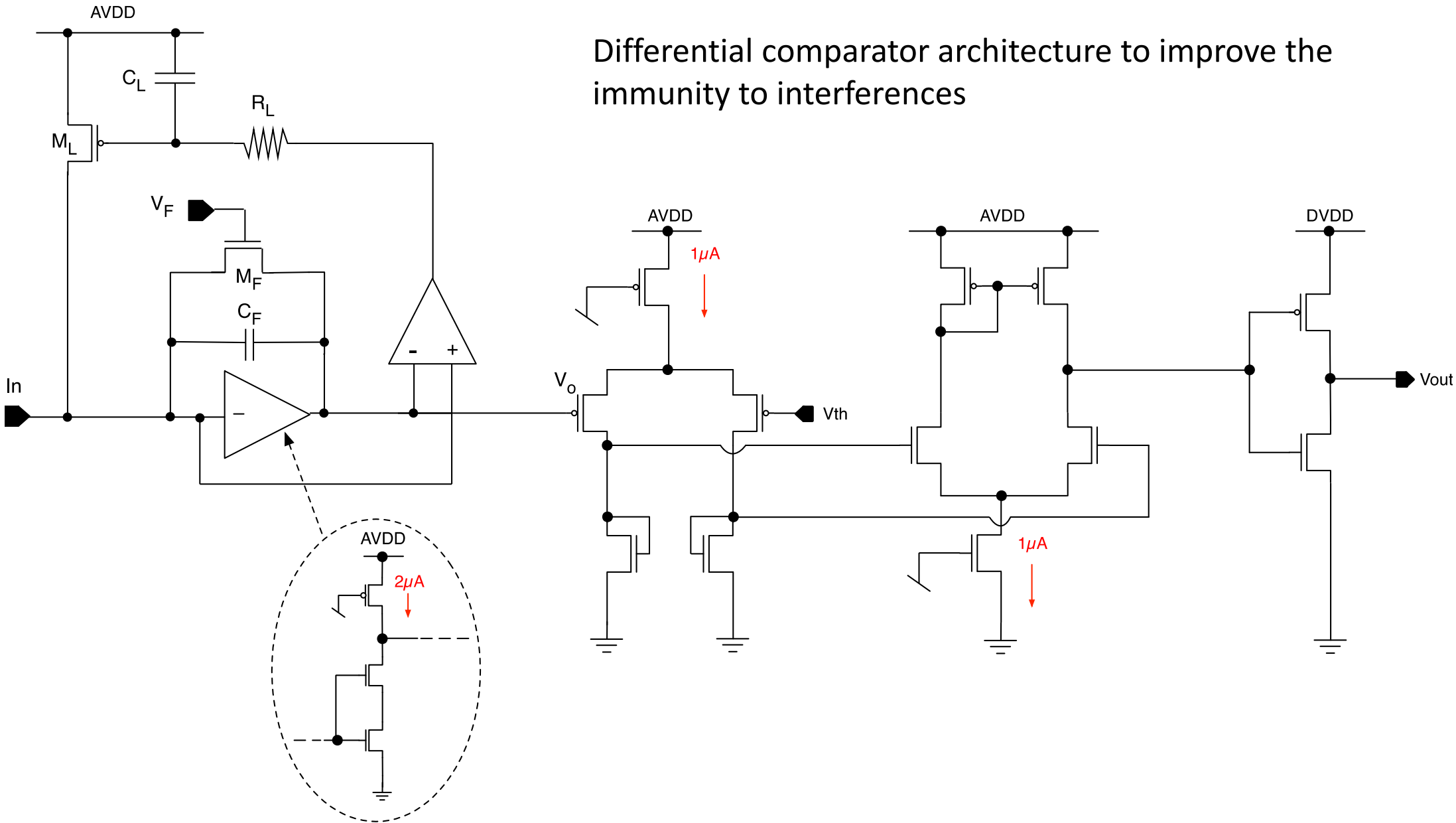
ToT-based front-end design

- **Front-end architecture optimized for low threshold (**< 500 e-), based on **Time-over-Threshold (ToT) A/D conversion** → preamp + DC coupled comparator + **5/6-bits** threshold tuning DAC



ToT-based front-end design

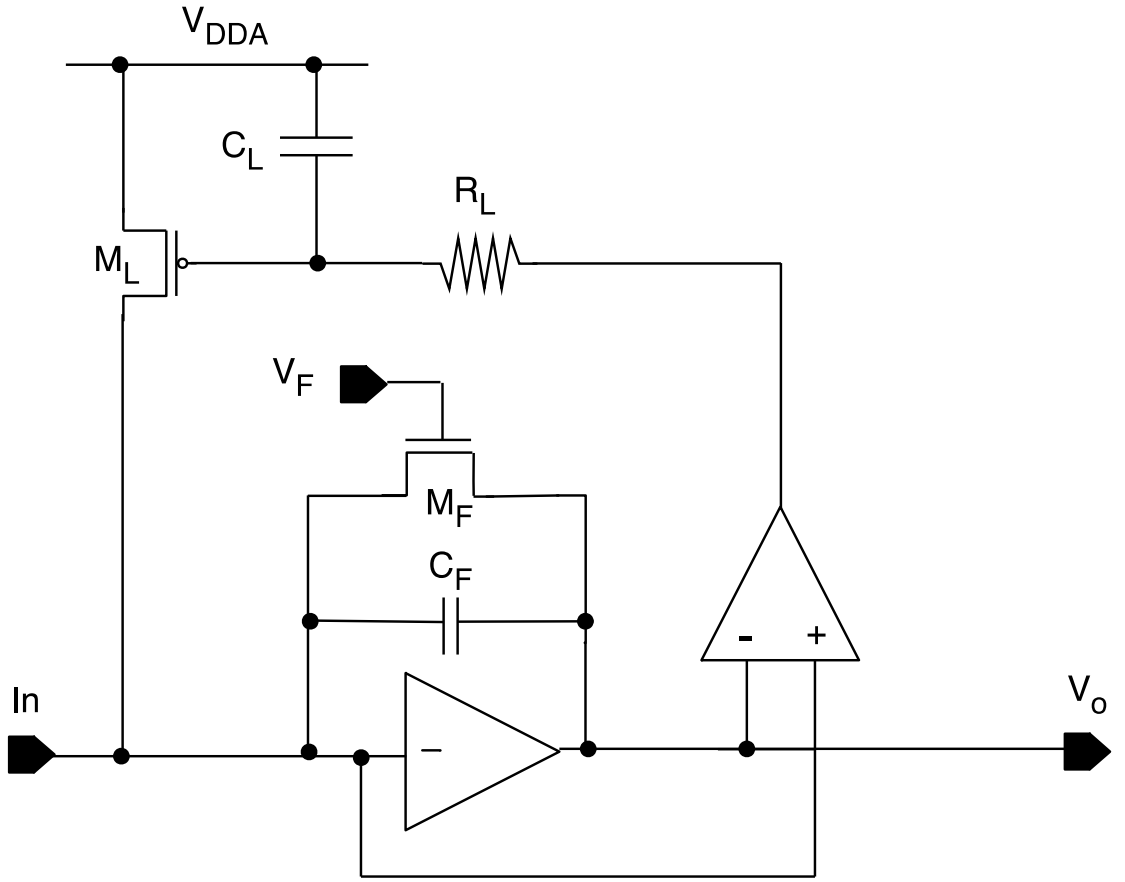
Differential comparator architecture to improve the immunity to interferences



ToT-based front-end specifications

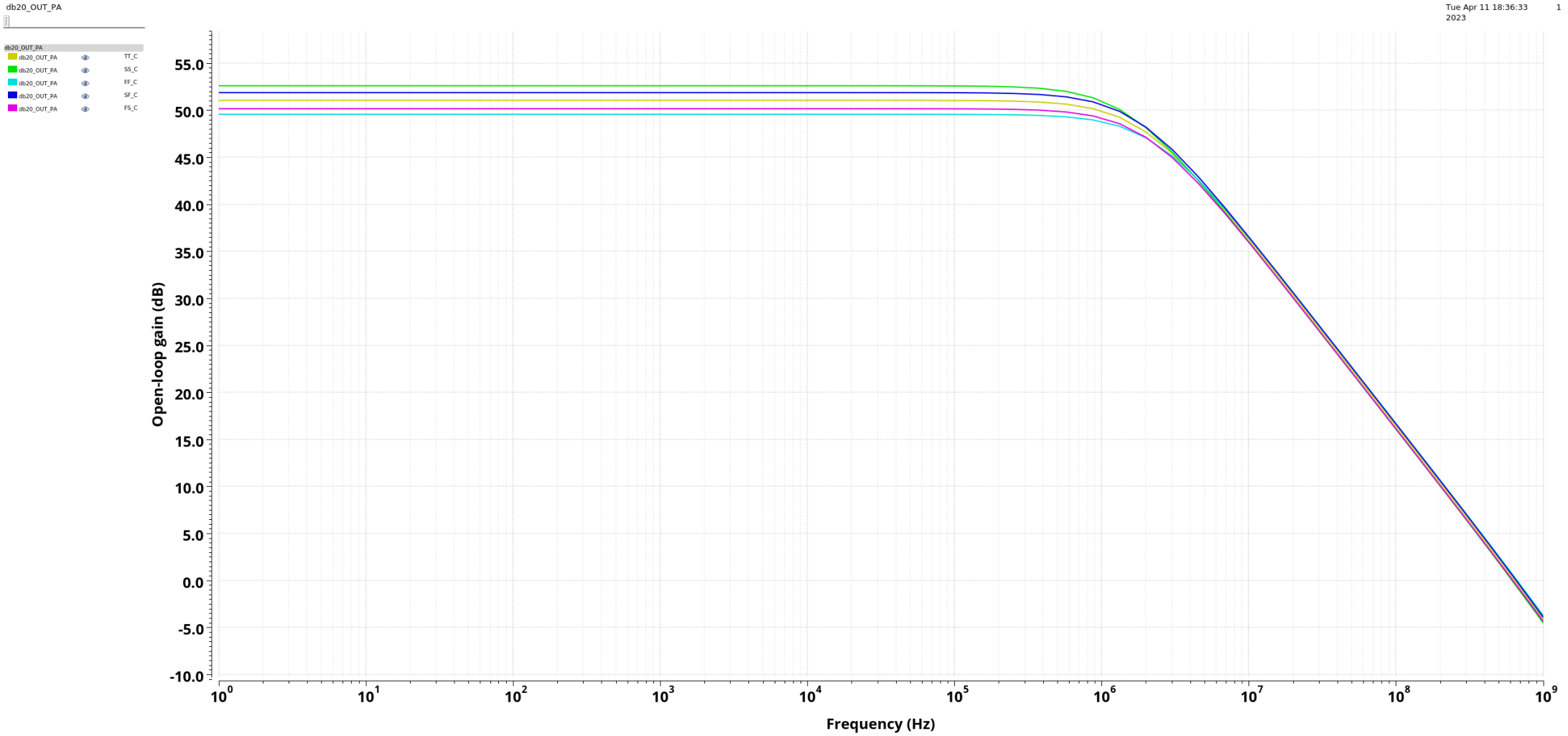
- Elementary cell size: 25 x 100 μm^2 (analog+digital)
- Per-pixel analog current consumption < 5 µA
- Minimum threshold < 500 e-
- Radiation TID > 1 Grad
- *Analog island* layout arrangement as in RD53
- Isolation of analog circuits: Single DNW
- Compensation of at least 50 nA sensor leakage current

Charge sensitive amplifier



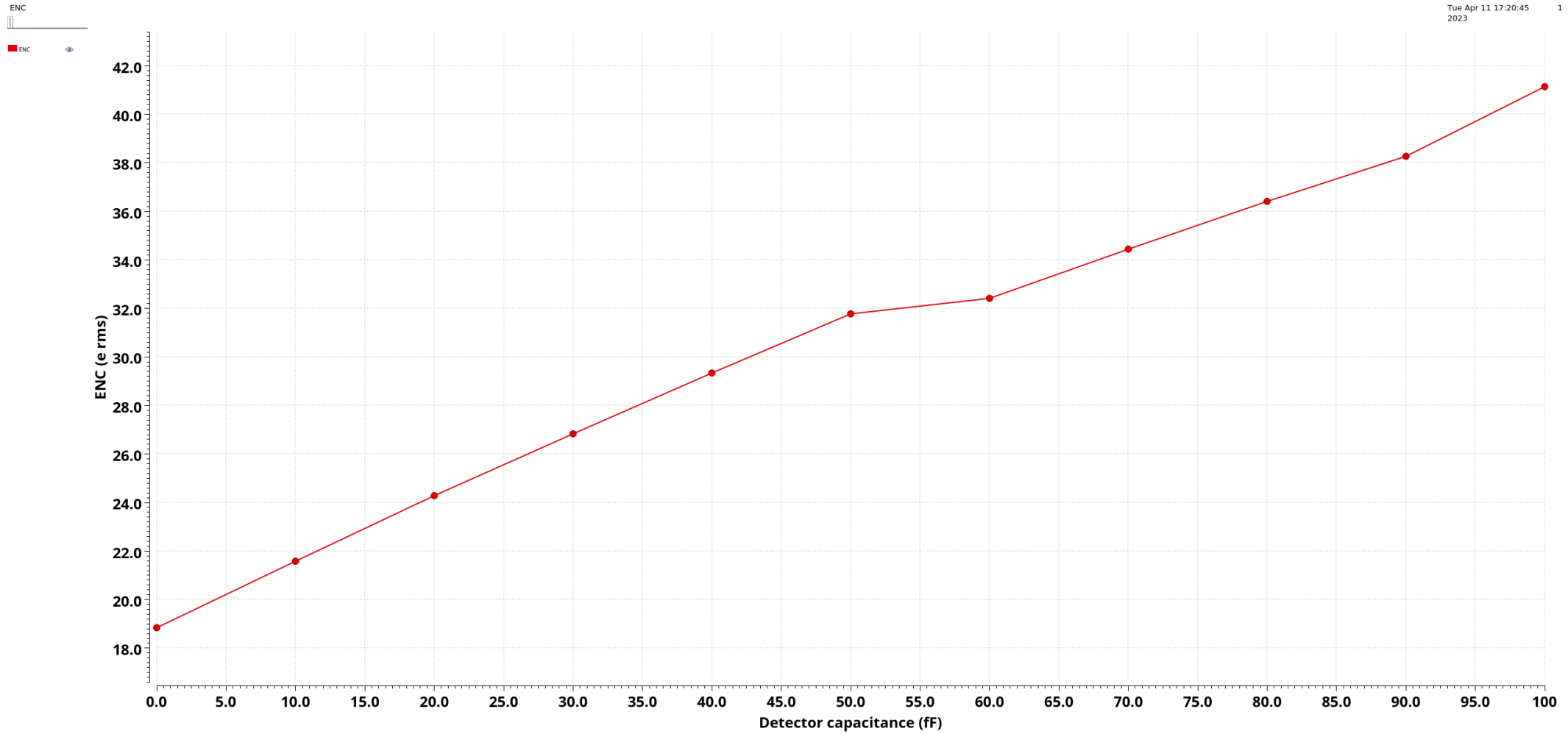
- Gain stage based on self-cascode architecture
- Two independent feedback loops: fast for signal integration, slow for sensor leakage current compensation
- RL implemented by means of an NMOS with shorted G and S
- Designed charge sensitivity of 25 mV/ke-

Open-loop gain



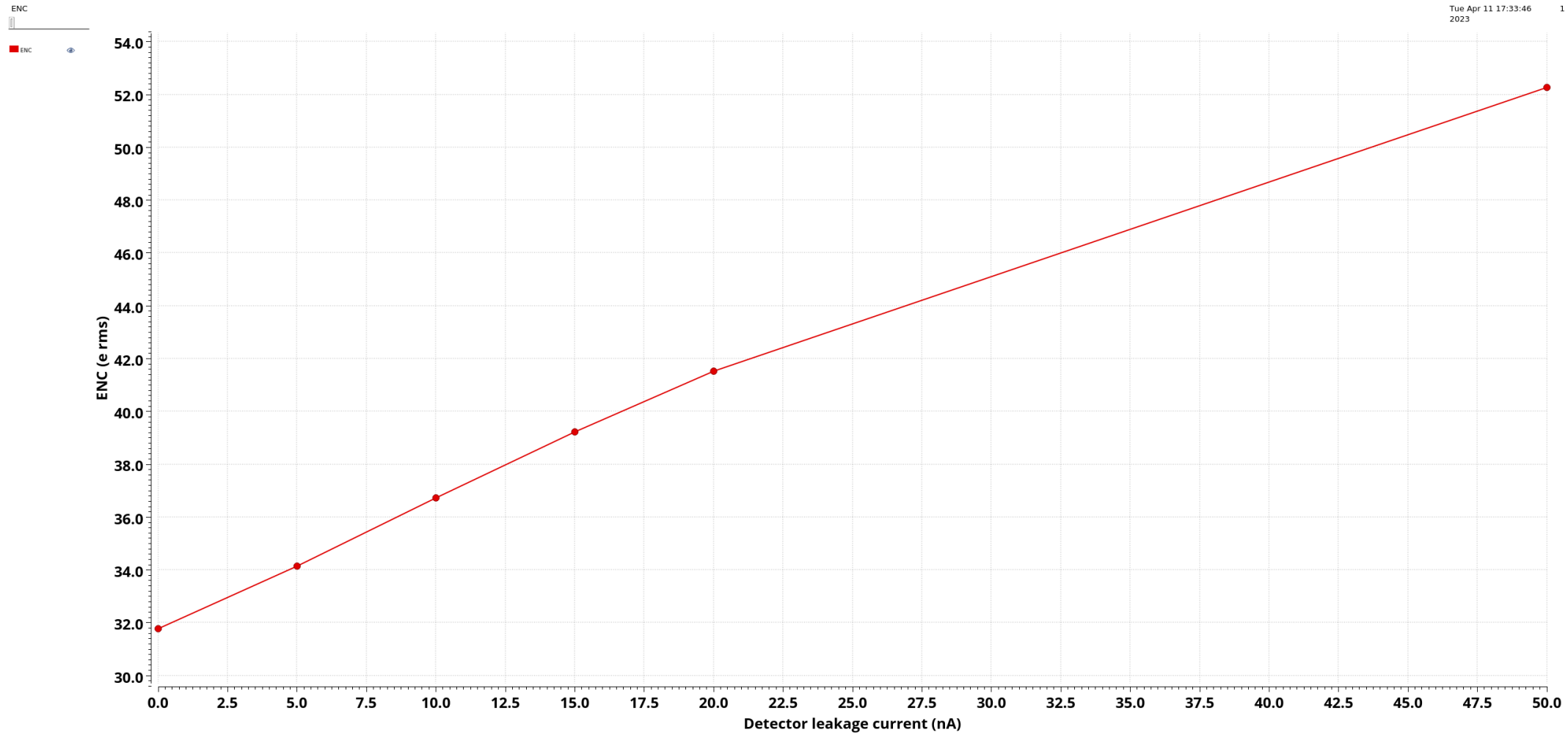
- A_0 ~ 52 dB in the TT corner
- Cut-off frequency around 2 MHz

ENC vs detector capacitance



- ENC ~32 e rms @ CD = 50 fF (simulation for T= - 20°C)

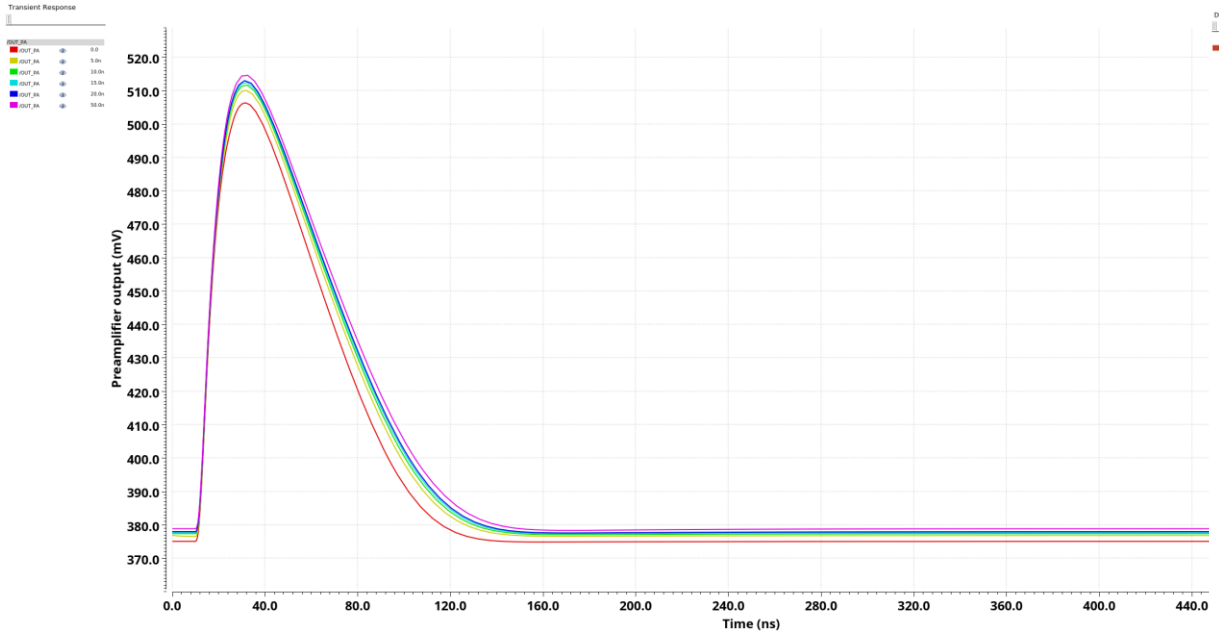
ENC vs detector leakage



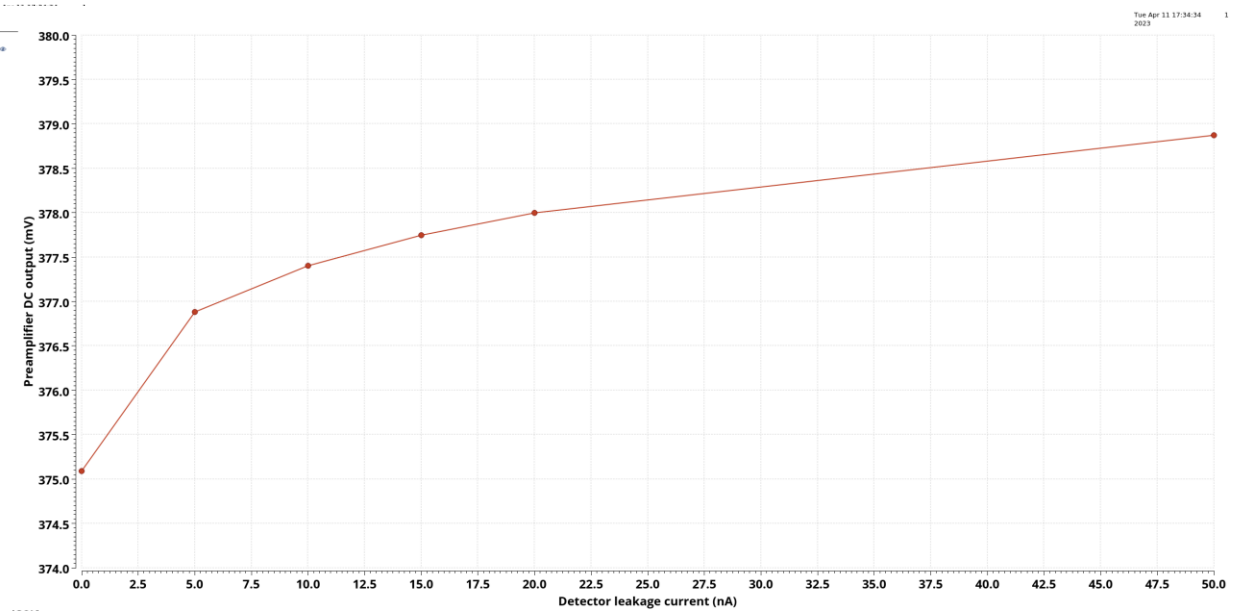
- Equivalent noise charge for detector leakage current up to 50 nA, for CD=50 fF
- Significant (~60%) increase in the ENC at 50 nA

Leakage compensation

Preamp out in response to Qin=6 ke

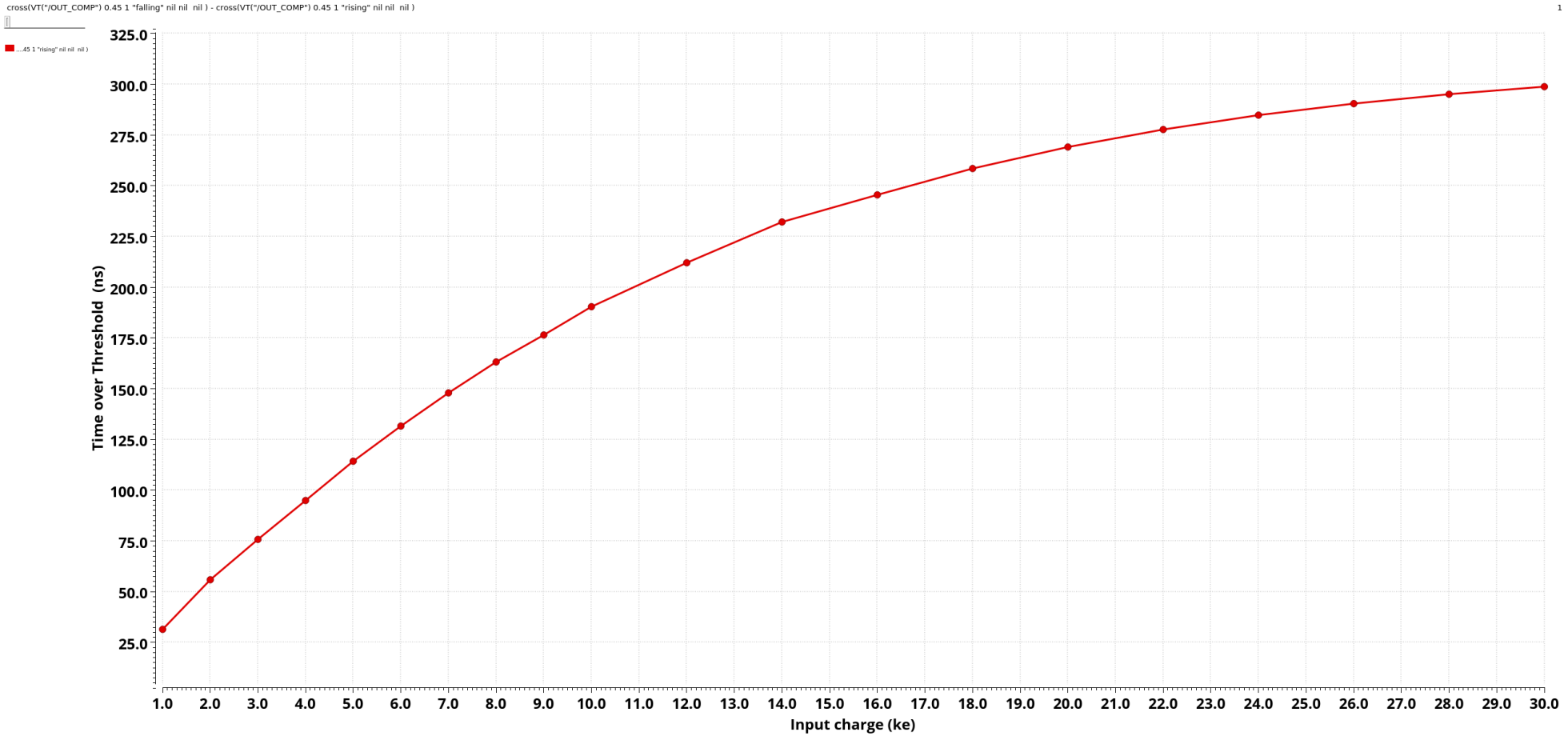


Preamp DC out vs detector leakage current



- Preamplifier output waveform not significantly affected by leakage up to 50 nA
- Slight (~4 mV) increase in the preamp DC output

Time-over-Threshold



- Time-over-Threshold as a function of the input charge
- ~ linear behavior up to Qin=10 ke$^-$

Conclusions

- **Two different AFEs** are being investigated in a 28 nm CMOS technology:
  - **ToT** A/D conversion
  - **Flash** A/D conversion

- **Flash-ADC based front-end matrix and test structures ready for testing**

- **Submission in October 2023 (mini@SIC):**

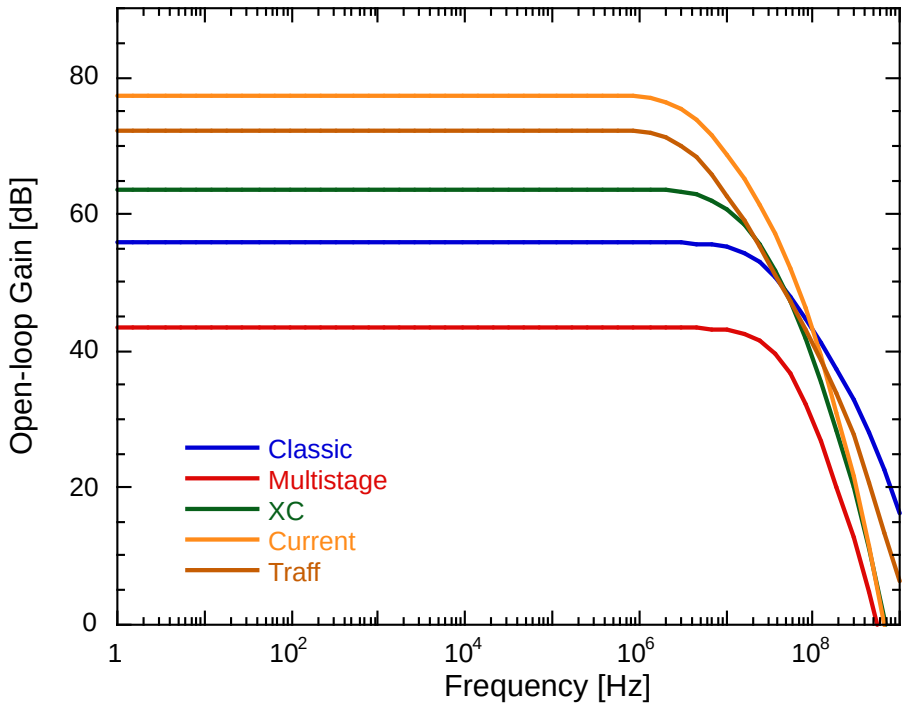
  ToT - based front-end in a 32x16 matrix of 100x25 µm^2 pixels

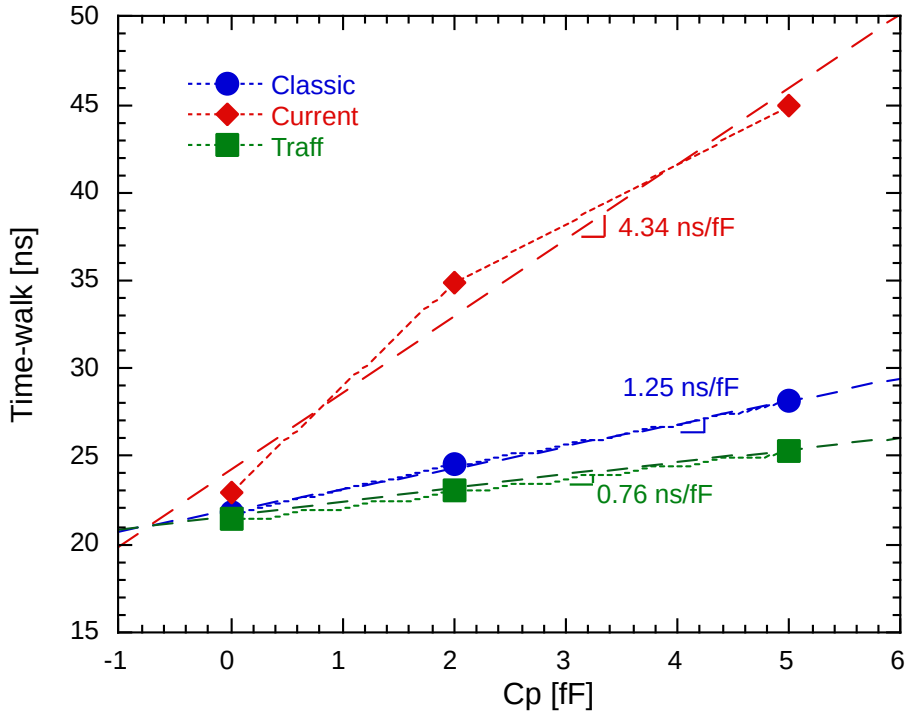
  digital logic will be designed by Davide Falchieri (INFN Bologna) with the support of Alberto Stabile and Luca Frontini (INFN Milano)

Backup slides

ToT-based front-end: threshold discriminator

- Different comparator architectures have been investigated
- Overall **time-walk** shown for three comparator versions
- Schematic-level simulations (ideal preamp with 20 ns peaking time)
- **Parasitic capacitance** (Cp) added to the main nodes of the comparators





Falaphel project

- **INFN funded project (CSN5)** 2021-2023 (830 kEuros, 35 people and ~13 FTE)

- **Participant institutes:** INFN Padova, INFN Pavia, INFN Pisa, Scuola Superiore S. Anna di Pisa, Dip. Ingegneria Informazione UniPisa. Dip. Fisica UniMilano. (P.I. Fabrizio Palla)

- **Goal**: Development and integration of Silicon Photonics modulators with high speed, rad-hard electronics in 28 nm

- **Focus of Pavia/Bergamo:**
  - Analog Front-end design
  - IP blocks (Bandgap, …)