AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Update from AGH
WP11.2 – CMOS 28 nm

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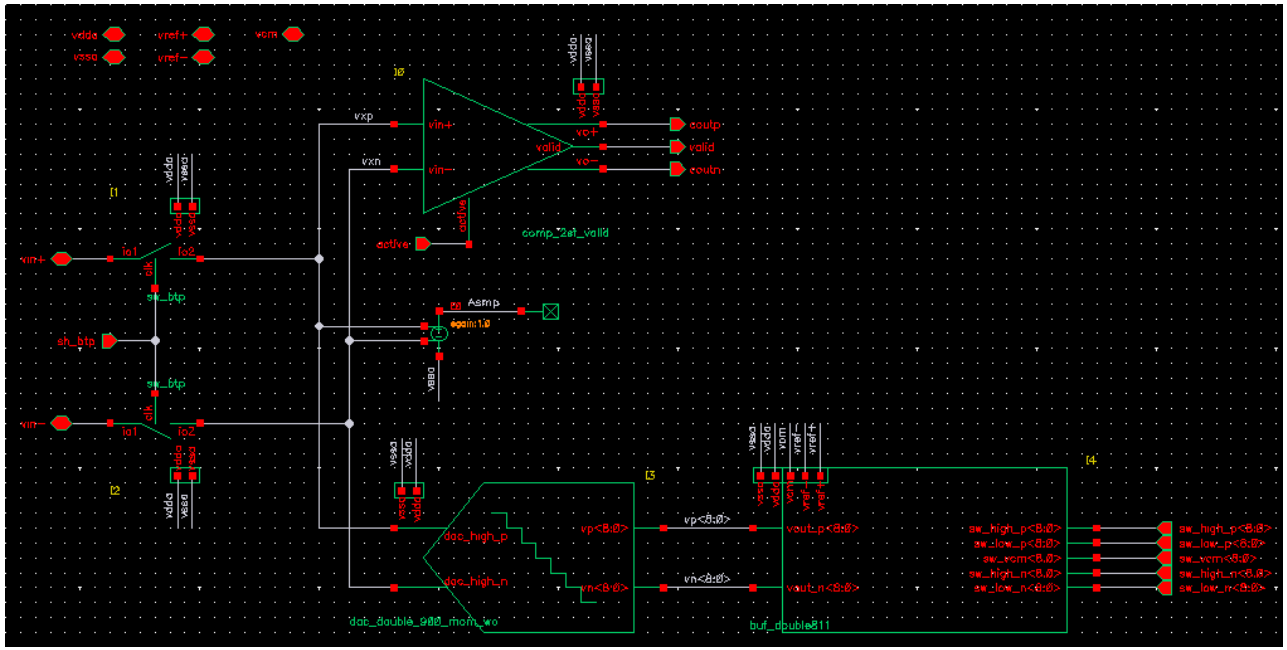
Quick summary

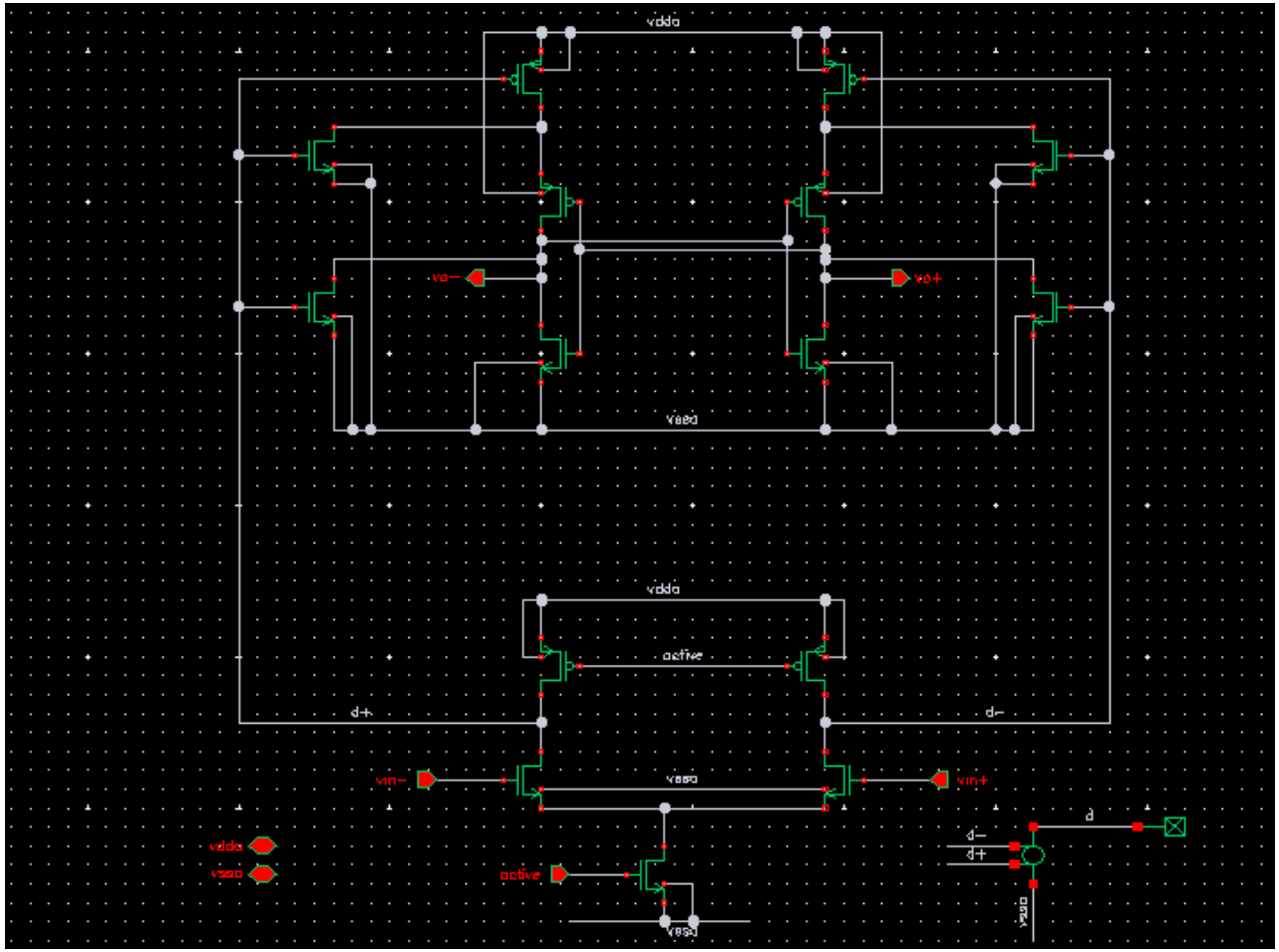
- Activities in TSMC CMOS 28nm
  - Long process with NDA, signed in 2021/2022
  - Design kit obtained&installed 2022
  - Understanding the process 2022
  - First design of fast ultra-low power 10-bit ADC started in 2022
  - ADC design in progress…., although slower than expected

Activities in TSMC CMOS 28nm
Design of fast ultra-low power 10-bit SAR ADC

- Standard SAR architecture chosen, which worked very well in CMOS 130 nm and 65 nm,
- Fully differential, MCS switching scheme, asynchronous logic,...
- The goal (apart from obvious ultra-low power) – is it possible to get sampling rate ~200MSps, using such simple architecture ?



Activities in TSMC CMOS 28nm
10-bit ADC – dynamic comparator



2-stage dynamic comparator

- Two versions of dynamic comparator designed and simulated 2-stage and 3-stage
- Layout of 2-stage comparator completed and verified in post-layout simulations

Activities in TSMC CMOS 28nm 10-bit SAR ADC – design status

- Schematic of analog part (bootstrap switch, comparator, capacitive DAC, buffers for DAC) completed and verified in simulations
- Layout of bootstrap switch and comparator completed and verified in post-layout simulations
- SAR logic and DAC layout in progress...