AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Update from AGH WP11.3 130/65 nm

Marek Idzik for AGH-UST

AIDAinnova 2nd Annual meeting, 24-27 April 2023, Valencia

Outline

FLAME ASIC in 130nm for calorimetry

FLAXE ASIC in 130nm for ECAL in LUXE experiment

Precise TAC-based TDC in 130nm

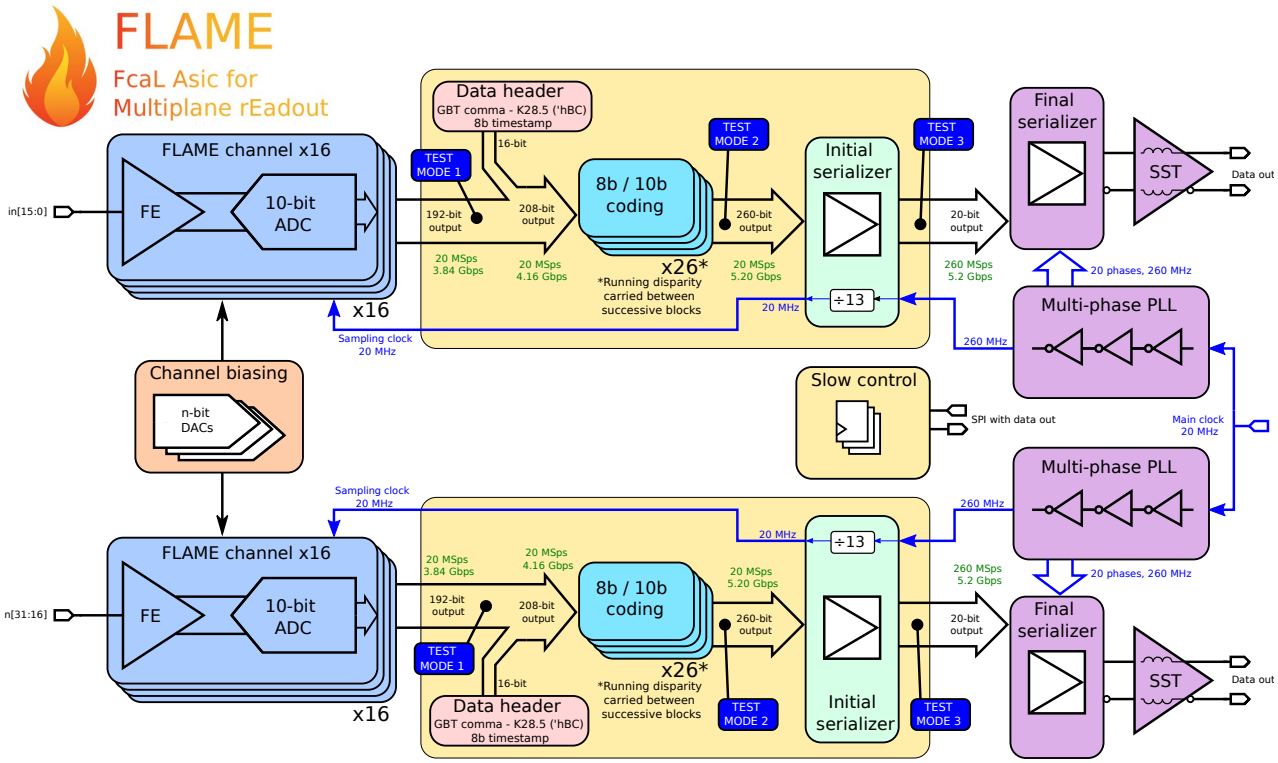
Fast Serializer&Transmitter in 130nm and 65nm

lpGBT monitoring subsystem in 65 nm

Test setups for ADCs in 130nm and 65nm

New publications

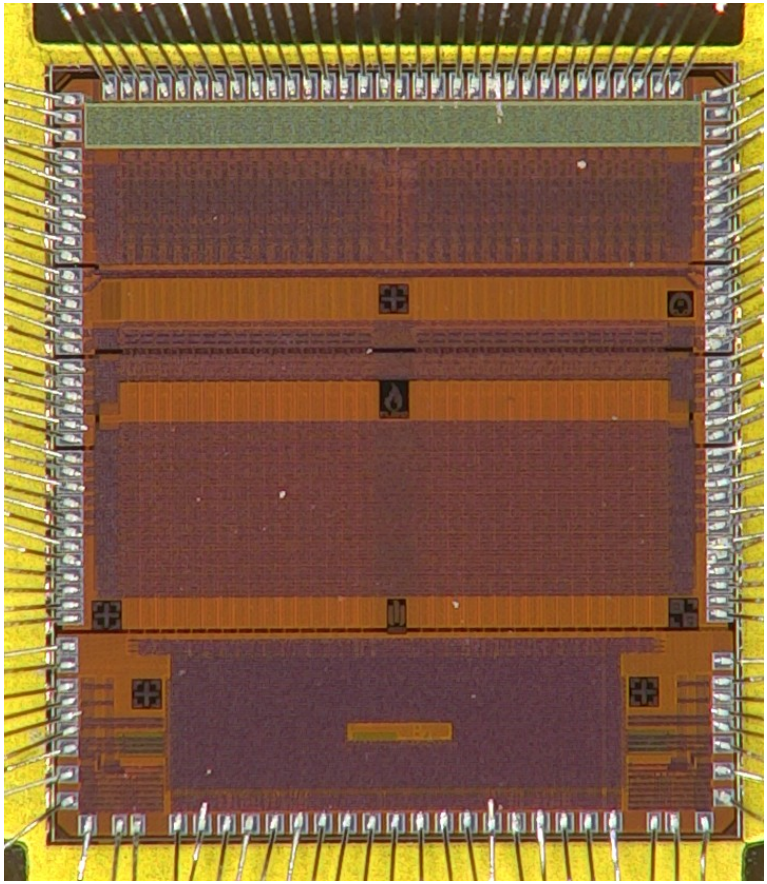
Activities in TSMC 130nm FLAME ASIC for calorimetry



- FLAME is a 32-channel ASIC in CMOS 130nm with analog front-end (T_{peak}~50ns, switched gain), and 10-bit ADC (f_{sample}=20MHz) in each channel, followed by two fast (~5Gbps) serializers and data transmitters

Activities in TSMC 130nm
FLAME & FLAXE ASICs in LUXE experiment

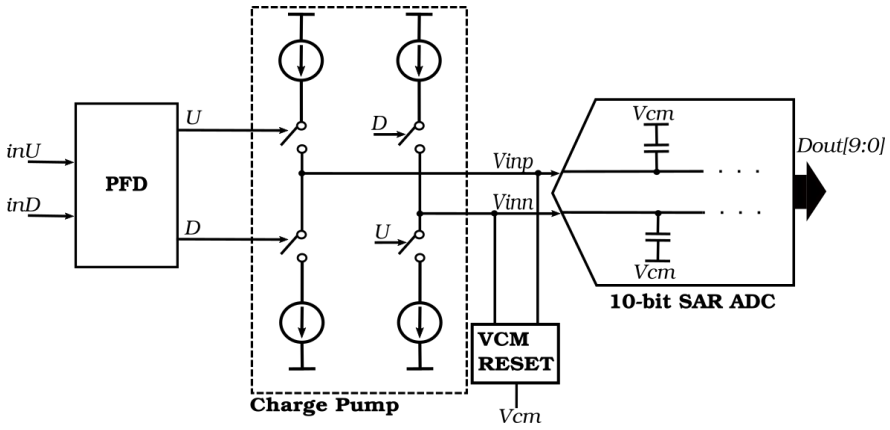
- For ECAL detector in LUXE experiment a new FLAME-based chip called FLAXE (FLAME with much lower data transmission rate) was designed
- Presently FLAME chips are used for first LUXE test-beams. In the last test-beam at DESY, 11-18 September 2022, a 4-chip front-end board (128 channels) was used to study the performance of Si and GaAs sensors and shower development. A lot of data was collected – analyses in progress…
- FLAXE ASIC has been just submitted for production

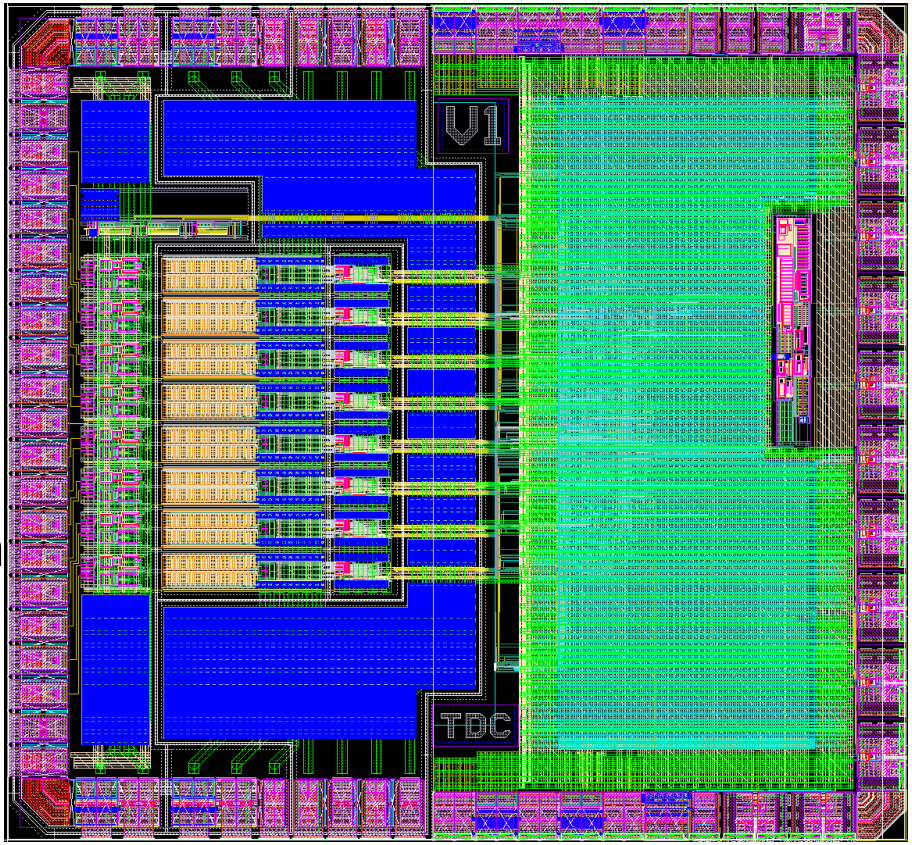


FLAME

Activities in TSMC 130nm
R&D on precise TDC (~10ps) in CMOS 130nm

Single TDC channel



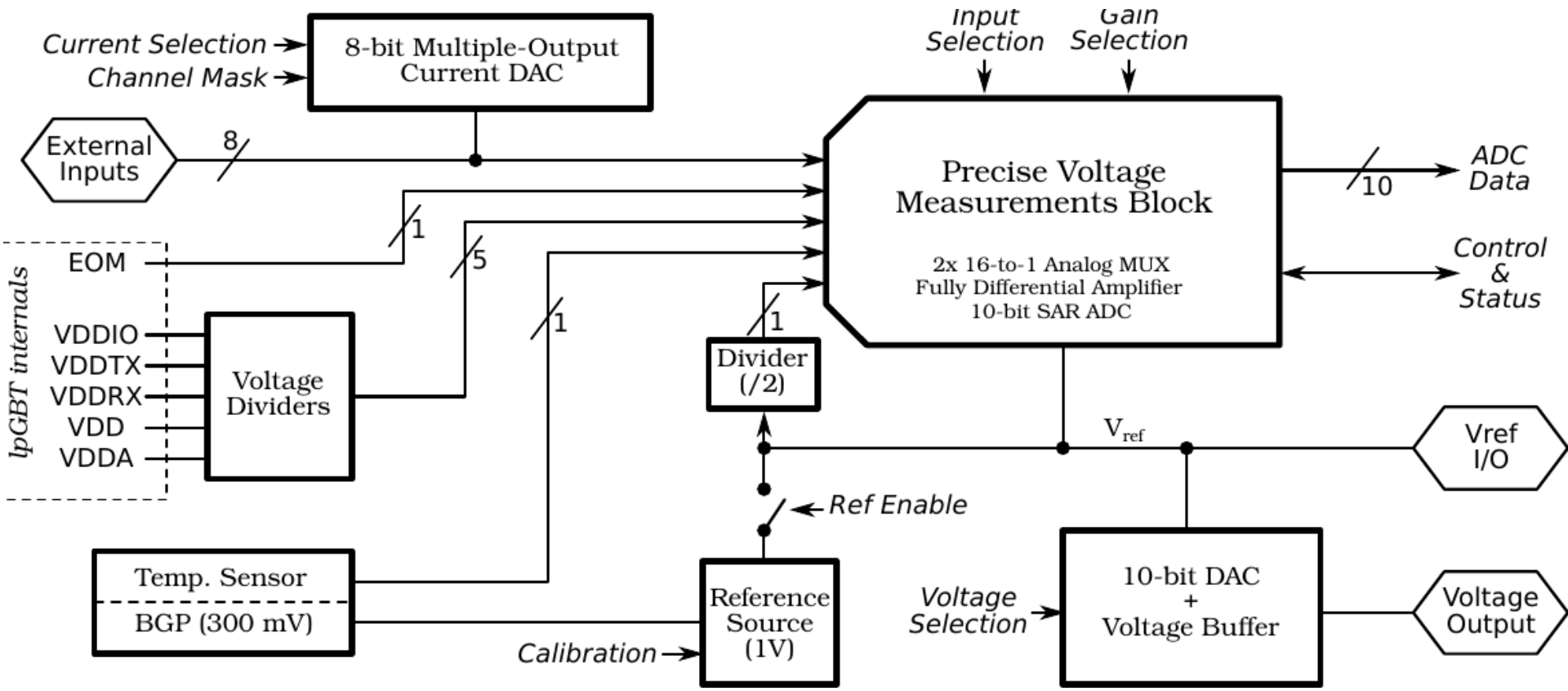


- New TAC-based TDC aiming with timing measurement precision of ~10ps, consuming ~1mW per channel, was designed
- 8-channel prototype TDC chip was produced 2022
- Test setup in progress...

Activities in TSMC 130/65 nm
Fast Serializer&Transmitter in 130nm and 65nm

- Prototype Serializer&Transmitter in CMOS 130nm (~5Gb/s) and CMOS 65nm (~10Gb/s) were designed and fabricated some time ago.
- Serializer&Transmitter in 130nm is part of the FLAME chip and it was already found functional in lab and test-beam, but important parameters like BER (Bit Error Rate) were not yet measured precisely
- Dedicated test setup to characterise both prototypes of Serializer&Transmitter chip is almost completed...

Activities in TSMC 65 nm lpGBT monitoring subsystem



Tests of lpGBT monitoring subsystem finished in 2023

Activities in TSMC 130/65 nm
Test setups for ADCs in 130nm and 65 nm

- Prototype 12-bit ADCs in 130 nm and 65 nm, and improved 10-bit ADC in 65 nm, are still waiting for tests...
- New PCBs and entire test-setup are needed, in progress...

New publications

An lpGBT Subsystem for Environmental Monitoring of Experiments

lpGBT collaboration

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Abstract: In this paper, the Low Power Giga Bit Transceiver (lpGBT) built-in system for environmental monitoring of the LHC experiments is presented. Eight external analogue inputs and eight internal voltages are multiplexed into an instrumentation amplifier with selectable gain, whose output is digitised by a 10-bit SAR ADC. A programmable current source can be enabled for each external input to implement resistance measurements. Internal channels are used to monitor power supplies and the output of the temperature sensor. The environmental monitoring system includes a precise 1 V reference voltage source and a 10-bit voltage DAC. All blocks were designed and fabricated in 65 nm CMOS technology, fully characterised, and the pre- and post-irradiation measurement results are presented in this work.

JINST - just accepted

An Ultra-Low Power 10-bit, 50 MSps SAR ADC for Multi-Channel Readout ASICs

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Abstract: The design and measurement results of a fast, ultra-low power, small area 10-bit SAR ADC, developed for multi-channel readout systems, in particular for applications in particle physics experiments, are discussed. A prototype ASIC was designed and fabricated in 130 nm CMOS technology and a wide spectrum of static (INL < 0.4 LSB, DNL < 0.3 LSB) and dynamic (ENOB = 9.45) measurements was performed to study and quantify the performance of ADC. The ADC converts analogue signals with a sampling frequency up to 55 MHz and power consumption below 1 mW. The ADC works asynchronously, so no external clock is required. The ADC Figure of Merit (FOM) at 50 MHz sampling frequency is 24 fJ/*conv.-step*, and is the lowest among the State of the Art designs with similar technology and specifications.

submitted to JINST

Publication on 80-90 MSps 10-bit ADCs in 65 nm almost completed...