OMEGA contribution in WP 11.3

AIDAinnova

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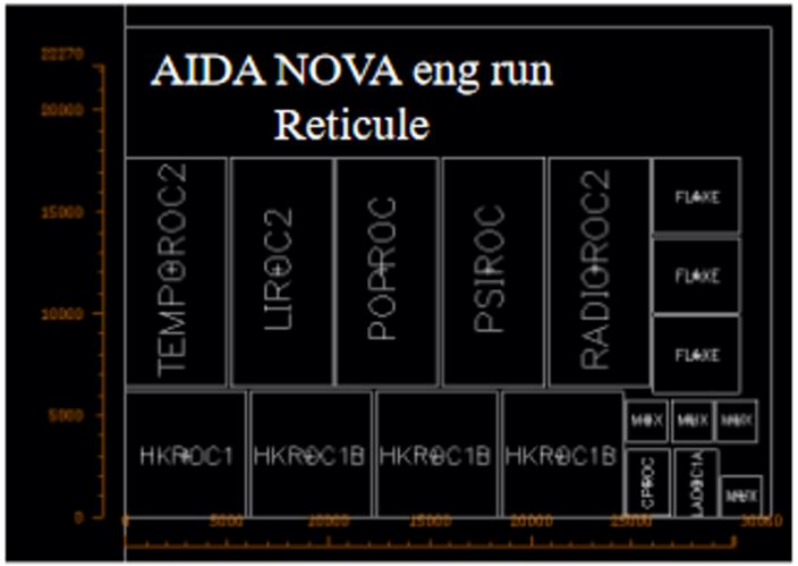
Organization for Micro-Electronics desiGn and Applications

Engineering run submitted this April 2023

- TSMC 130 nm
- 10 chips have been submitted
  - From OMEGA, AGH, IJCLAB, WEEROC
  - C4 (16 wafers) and WB (4 wafers), 90 chips/wafer
- HKROC1B and EICROC
- CPROC



chip	x	y		lab	unit area	#	total area	fraction	cost		rad tol
HKROC1B	5,96	6,16	C4	OMEGA	37,9	4	151,7	24,50%	73 415 €	# chips	Y
LADOC2B	3,243	2,142	WB	IJCLAB	7,5	16	119,9	19,30%	58 019 €	5760	Y
LIROC2	11,244	4,919	C4	OMEGA	56,9	1	56,9	9,20%	58 019 €	5760	Y
POPROC	11,244	4,919	C4	WEEROC	56,9	1	56,9	9,20%	58 019 €	1440	N
PSIROC	11,244	4,919	C4	WEEROC	56,9	1	56,9	9,20%	58 019 €	1440	N
RADIOROC2	11,244	4,919	C4	WEEROC	56,9	1	56,9	9,20%	58 019 €	1440	N
TEMPOROC2	11,244	4,919	C4	WEEROC	56,9	1	56,9	9,20%	58 019 €	1440	N
FLAXE	4,02	3,7	WB	AGH	15,7	3	47	7,60%	22 724 €	1080	Y
EICROC0	2,89	3	WB	OMEGA	9,3	1	9,3	1,50%	4 484 €	360	Y
CPROC	3,243	2,142	WB	OMEGA	7,5	1	7,5	1,20%	3 626 €	360	Y
Total					362,5	30	620,1	100%	300 000 €		

Hyper-Kamiokande detector and HKROC chip

The next generation of **neutrino** observatory in Japan (HyperK) will be built in **2026** with **260 kton** water Cherenkov detector**.** It will study **neutrinos** from **various sources**: solar, atmospheric, accelerator and Supernova neutrinos

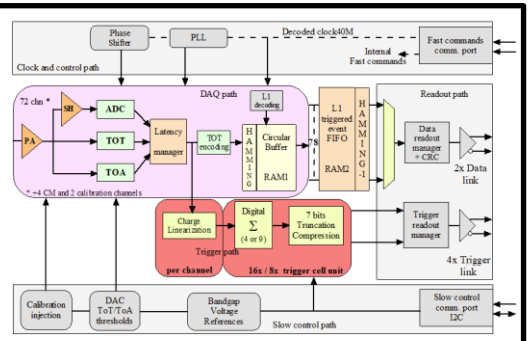
Based on HGCROC, HKROC will provide a versatile, low-power and fully integrated solution for large neutrino experiments

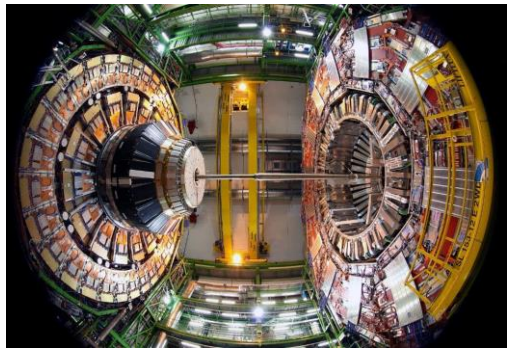
HGCROC for the CMS endcap calorimeter ar HL-LHC

6M of Silicon channels
(+ 240k of SiPM)

Radhard (200 Mrad)
Low Power (15 mW per chn)
Precise timing (25 ps)

Total of 150k ASICs needed
Pre-prod this year
Project started in **2017**

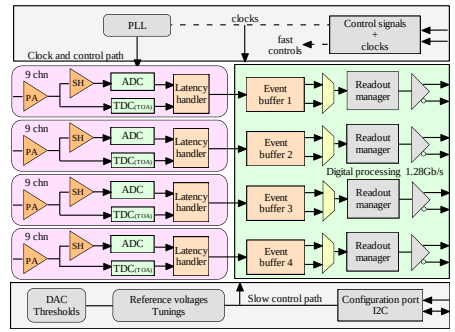


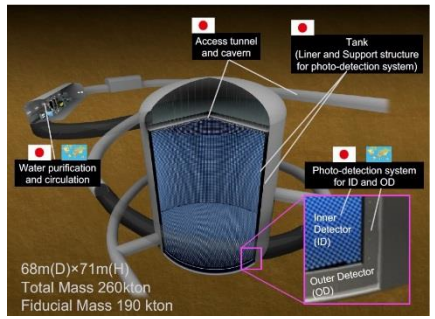


HKROC was developed in < 6 months

Same ASIC structure (floorplan)
Same ADC and TDC
Same readout

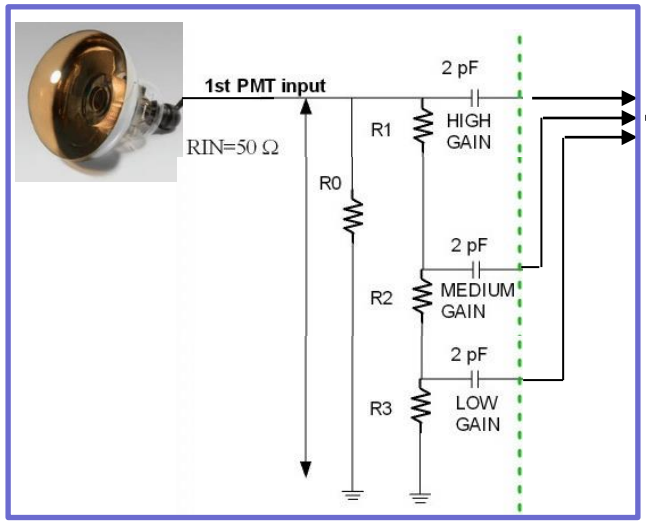
New preamplifier
New digital processing

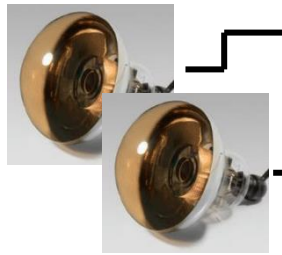


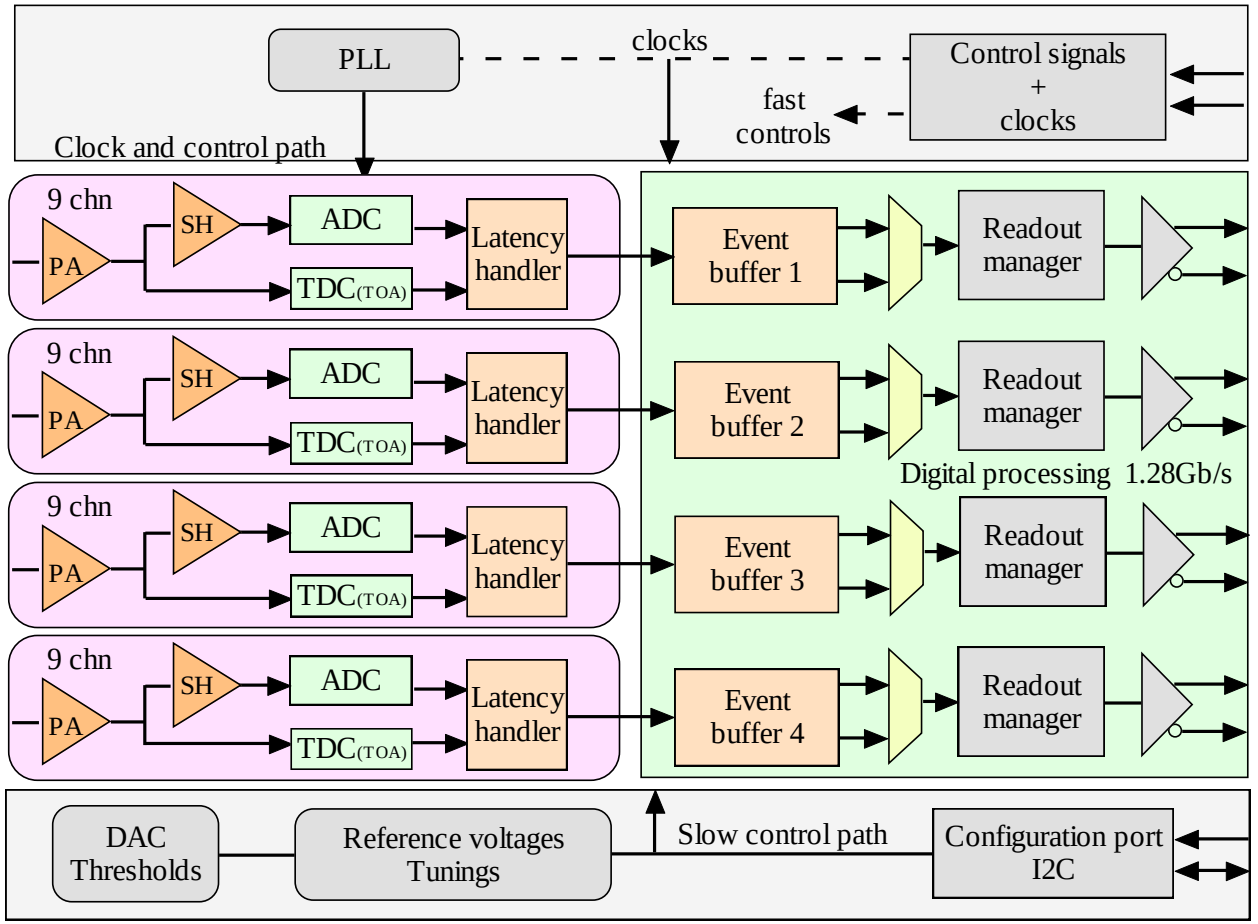


HKROC main features

- HKROC has 36 channels: 12 PMTs with High, Medium and Low gain
  - Or 36 PMTs with one gain



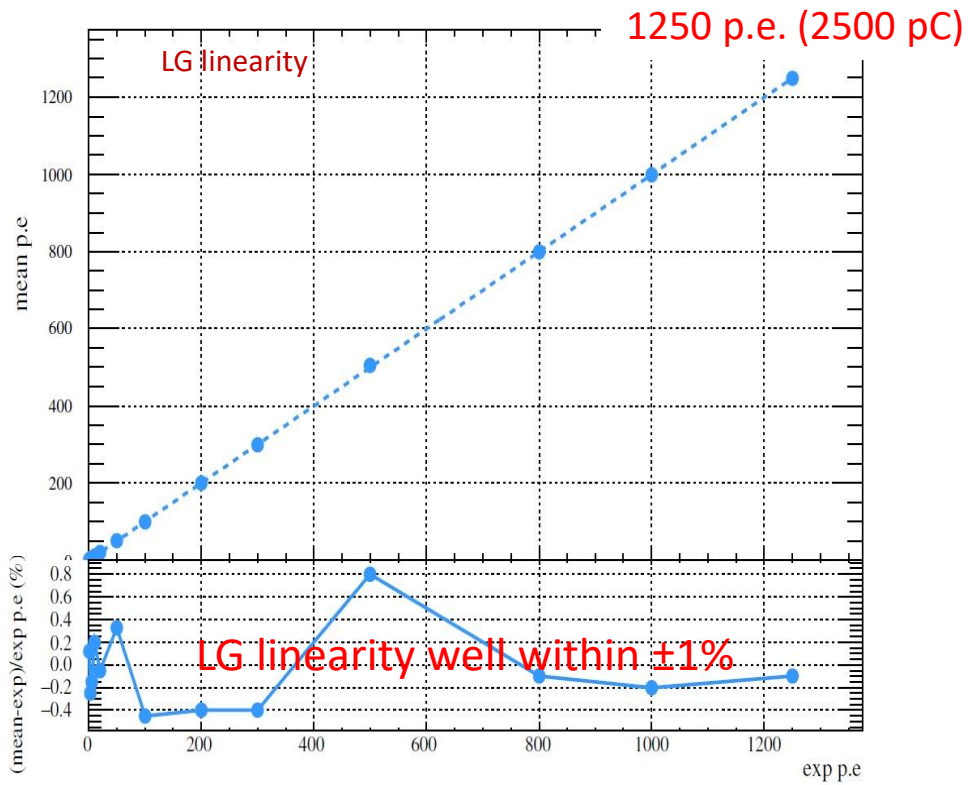


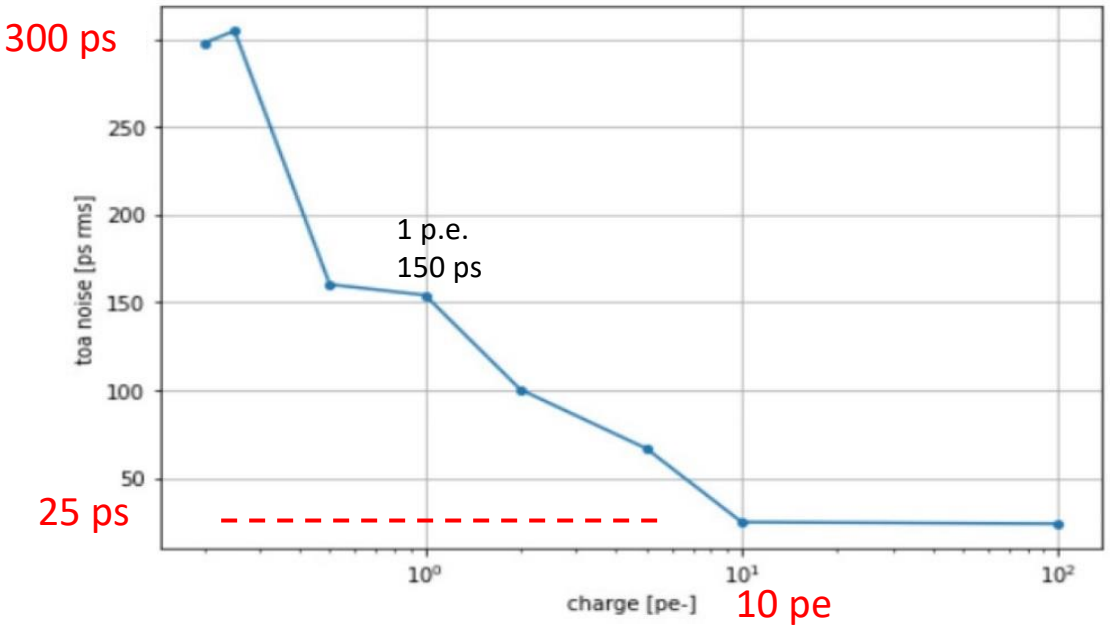


- ASIC in TSMC 130 nm node
- Low power: 10 mW per channel
- Large charge measurement with 3 gains (up to 2500 pC), < 1% linearity
- Integrated timing measurements (25 ps binning)
- Readout with high speed links (1,28 Gb/s), Hit rate up to ~40 MHz
- HKROC is a waveform digitizer with auto-trigger

Main experimental results with HKROC0 – Charge and Time

- Measurement with the full chain (analog + digital and reconstruction)
  - Signal auto-triggered with threshold





Charge resolution :

< **0.1 p.e (200 fC)** at ≤ 10 p.e

< 1 % otherwise

Charge linearity < **±1%** from 1 to **1250 p.e. (2500 pC) across the 3 gains**

TDC characterization with **1/6 p.e. threshold**

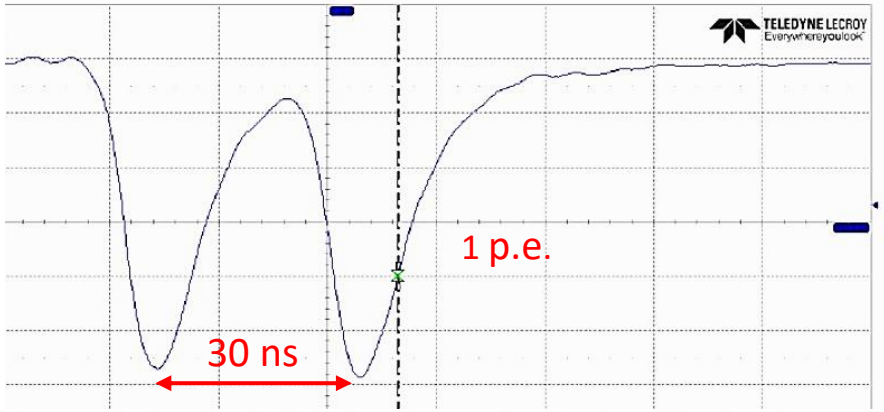
TDC resolution :

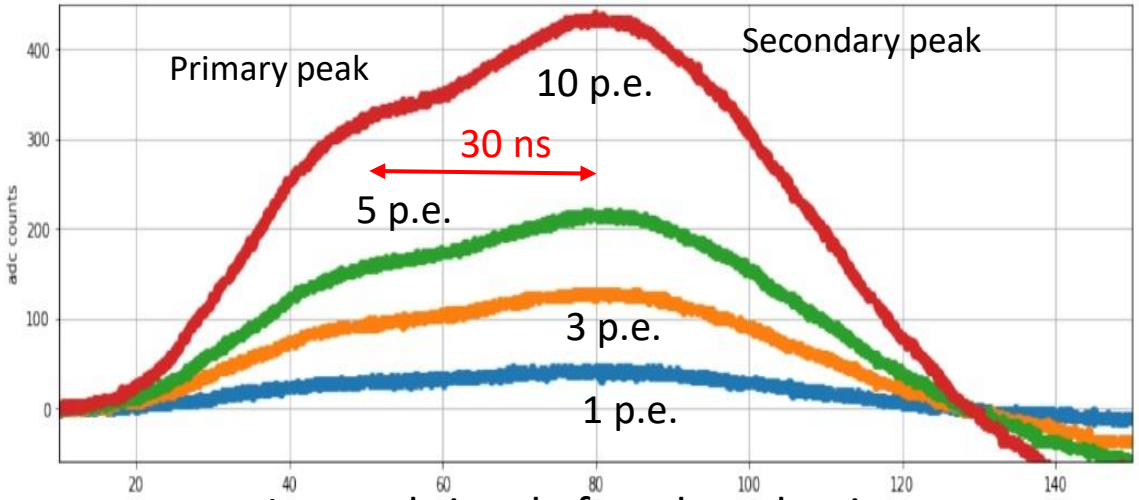
150 ps rms @ 1 p.e

≤ 25 ps rms @ 10 p.e

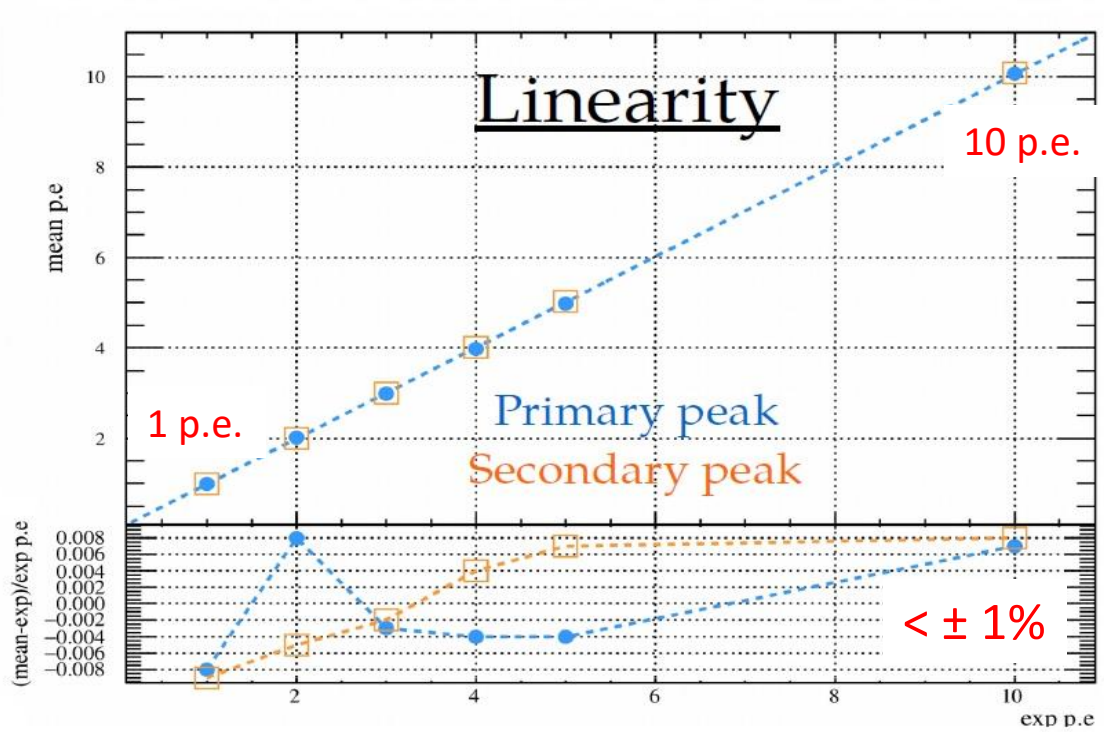
Main experimental results with HKROC0 - Pile-up

- Measurement with 2 events separated by ~30 ns (full chain: analog, digital and reconstruction)
  - Signals auto-triggered (internal prommagble threshold)





Internal signal after slow shaping



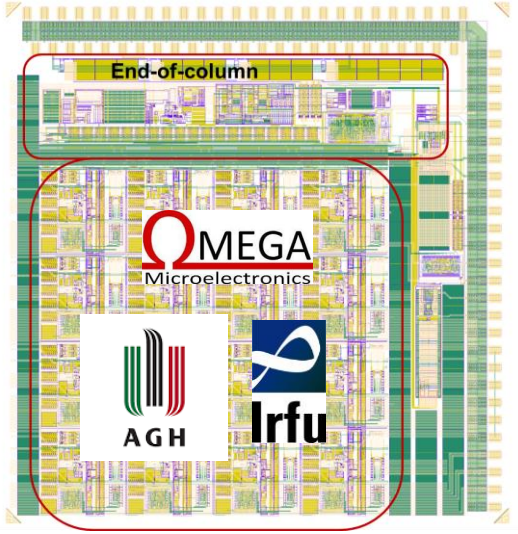
Charge reconstruction algorithm of the two peaks

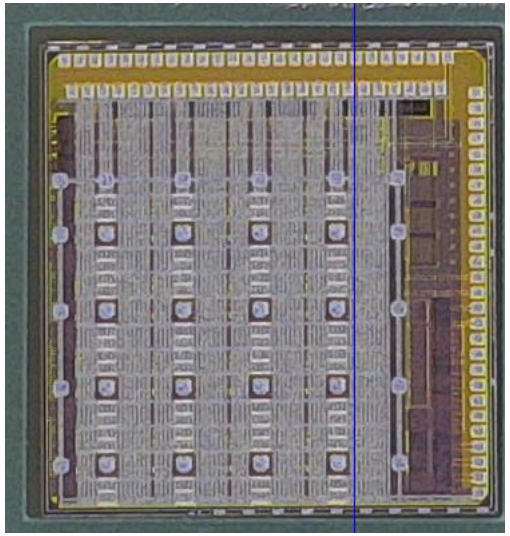
Good linearity of reconstructed pile-up events

We can reconstruct both peaks properly !

EICROC0 overview

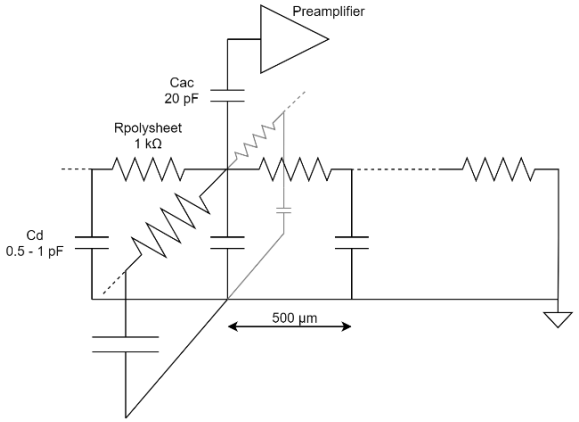
- EICROC0 is a 16-channel testchip for AC-LGADs at EIC
  - Based on ALTIROC (ATLAS HGTD) front-end and HGCROC (CMS HGCAL) ADC/TDC
  - Reads 500x500 µm pixels for sensor evaluation
  - Readout designed for testbeam (not EIC)
  - Fabricated in march 2022, received beg july 2022
  - now under test at IJCLAB and OMEGA
  - New submission in AIDA innova eng. run

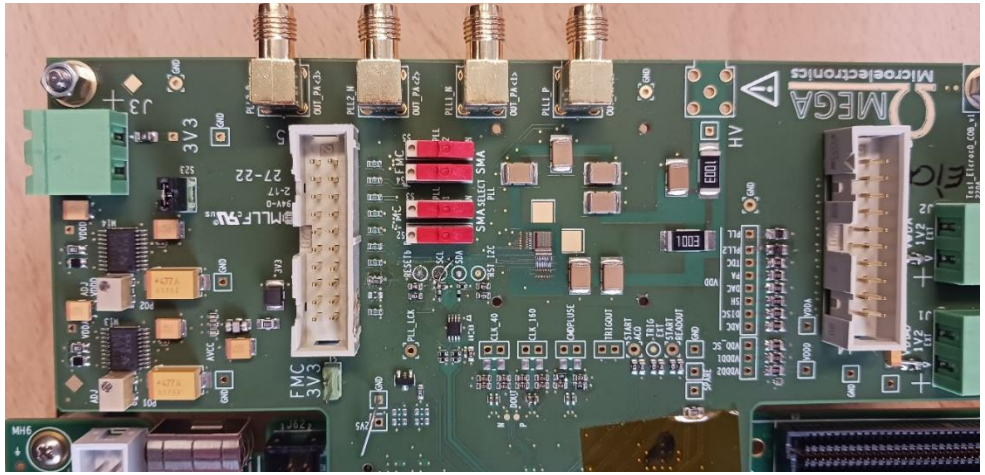




New concept of sensor [N. Cartiglia et al.]

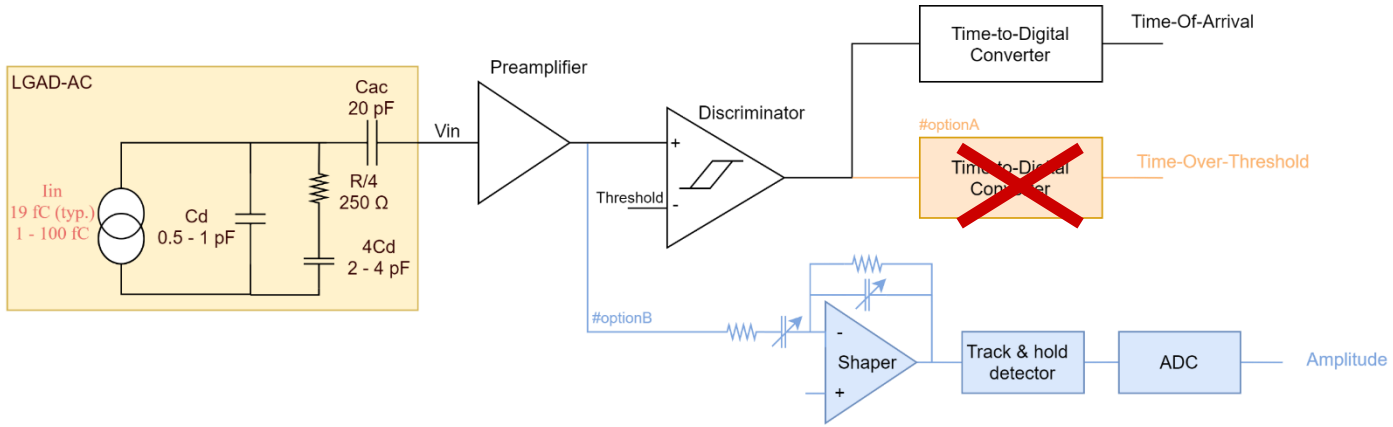
- AC coupled LGAD: **large signal and fast timing**
- Resistive layer for charge sharing: high position resolution
- « Large » pixel allows implementation of **ADC and TDC pixel-wise**

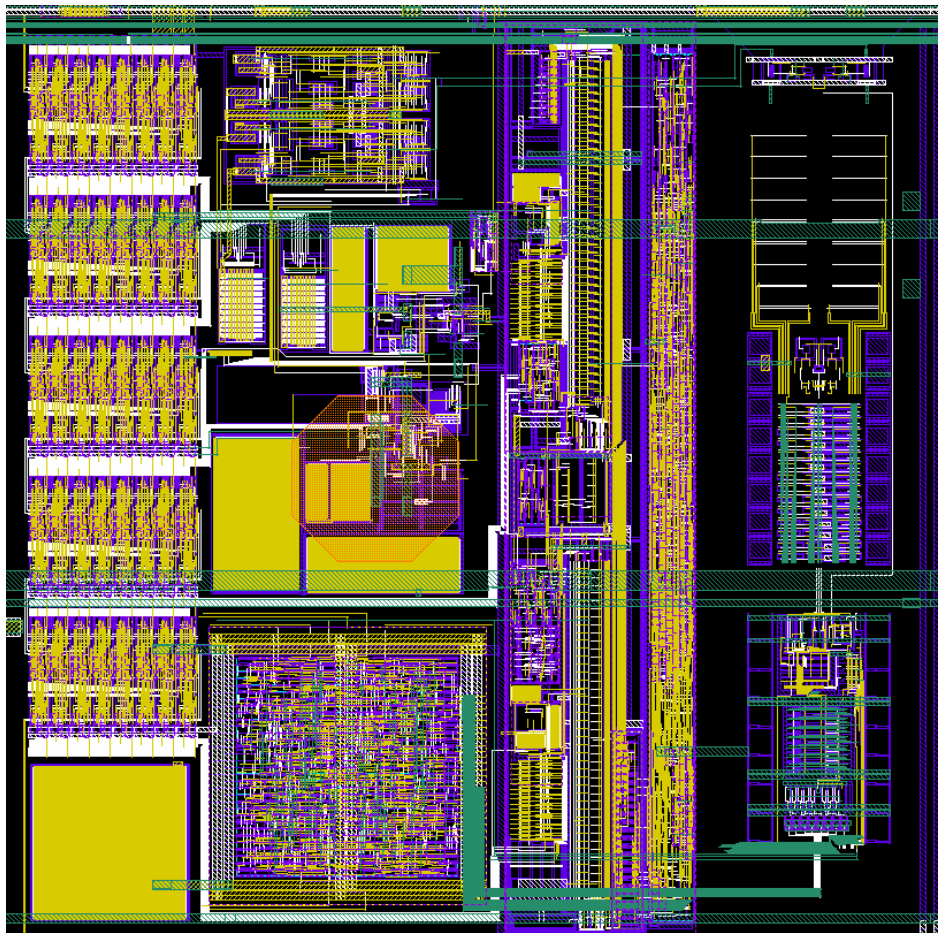




EICROC0 : one pixel overview

- One pixel design
  - Preamp, discri taken from ATLAS ALTIROC
  - I2C slow control taken from CMS HGCROC
  - TOA TDC adapted by IRFU Saclay
  - ADC adapted to 8bits by AGH Krakow
  - Digital readout : FIFO depth 8 (200 ns)
- 5 slow control bytes/pixel
  - 6 bits local threshold
  - 6 bits ADC pedestal
  - 16 TDC calibration bits
  - Various on/off and probes





Slow control

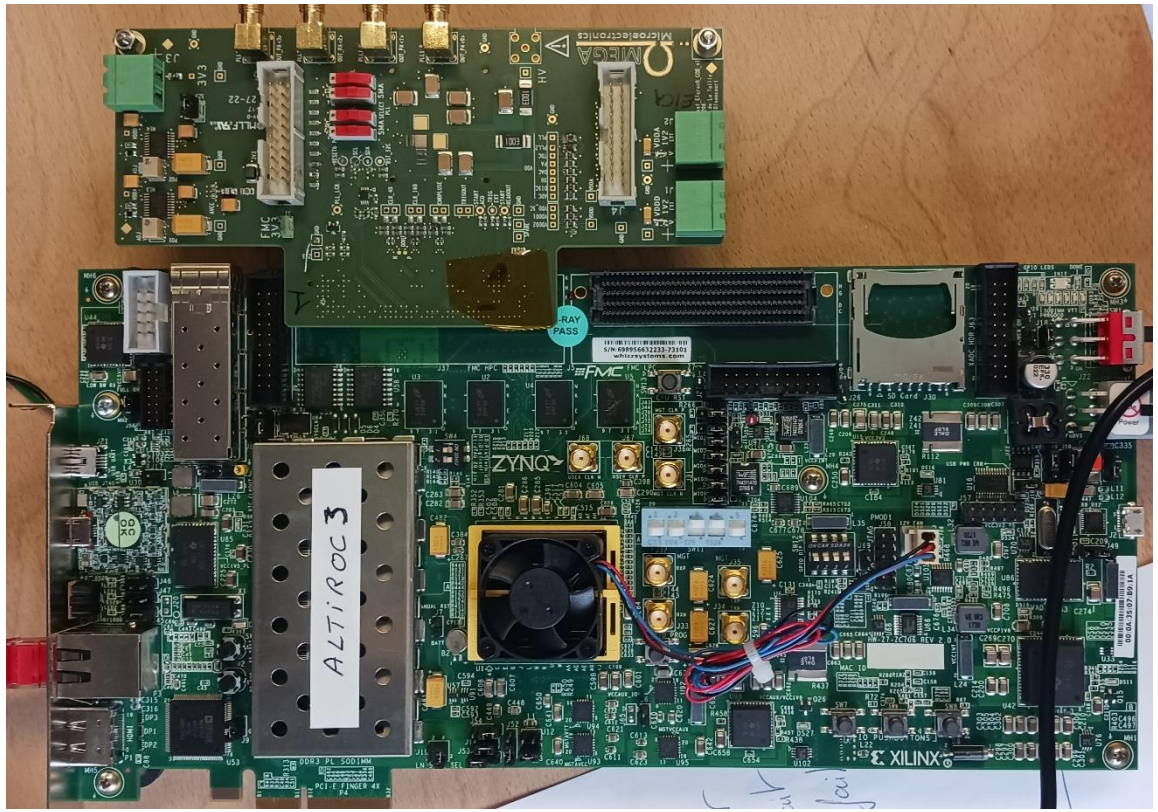
PA +discri

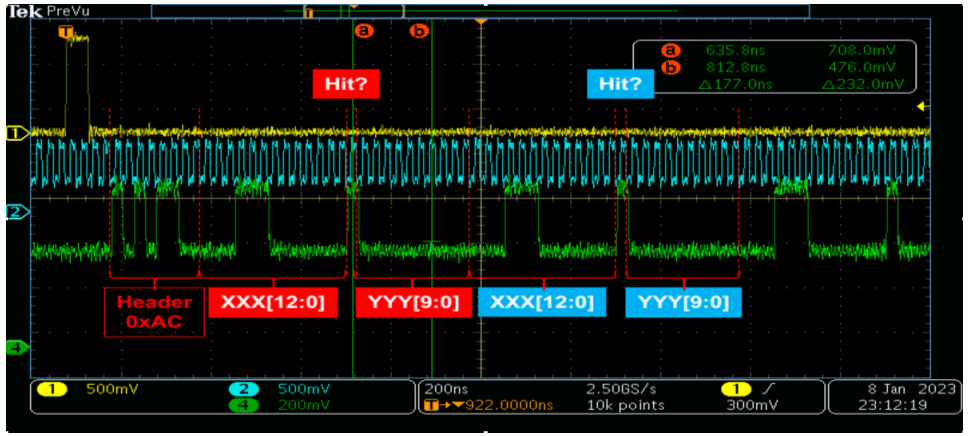
TOA TDC

8b 40M ADC

EICROC0 status

- Submitted in March 2022
- Both chips and testing boards arrived in July 22 and assembled in September 22
- Testboard up and running
  - Firmware and software from IJCLAB
  - Configuration OK
  - Preamp, discri signals observed
  - Data coming out as expected
  - Still trying to find time to understand the data





- CPROC (Central Processing unit in ReadOu Chip)
  - TSMC 130 nm
  - Exploratory R&D: programmable, needs of more and more intelligence in chip
  - Based on the RISCV

Trends for calorimeter readout

- On-detector embedded electronics, low power multi-channels ASICS
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC Lar, FATIC…
  - Challenges: # channels, low power, digital noise, data reduction, timing capability

- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC-ee, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence + joint optimization
  - Detector specific front-end but common backend
  - Allows common DAQ and facilitates combined testbeam

- Start from HGCROC / HKROC: Si and SiPM
  - Reduce power from 15 mW to few mW/ch
  - Allows better granularity
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - Several improvements foreseen in the VFE and digitization parts
  - 130 nm or 65 nm ?

Summary

- HKROC:
  - The second version, HKROC1, has been submitted this April
  - Bugs fix: ADC, TDC, DRAM
  - Lower crosstalk
- EICROC
  - A new chip dedicated for testing AC-LGAD has been submitted
  - TSMC 130 nm MPW run by 31st of March 2022
  - 4x4 matrix of 500x500 µm² pixel size
  - 8b SAR ADC per pixel for charge measurement up to 100fC
  - 10b TDC for timing measurement (25 ps binning)
  - ~ 1 mW/pixel
- CPROC
  - First chip with a RISC-V embedded
  - New exploratory R&D
- Implication in the DRD6 of ECFA
  - Targeting a new family of chips for future calorimeters