AIDA innova

Advancement and Innovation for Detectors at Accelerators

WP6 introduction

Hybrid Pixel Sensors for 4D Tracking and Interconnection Technologies

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AIDAInnova Annual meeting
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WP6 Tasks and Task Leaders

Objectives

Task 6.1. Coordination and Communication

See introductory section on page 29.

Task 6.2. Simulation and processing of common 3D and LGAD sensor productions

- Optimisation of processes for 3D and LGAD sensors for timing applications
- Simulations of various designs for 3D and LGAD sensors to compare and optimise the layout in terms of timing performance
- Simulations of surface and bulk radiation damage for 4D (tracking+timing) detectors toward more radiation tolerant solutions
- Processing of two common 3D sensor productions and two common LGAD productions by FBK/CNM
- Design and implementation of simulation software which is applicable to a large range of technologies and includes models for the description of effects from sensor level to readout electronics in semiconductor detectors

Task 6.3. Validation of common 3D and LGAD sensor productions

- Characterisation of the 3D sensors in terms of timing, radiation hardness, efficiency and uniformity via measurements in the laboratory and beam tests
- Characterisation of small pitch LGAD and inverse LGAD sensors (iLGADs) from the common production in terms of timing and efficiency via measurements in the laboratory and beam tests
- Feedback to the foundries for further process optimisation of 3D and LGAD sensors

Task 6.4. Development of interconnection technologies for future pixel detectors

- Development of suitable Anisotropic Conductive Films (ACF) material and die-to-die bonding process flows for small pixel pitches
- Production and post-processing of dedicated planar sensor wafers for ACF trials
- Test of the performance of sensor modules interconnected with ACF
- Production and test of ultra-thin assemblies interconnected with a wafer to wafer bonding technology
- Post-processing of sensor prototypes developed in Task 6.3

Task Leaders

T6.2
Gian Franco Dalla Betta
Giulio Pellegrini

T6.3
Gregor Kramberger
Ivan Vila

T6.4
Dominik Dannheim
Fabian Hügging

WP6 Milestones

Deliverable Number	Deliverable Title	Lead Beneficiary	Due Date (in months)	Means of verification
MS22	Wafer layout	FBK	18 ✓	Layout design file and report on the design choices, supported by simulations (Task 6.2)
MS23	Preliminary characterization of 3D and LGAD prototypes. Test set-up ready in the laboratories.	CSIC	23 February 23	Preliminary characterization on prototypes with the readout systems to be used with the final productions. (Task 6.3)
MS24	Completion of planar sensor productions for ACF	CNRS	18 ✓	Planar pixel sensor wafers delivered for interconnection tests (Task 6.4)
MS25	Availability of parts and definition of the technologies for wafer to wafer hybridization	UBONN	18 ✓	Wafers delivered to IZM and report on the technologies chosen for the interconnection (Task 6.4)

- Gregor and Ivan have prepared the draft of the MS23 report. After revision, by next week, it will be sent to the management.

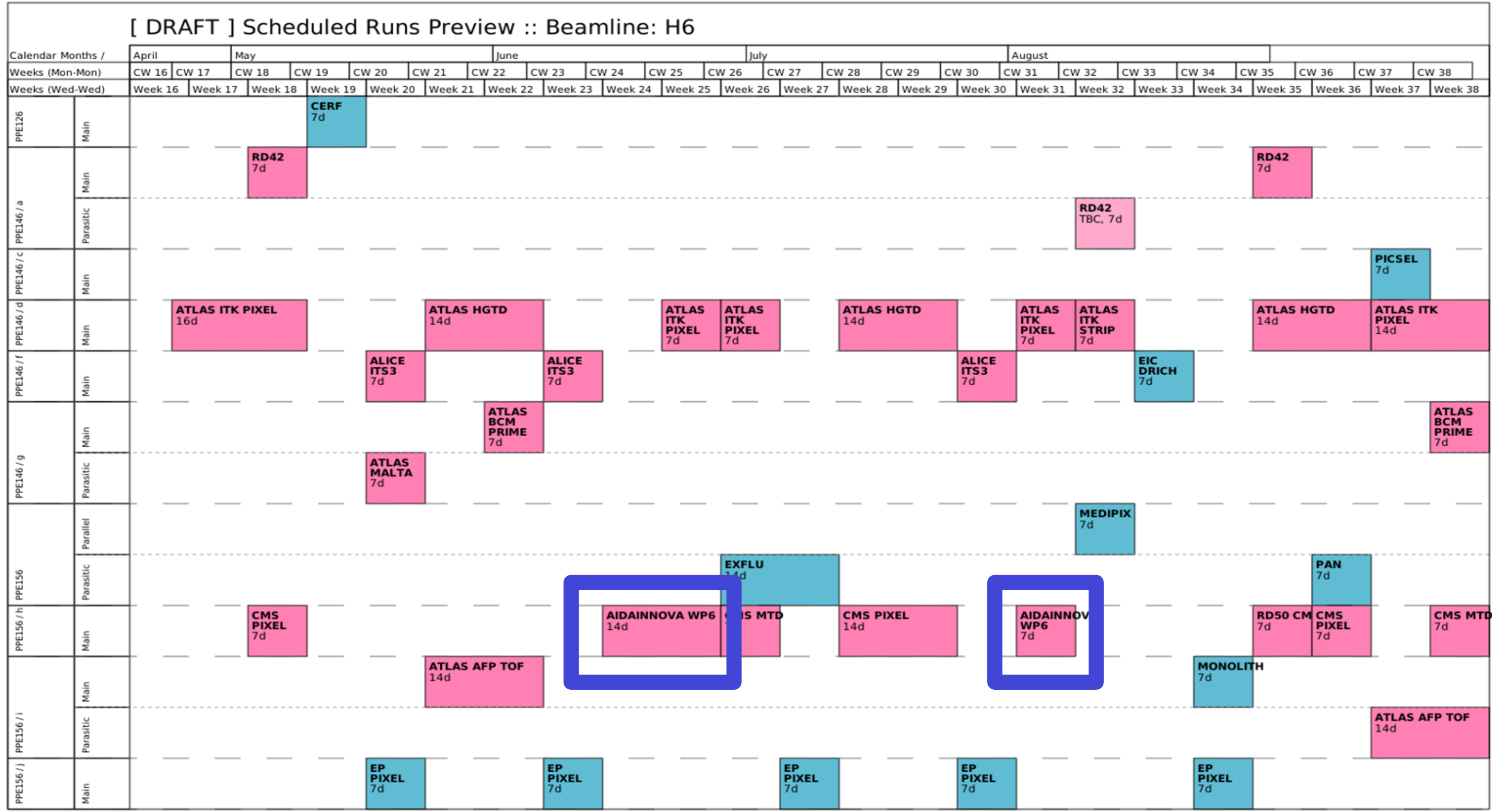
WP6 Deliverables

Deliverable Number	Deliverable Title	Lead Beneficiary	Type	Dissemination level	Due Date (in months)	comments
D6.1	Completion of common productions	CSIC	Report	Public	30 Oct 2023	Including preliminary char. at foundries
D6.2	Final validation of timing performance of common productions	INFN	Report	Public	46	Before and after irradiations
D6.3	Test of the final ultra-thin hybrid assemblies from wafer to wafer bonding	Bonn	Report	Public	44	Module functionality, interconnection yield and strength
D6.4	Validation of the ACF for large and small pitch assemblies	CERN	Report	Public	45	Small pixel sizes from 25 to 55 µm

First Deliverable is D6.1 in October 2023.

TB at SPS

- **Test beam campaigns**
  - 2+1 week of data taking at CERN SPS in Q2/Q3 2023, coordinated by Gregor and Ivan
  - One week at DESY in the second half of the year



Publications

- Remember to quote the AidaInnova acknowledgements when it applies in talks and papers.
  - Please do not forget to include the EC acknowledgement in all your publications (journal articles, conference papers, presentations, internal notes, etc.) related to AIDAinnova and to upload a copy of your publication on Zenodo.

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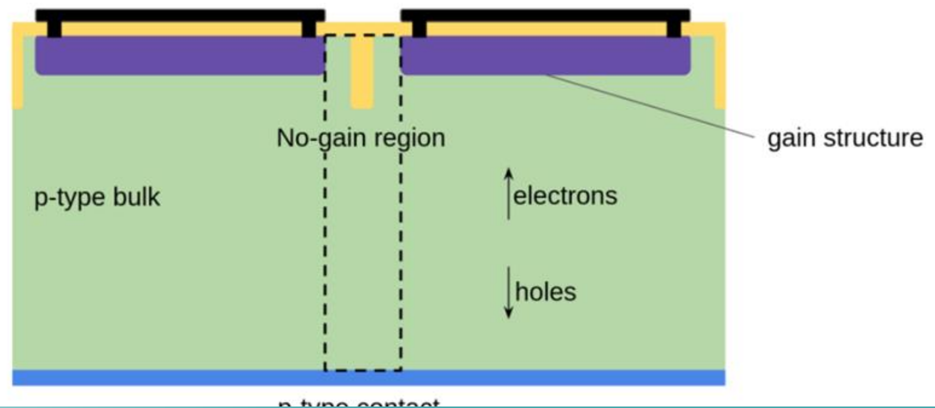
- All the information here: https://aidainnova.web.cern.ch/results/publication-committee
- Access to past publications and documents in Zenodo, https://zenodo.org/communities/aidainnova-project

Report from FBK

Trench Isolated LGADs @ AIDAinnova

- The goal is to realize an LGAD compatible with small pitch (55micron or less) and with high fluences
  - Isolation made by trenches
  - Carbon co-implantation to increase radiationa hardness
- Previus exeperiece
  - Internal FBK batches
  - Batches in RD50



Trench Isolated LGADs @ AIDAinnova
Layout

One full reticles (about 2x2 cm)

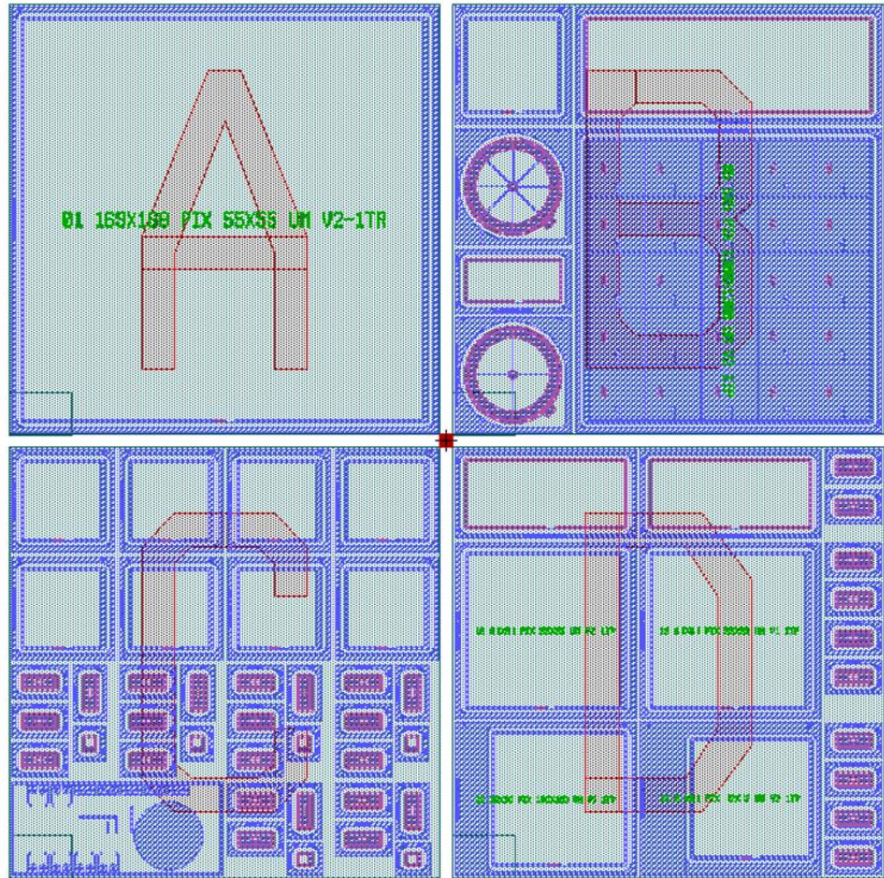
4 quarter (about 1x1cm)

- Pixel & strip
- PCM FBK
- 2x1 Test devices

In orded to explore

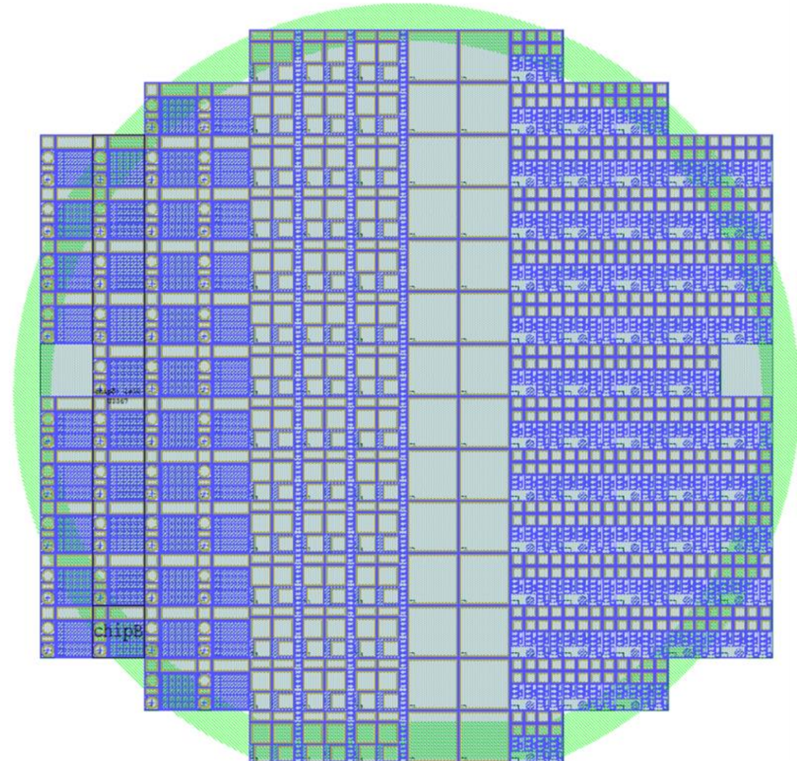
- Pitch
- Border: 4 version
- Number of trenches : 1 or 2

- Reticles in FBK



Trench Isolated LGADs @ AIDAinnova Wafer Layout

- the wafers are divided into a regular grid ($1cm^2$)
- in each column are printed the same quarter of the reticle



Trench Isolated LGADs @ AIDA Process

- **12 wafers**
- **Main process**
  - 45 µm, D2 , P2 and «high diffusion»

Split on

✓ Wafer thickness
✓ With or without carbon (it's the first time that we use carbon on TiLGAD)
✓ Trench Depth
✓ Trench Process

Note : two wafer per «main» split

Table splits

Wafer	Thickness	Carbon	Trench depth	Trench process
1	45	Y	D2	P2
2	45	Y	D2	P2
3	45	Y	D1	P2
4	45	Y	D1	P1
5	45	Y	D2	P1
6	45		D2	P2
7	45		D2	P2
8	45		D1	P1
9	55	Y	D3	P2
10	55	Y	D2	P2
11	55	Y	D2	P2
12	55		D2	P2

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Trench Isolated LGADs @ AIDAinnova

Timescale

- 12 wafers
- With and without carbon
- Process in progress
- To be completed in end September 2023

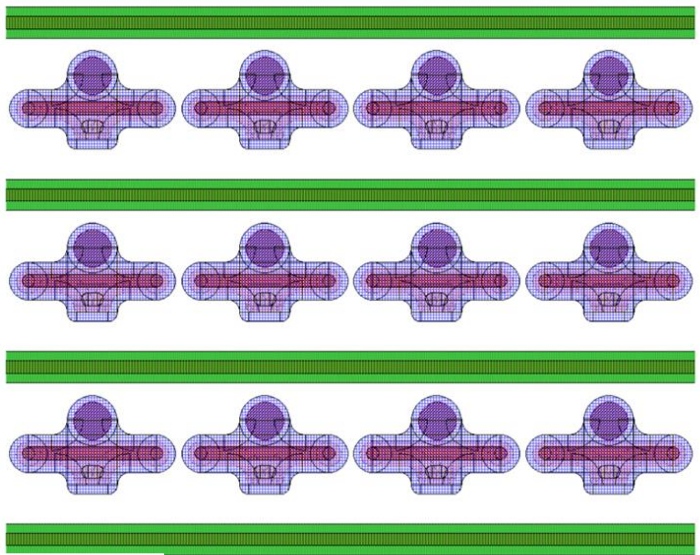
ExstraCost

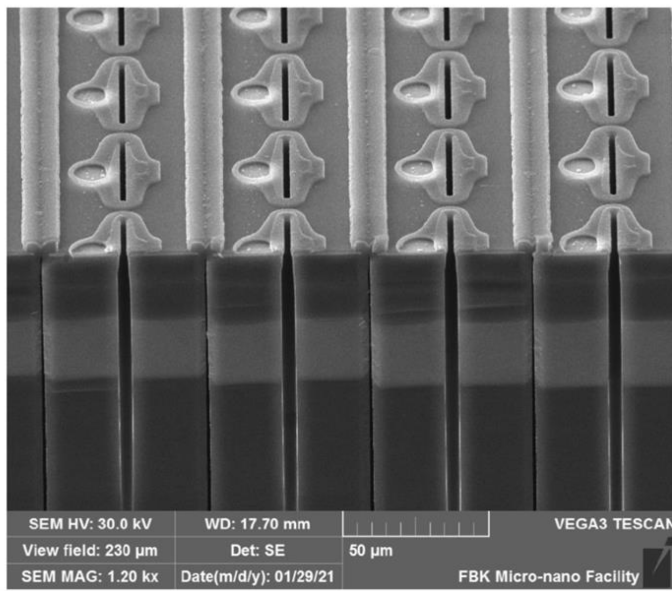
- Temporary metal not forseen from the begin
  - One reticle + process is about 6.5Keuro
- Carbon co-implantation (external service)
  - Set up 2Keuro + about 200euro per wafer

3D FBK@AIDAInnova

Si-3D @ AIDAinnova

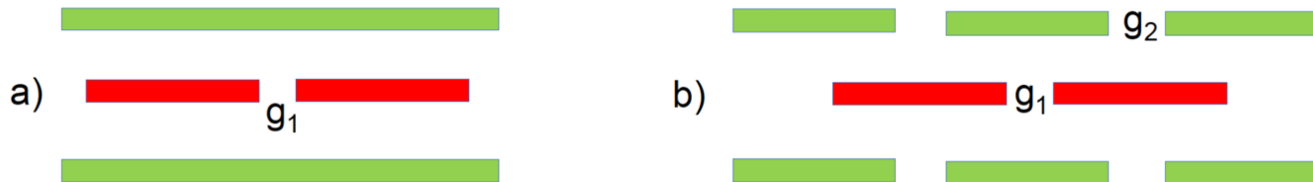
- Based on trench electrode
- Best performance for timing
- Develop in partnership with INFN Collaboration





Si-3D @ AIDAinnova
Layout 1

- 3D-trenched pixels only (no columns)
- Continuous ohmic trench (a) vs dashed ohmic trench (b)

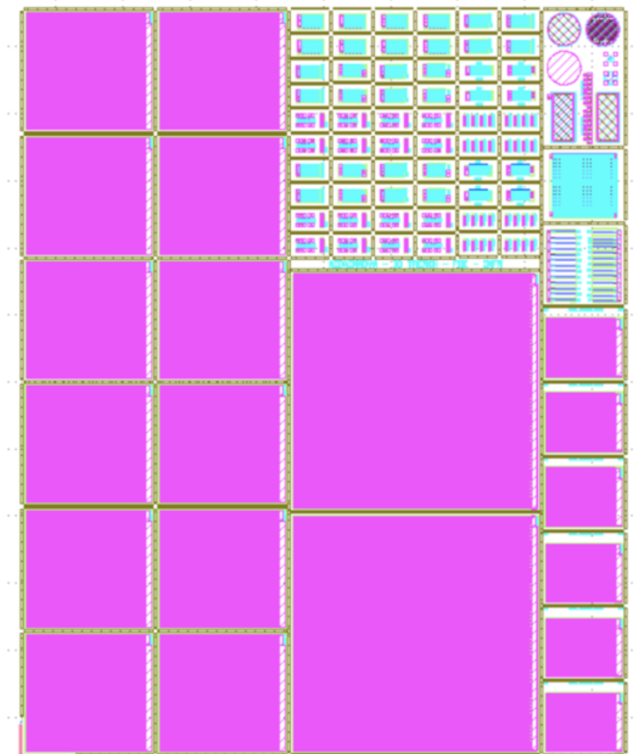


- Test structures (single/multiple pixels, strips, diodes, including 42 μm pitch)
- Pixel sensors (55 μm pitch)

Thanks to G.F. Dalla Betta

Si-3D @ AIDAinnova
Layout 2

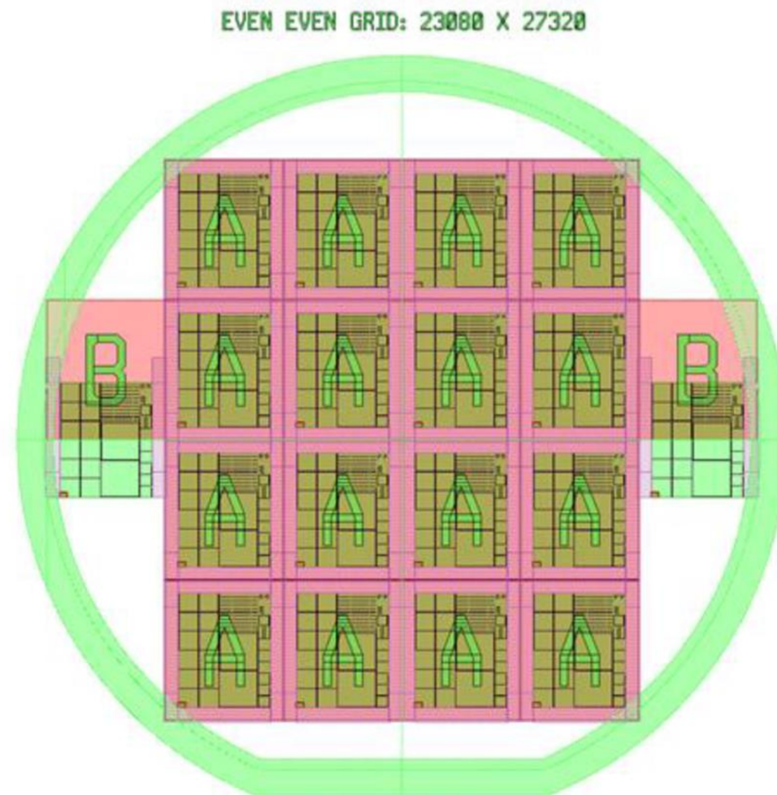
- **Pixel sensors (55 μm pitch)**
  - 32x32 pixels, multiplicity = 6 (3 std, 3 dashed)
  - 64x64 pixels, multiplicity = 12 (6 std, 6 dashed)
  - 128x128 pixels, multiplicity = 2 (1 std, 1 dashed)
- **Device test structures (55 μm pitch and 42 μm pitch, std and dashed)**
  - Groups of individual pixels
  - Strips
  - Diodes
- **Technological test structures**



Si-3D @ AIDAinnova wafer layout

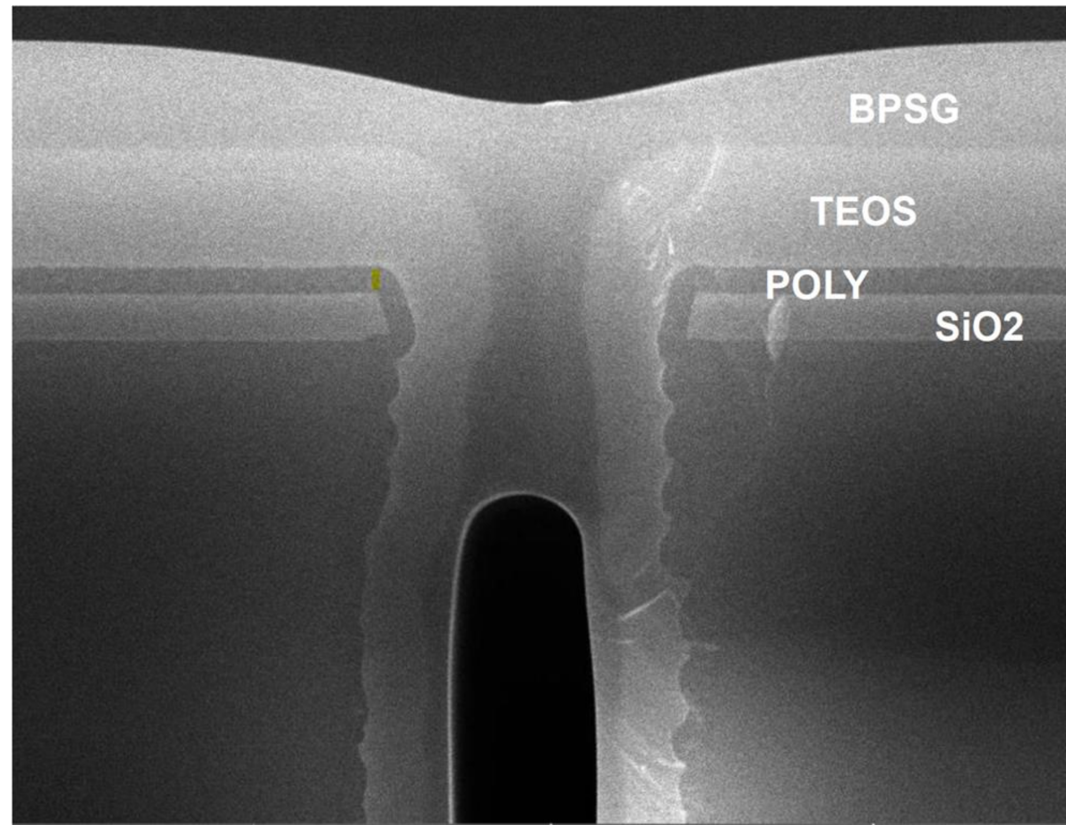
Test on going to increase the exposure shot on wafers

Increase the trench density increase the wafer bow



Si-3D @ AIDAinnova test : p-trenches filling

Planarization test:
BPSG deposition and reflow



Si-3D @ AIDAinnova TIMESCALE

Timescale

- 12 wafers
- 18 DIE on wafers
- 3 wafers at p-hole filling: check the bow
- 9 wafers ready to process: p-spray implanted
- To be completed in end August 2023

- Planarization test on going