Task 3.3:
Sub-ns timing capabilities for EUDET-style telescopes:

A Trigger Logic Unit (TLU) for AIDA-Innova With Picosecond Timing Support

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Task 3.3 Goals

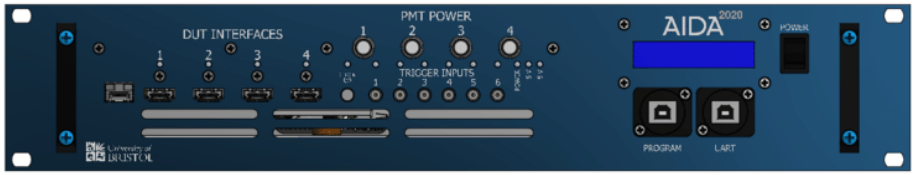
- From AIDAinnova grant agreement, part A:
  - "To provide a O (100) ps timing for particle hits, a dedicated timing layer as well as a trigger logic unit (TLU) with picosecond-timing support need to be developed, integrated and installed at both CERN and DESY. The precision timing layer will be provided by a TimePix4 plane, which will be fully integrated into the telescope hardware and the EUDAQ2 framework. We foresee having such planes available at all beam lines. To provide an ultimate timing resolution of 30 ps, an LGAD plane based on current developments for the HL-LHC will be included in the EUDET-style pixel telescopes. In order to benefit from this exquisite timing, the TLU needs to provide a stable clock with a 10 ps or better stable edge, which will be part of the AIDA TLU upgrade."
- Fast timing detector WP: NWO-I/Nikhef, UNIVBRIS, CSIC-IFCA, DESY,UCL, USC

Picosecond TLU

AIDA-2020 TLU connected to beam telescope

- Timing specification:
  - Clock jitter < 10ps RMS
  - Timing-stamping of input signals O(10ps) RMS
    - c.f. O(1ns) for AIDA-2020 TLU
- Backwards compatible with AIDA-2020 TLU
  - Same signals on DUT connections
    - trigger/busy/DUT-clk in EUDET-mode
    - Global-clk, trigger, busy, shutter, T0 in AIDA-mode
  - Small change to data format – timestamp will need more bits

Picosecond TLU - I/O



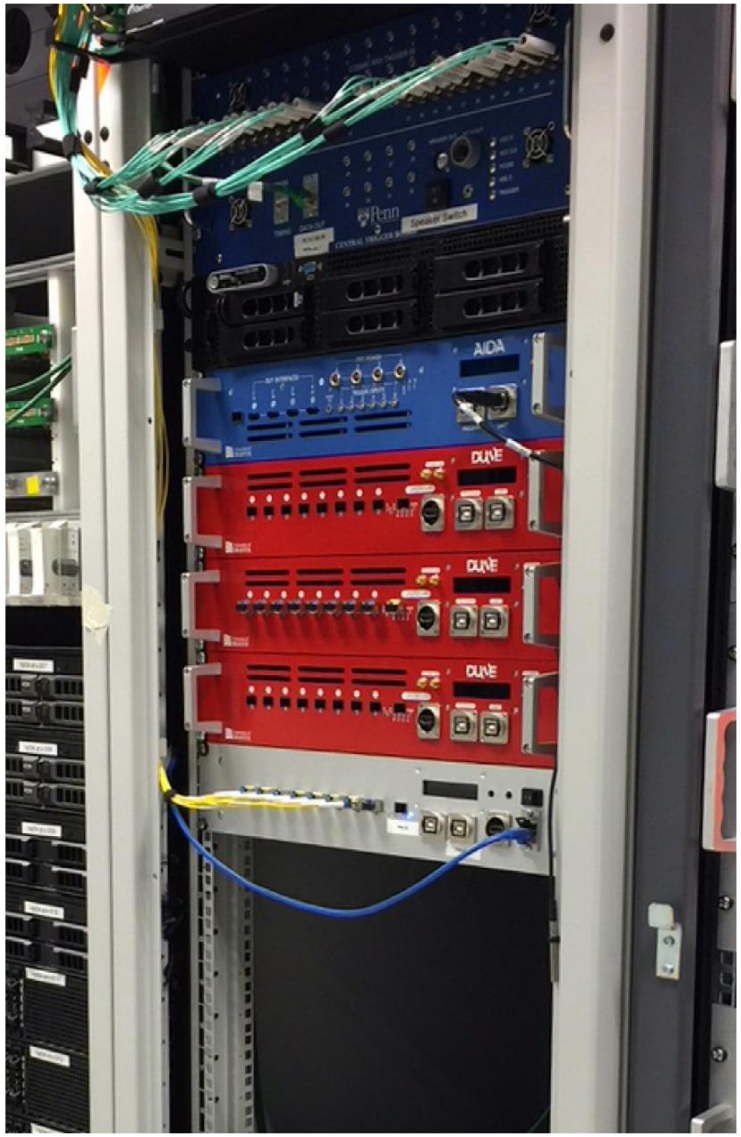
- Trigger inputs
  - Probably 8
    - (c.f. 6 for AIDA-2020 TLU)
  - One or more threshold discriminator per channel with ADC for time-walk correction
    - (c.f. threshold discriminator only in AIDA-2020 TLU)
  - TDC with O(10ps) bins
    - Looking at using PicoTDC (3ps bins)
  - Aim to contribute less to timing uncertainly than detector.
- Device Under Test (DUT) connectors
  - Compatible signal definitions as AIDA-2020 (also LVDS)
  - Move to “Display Port” from HDMI - mechanically more robust. Five good quality pairs (c.f. 4)
    - Passive adaptor to existing HDMI connector.
    - Opinions?

PicosecondTLU - Rate Capability

- Same goal for rate capability as AIDA-2020 TLU:
- Instantaneous rate ~ 10MHz:
  - 50ns between hits (little pile up at 10MHits/s)
- Sustained rate ~ 1MHz
  - Internal buffer in current AIDA-2020 TLU only 4k events.
    - Aiming to expand to O(10M events)

Picosecond TLU - Optical Interface

- Retain optical interface introduced in AIDA-2020 TLU
  - Can distribute timing information over fibre
  - Used for (Proto)DUNE-SP
    - https://doi.org/10.1016/j.nima.2019.04.097
  - fibre bandwidth much larger than copper cable.
    - Possibility of more precise timing over longer distances
      - Clock jitter (endpoint w.r.t. master) of 12ps measured (**DOI** 10.1088/1748-0221/18/01/C01067)
      - Measurement of fibre-delay , precision < 100ps

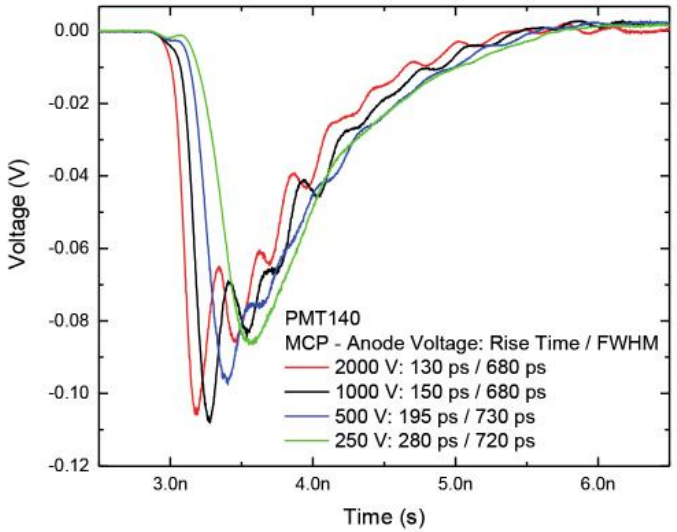


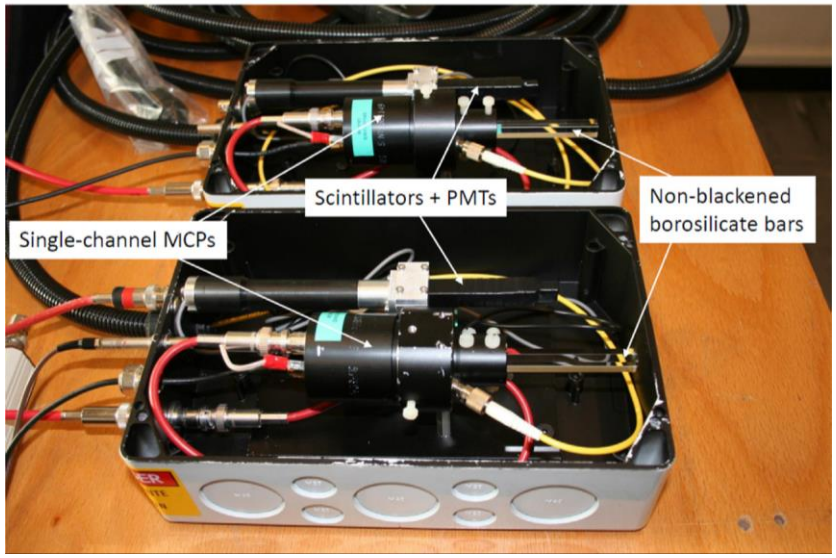
Picosecond TLU - Timing reference

- Testing pico-second detectors requires pico-second time reference
  - TLU timing only as good as reference
- Some beam-line users will bring their own time reference detectors. Some would benefit from precise time reference at beam-line.
- Baseline timing reference – LGAD

Picosecond TLU - Timing reference

- Baseline timing reference – Either MCP-PMT or LGAD
- For testing anticipate using Cherenkov light and high speed photo-detector
  - Used for “TORCH” LHCb upgrade beam-tests
  - MCP-PMT single photon jitter 66ps FWHM http://www.photek.co.uk/pdf/datasheets/detectors/DS006%20Photomultiplier%20Tube%20Datasheet%20issue%202.pdf
  - Reports of single particle timing < 10ps RMS

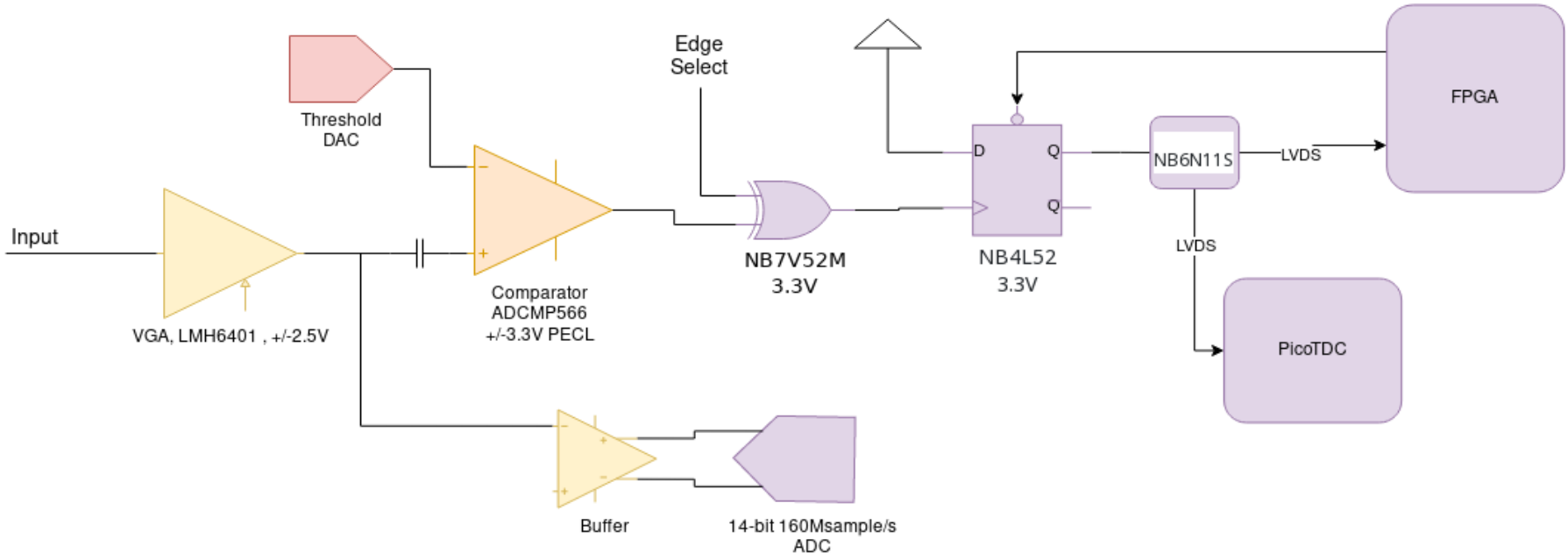




Taken from http://dx.doi.org/10.1016/j.nima.2016.06.087

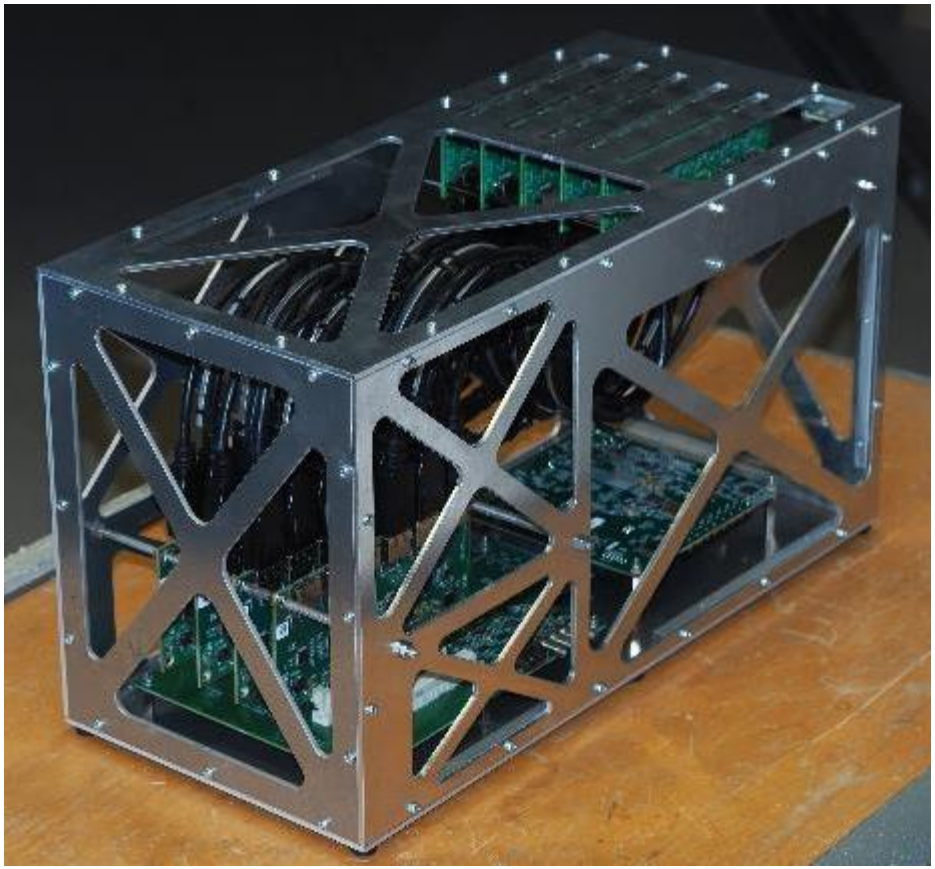
Picosecond TLU – Prototyping Trigger Input

- ~ 4GHz -3dB bandwidth to comparator
- Adjustable gain
- ADC for pulse-by-pulse time-walk correction.



TLU – DUT Fanout

- Some user require many DUT interfaces
  - TLU has 4 (perhaps 6 in AIDAInnova TLU)
- Fanout produced for AIDA TLU
  - Up to 30 DUTs
  - Used in CERN East Area with “TORCH” (LHCb PID prototype) beam-test
  - Update of module in use at LHCb Timepix telescope on SPS
- Updated circuitry with up-to-date devices
  - Lower clock jitter.



Picosecond TLU - Software/Firmware/Hardware

- Read out with UDP/IP
  - IPBus (developed by CMS, but widely used)
  - Same as AIDA(-2020) TLU.
- Integrate with EUDAQ
  - EUDET and AIDA-2020 TLUs already integrated
- Open source firmware and hardware design
  - ohwr.org

TLU Clock

- TLU can either produce a clock or accept a master clock
- Investigate ability to lock clock to e.g. DESY beam-clock
  - Use internal clock during ramp, swap to beam-clock before extraction
  - Needs detectors to be able to tolerate clock being “slid” from one source to another
  - Advantage – particles arrive at fixed time with respect to clock edges
- Can be prototyped with current TLU
  - Progress effort limited.

Timescale

- Deliverable D3.2:
  - What: “PicoSecond TLU” produced
  - When: M39
- Slippage due to difficulties recruiting
- Stages:
  - Prototype of analogue input stage
    - Q2/23 (Was aiming for end ‘22
  - Prototype 1 trigger, 1 DUT TLU
    - Point at which integration with EUDAQ can start
  - Full TLU (probably using COTS FPGA module)