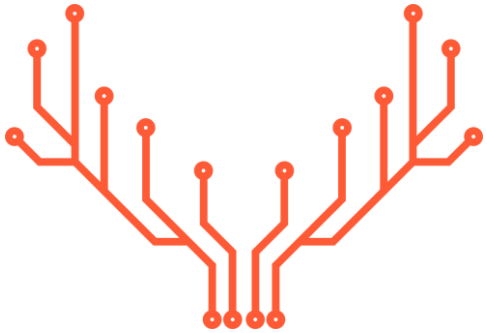
Task 3.5.1 – Development of common DAQ hardware (Caribou)



Eric Buschmann, Dominik Dannheim (CERN)

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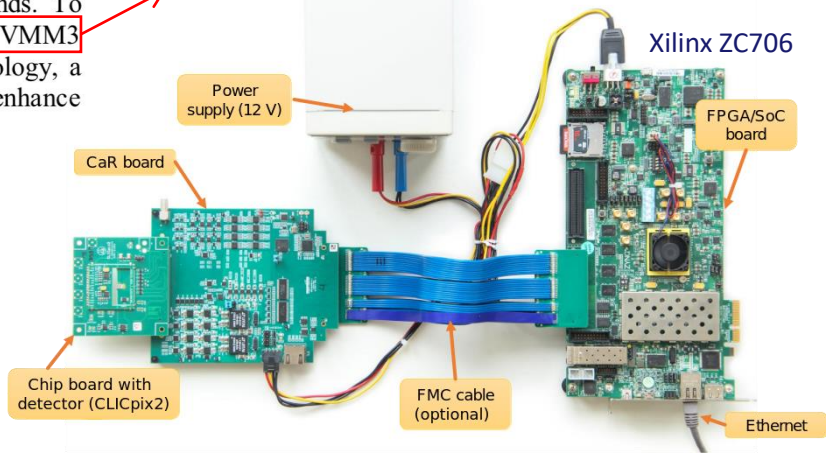
Overview

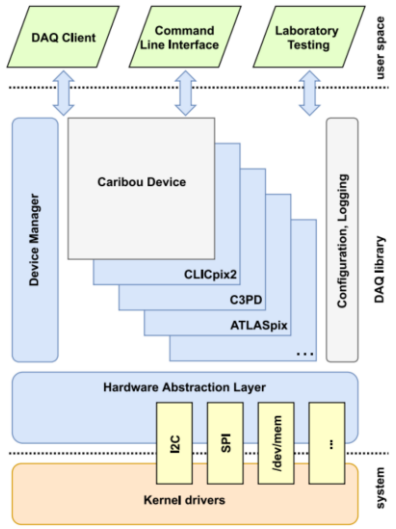
Task 3.5 Development of common DAQ hardware (CERN, DESY, *SRS Technology*[23])

In this task, common DAQ boards will be developed to support the silicon sensor (WP5, WP6) and gas detector (WP7) developments and to reduce duplication of work by providing generic DAQ test-stands. To meet the specific needs of the silicon and gas detector community, boards based on the Caribou and VMM3 will be developed. The VMM3 development also has industrial involvement from SRS Technology, a CERN spin-off company. These systems will be fully integrated into EUDAQ2 and will therefore enhance and simplify beam tests for prototype detectors.

VMM3 covered in next talk



- Flexible DAQ system for silicon detector testing based on modular hardware, firmware and software
  - System-on-Chip (SoC) board
    - Embedded CPU for Linux operating system, DAQ software (Peary), user interface
    - FPGA for detector control and data processing, TDC
  - Common Carboard interface board
    - Physical interface from SoC board to detector
    - Provides resources (voltage regulators, ADCs, pulse/clock generator)
  - Application-specific chip carrier boards
    - Detector and passive components



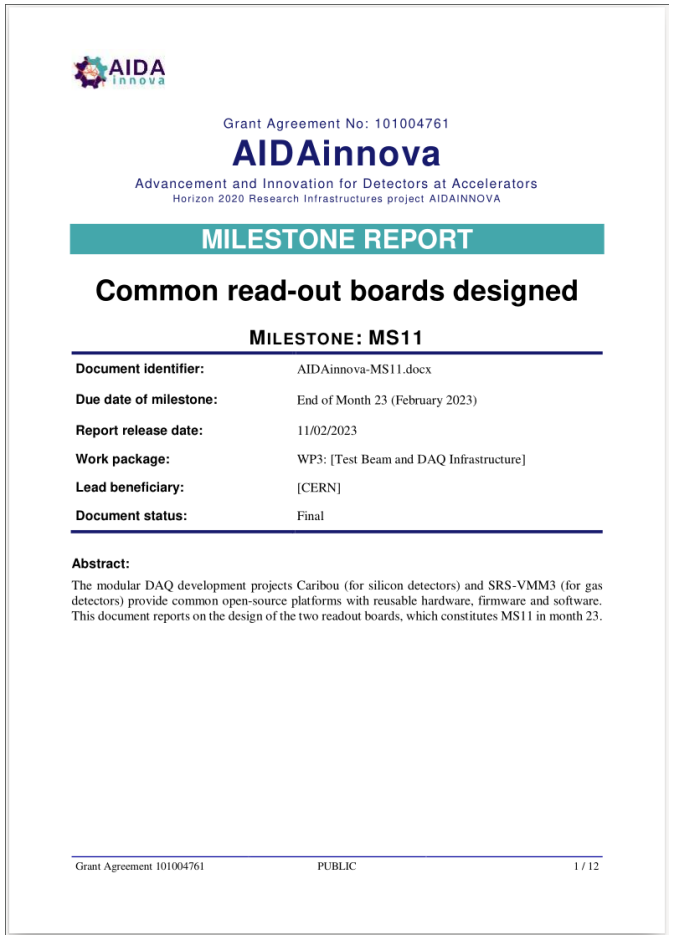
Caribou architecture

Groups involved

- CERN
  - Coordination of common hardware production, firmware development, user support
- DESY
  - Coordination of common Peary Software, test-beam integration
- External resources:
  - CERN Strategic EP R&D Programme
    - Caribou receives resources from EP R&D programme, linked to Caribou support of monolithic sensor developments
  - BNL OMEGA group, Carleton University, ORNL
    - Design of Common Hardware (Carboard)
  - RD50
    - 9 RD50 member institutes use Caribou for radiation-hard High-Voltage MAPS developments
    - RD50 supported v1.4 Carboard hardware production through common funds project

Milestones

- MS11 [M23]: Common readout boards designed (CERN)
- Achieved on time for Caribou (and VMM3)
- Milestone report includes design of Carboard version 1.4 Caribou hardware



AIDA innova

Grant Agreement No: 101004761

AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

Common read-out boards designed

MILESTONE: MS11

Document identifier:	AIDAinnova-MS11.docx
Due date of milestone:	End of Month 23 (February 2023)
Report release date:	11/02/2023
Work package:	WP3: [Test Beam and DAQ Infrastructure]
Lead beneficiary:	[CERN]
Document status:	Final

Abstract:

The modular DAQ development projects Caribou (for silicon detectors) and SRS-VMM3 (for gas detectors) provide common open-source platforms with reusable hardware, firmware and software. This document reports on the design of the two readout boards, which constitutes MS11 in month 23.

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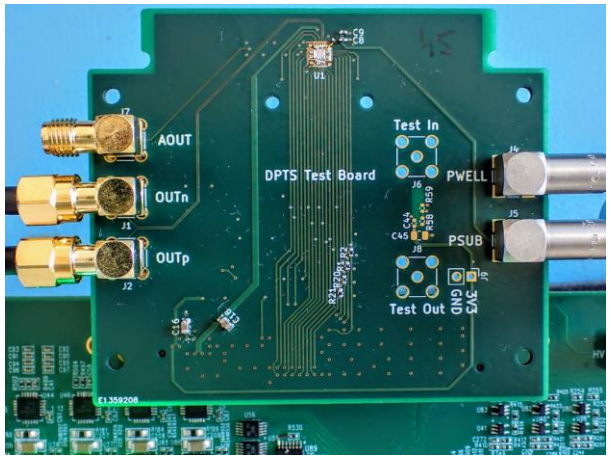
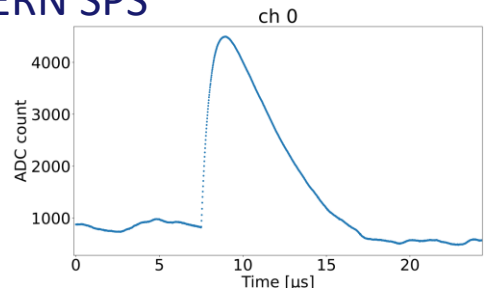
Achievements – Device integration

- Integration of APTS 65 nm monolithic technology demonstrator
  - 4x4 pixels with 10..25 µm pitch and asynchronous analog readout on 16 channels
  - Readout with 65 MHz sampling ADC on Carboard
  - Successful test beams at MAMI and DESY

- Integration of DPTS 65 nm demonstrator
  - 32x32 pixels with 15 µm pitch and asynchronous digital readout on one channel
  - Readout with TDC in Caribou FPGA
  - Successful test beams at CERN SPS



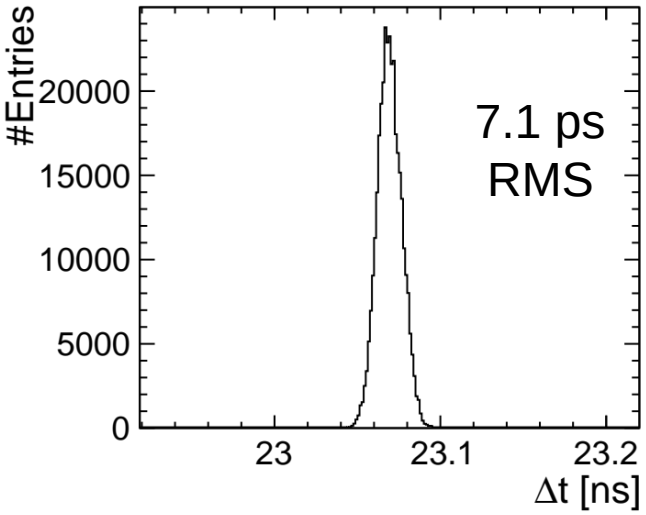
ADC readout: Pulse from 90Sr source on APTS



Achievements – TDC in Caribou FPGA

- Detector prototypes with asynchronous r/o and delay encoding of pixel positions (FASTPIX, DPTS) require detection of pulses with 100s of ps width with 10s of ps resolution over 100s of µs timescales with no deadtime
- TDC implemented in FPGA replaces oscilloscope-based readout of digital signals (ToA, ToT, position encoding)

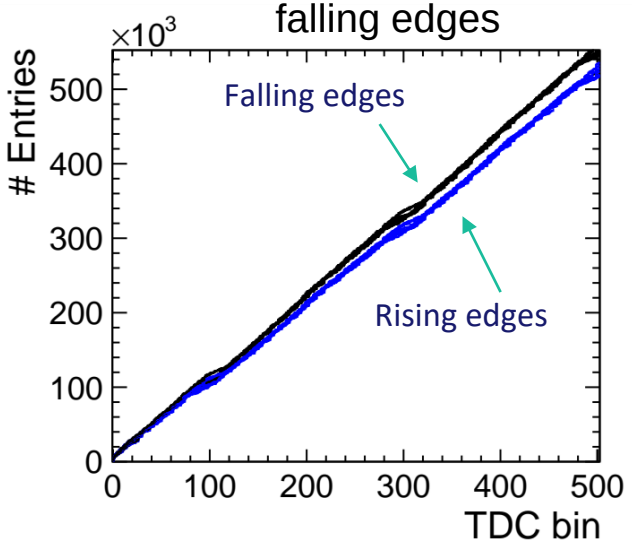
  →Very compact and versatile r/o system w/o additional hardware
- Used successfully for DPTS readout



TDC time resolution for 12ns delay on 4v4 channels

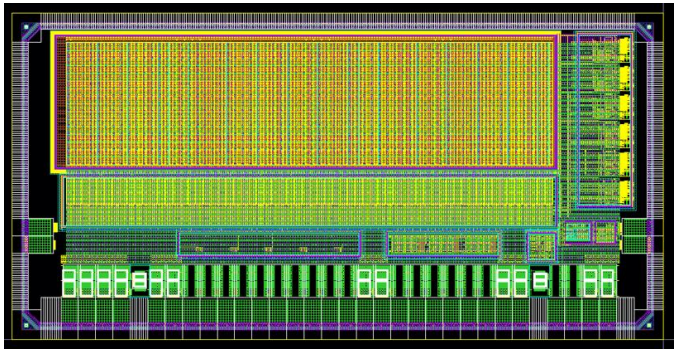
7.1 ps / $\sqrt{2}$ = 5.1 ps resolution per group

TDC calibration for rising and falling edges

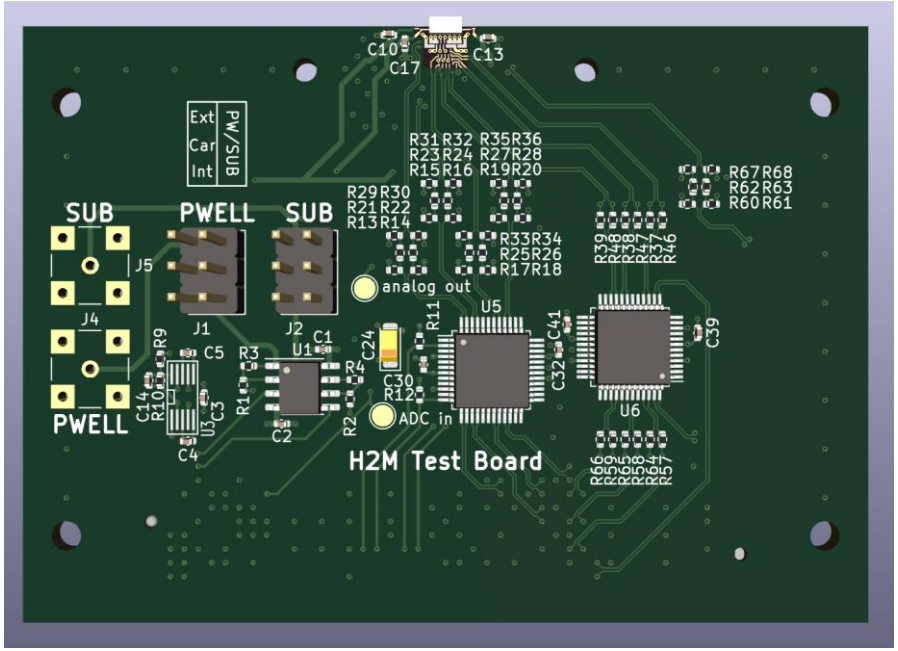


Ongoing work – H2M

- Integration of new H2M (Hybrid-to-Monolithic) 65 nm demonstrator chip
  - Developed by CERN / DESY TANGERINE / IFAE
  - 64x16 matrix with 35 µm pitch
  - Porting of hybrid pixel architecture to monolithic process
  - Testing of design methodology and digital cell library
- Chip board design finished (CERN)
- Software and firmware development ongoing (DESY / TANGERINE)
- First tests expected in a couple of weeks



H2M chip and chipboard



Ongoing work – Caribou 2.0

- Caribou 2.0 hardware under development
  - Based on System-on-Module (SoM) platform with Zynq UltraScale+
  - Replace Xilinx evaluation board + Carboard with custom carrier board and SOM

  →Reduced Cost and improved performance
- Ongoing design effort by Carleton, BNL, ORNL
  - Pre-protoype board tested at BNL, successful validation of digital design (M. Benoit and D. Matakias)
  - List of resources and design features iterated in Caribou user meetings
  - Carboard 2.0 design in progress (M. Pijacki)
  - First prototypes expected in 2023
- Need for consolidation of software and firmware

Pre-prototype for Caribou 2.0

XU1 SOM

Summary / Conclusions

- Ongoing work on integration of new prototypes
- Support for new readout schemes with fast ADC and TDC in FPGA
- Ongoing developments towards Caribou 2.0 on SOM platform: reduced cost, improved performance

- Resources:
- Repository: https://gitlab.cern.ch/Caribou
- Egroup: caribou-users@cern.ch
- Presentations and Publications:
- E. Buschmann, Status and recent extensions of the Caribou DAQ system for picosecond timing with an FPGA TDC, TWEPP 2022, https://indico.cern.ch/event/1127562/contributions/4904889/ and https://doi.org/10.1088/1748-0221/18/02/C02005
- E. Buschmann, Status of the Caribou DAQ System, BTTB 2022, https://indico.cern.ch/event/1058977/contributions/4631224/
- Reference publications:
- T. Vanat, Caribou – A versatile data acquisition system, TWEPP 2019, http://dx.doi.org/10.22323/1.370.0100
- H. Liu et al., Development of a modular test system for the silicon sensor R&D of the ATLAS Upgrade, http://dx.doi.org/10.1088/1748-0221/12/01/P01008