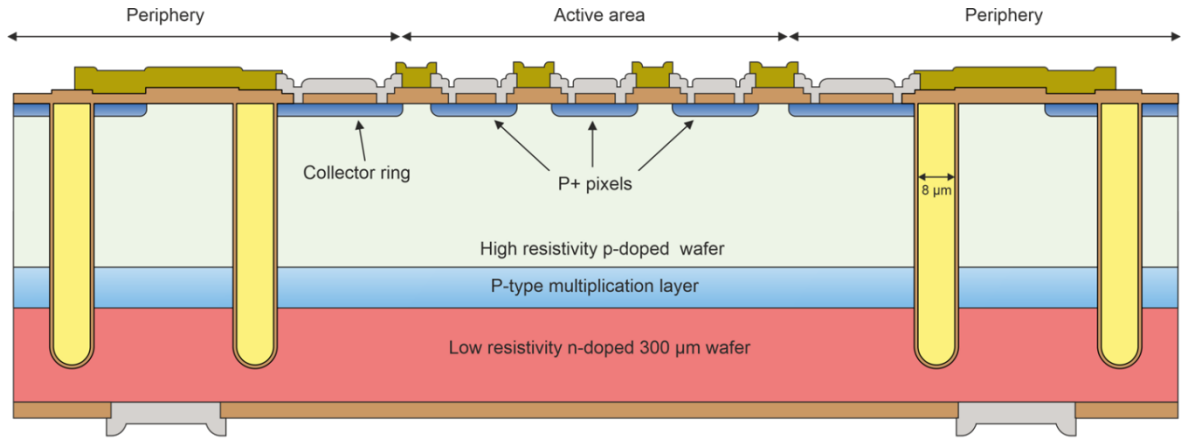
Status of LGAD and 3D Productions at CNM

Current Status of the CNM AidaInnova Runs

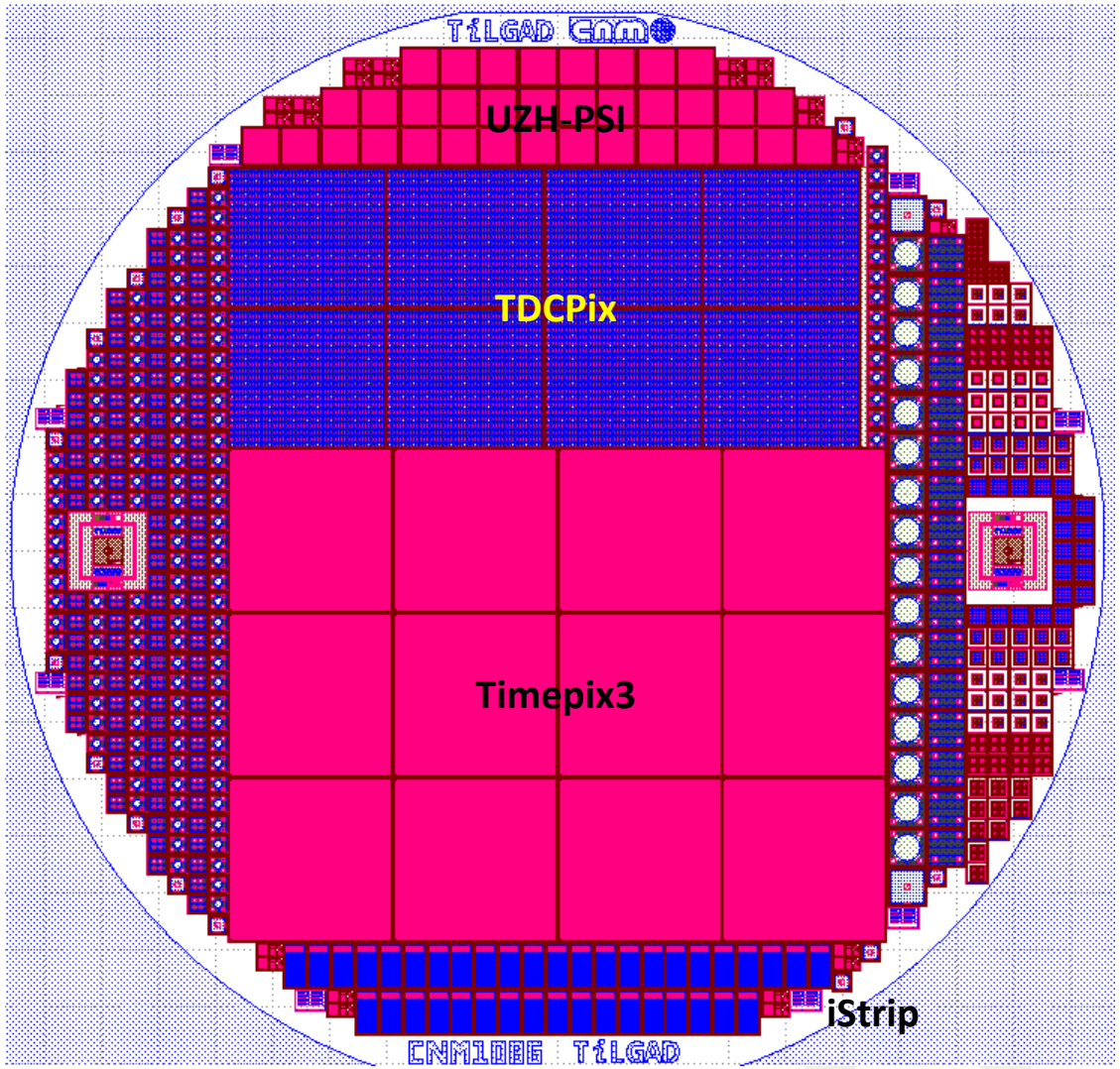
Run	Description	Clean Room Step
15543	150 mm **Timepix4 PiN**, Si (300 µm), 6PN1. **AidaInnova WP3**	Production completed (Waiting for UBM)
16020	150 mm **AC-LGAD**, Si (300 µm) and Si-Si (50/350 µm), 6LG4. **RD50**	Production completed (Waiting for UBM)
16069	100 mm **3D-DS Timing**, Si (285 µm), 240 µm depth columns, 10 µm columns diameter. **RD50**	Step 105/130 (Passivation Deposition)
16421	100mm **Timepix3 Trench iLGAD**, Epitaxial and Si-Si wafers, 4iLG3. **Engineering Run**. **RD50**. **AidaInnova WP6**	Step 16/65 (P+ Ohmic Contact Implantation, IBS France)
-	100mm **Timepix4 Trench iLGAD**, Epitaxial and Si-Si wafers, 4iLG3 **AidaInnova WP6**	Mask being drawn, Waiting for **TimeSpot1** Specifications

iLGAD Third Generation (4iLG3). Engineering Run. On going

- **Run16421: 6 Wafers**, 100 mm, CNM1086 Mask Set
  - **3 wafers**: **Epitaxial Wafers** (50/515 µm)
  - **3 wafers**: **Si-Si Wafers** (50/350 µm)
- **TimePix3.** 55x55 µm pitch, 256x256 pixels: **12 devices**
- **TDCPix.** 300x300 µm pitch, 40x45 pixels: **8 devices**
- **UZH-PSI.** 100x100 µm pitch, 30x30 pixels: **36 devices**
- **iStrip.** 80 µm pitch, 20 strips: **40 devices**
- **Pad and Nikhef Test Devices** to fill the gaps
- **Six months** are needed for its Production and Electrical Characterization (**started in February**)

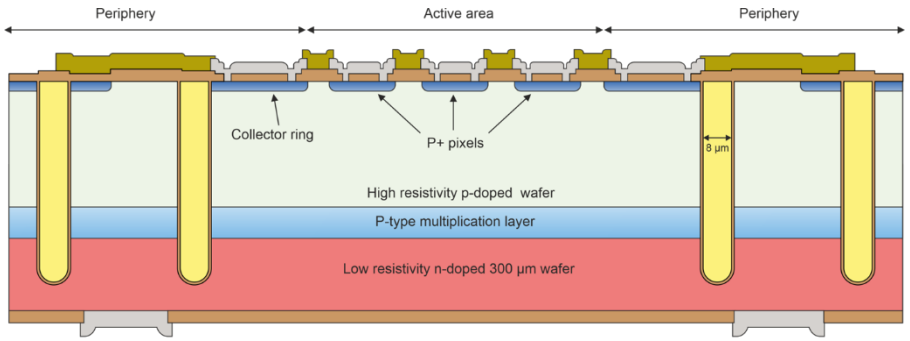


Wafer Layout

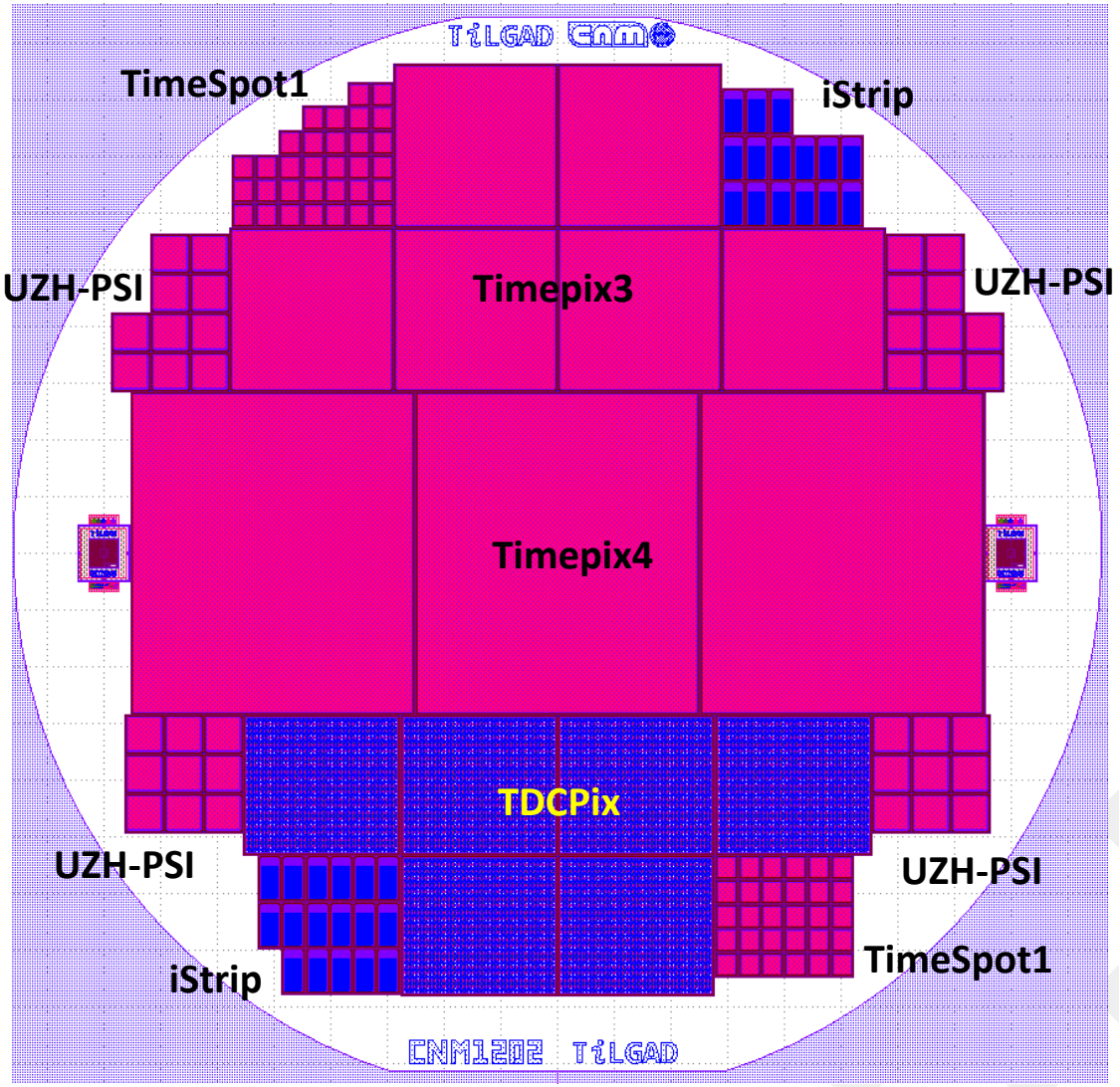


iLGAD Third Generation (4iLG3). AidaInnova Run

- **RunXxxxx: 6 Wafers**, 100 mm, CNM1202 Mask Set
  - **3 wafers**: **Epitaxial Wafers** (50/515 µm)
  - **3 wafers**: **Si-Si Wafers** (50/350 µm)
- **TimePix4.** 55x55 µm pitch, 448x512 pixels: **3 devices**
- **TimePix3.** 55x55 µm pitch, 256x256 pixels: **6 devices**
- **TDCPix.** 300x300 µm pitch, 40x45 pixels: **6 devices**
- **TimeSpot1.** 55x55 µm pitch, 32x32 pixels: **32+30 devices**
- **UZH-PSI.** 100x100 µm pitch, 30x30 pixels: **20+18 devices**
- **iStrip.** 80 µm pitch, 20 strips: **15+17 devices**
- **Pad and Nikhef Test Devices** to fill the gaps
- **Six months** are needed for its Production and Electrical Characterization

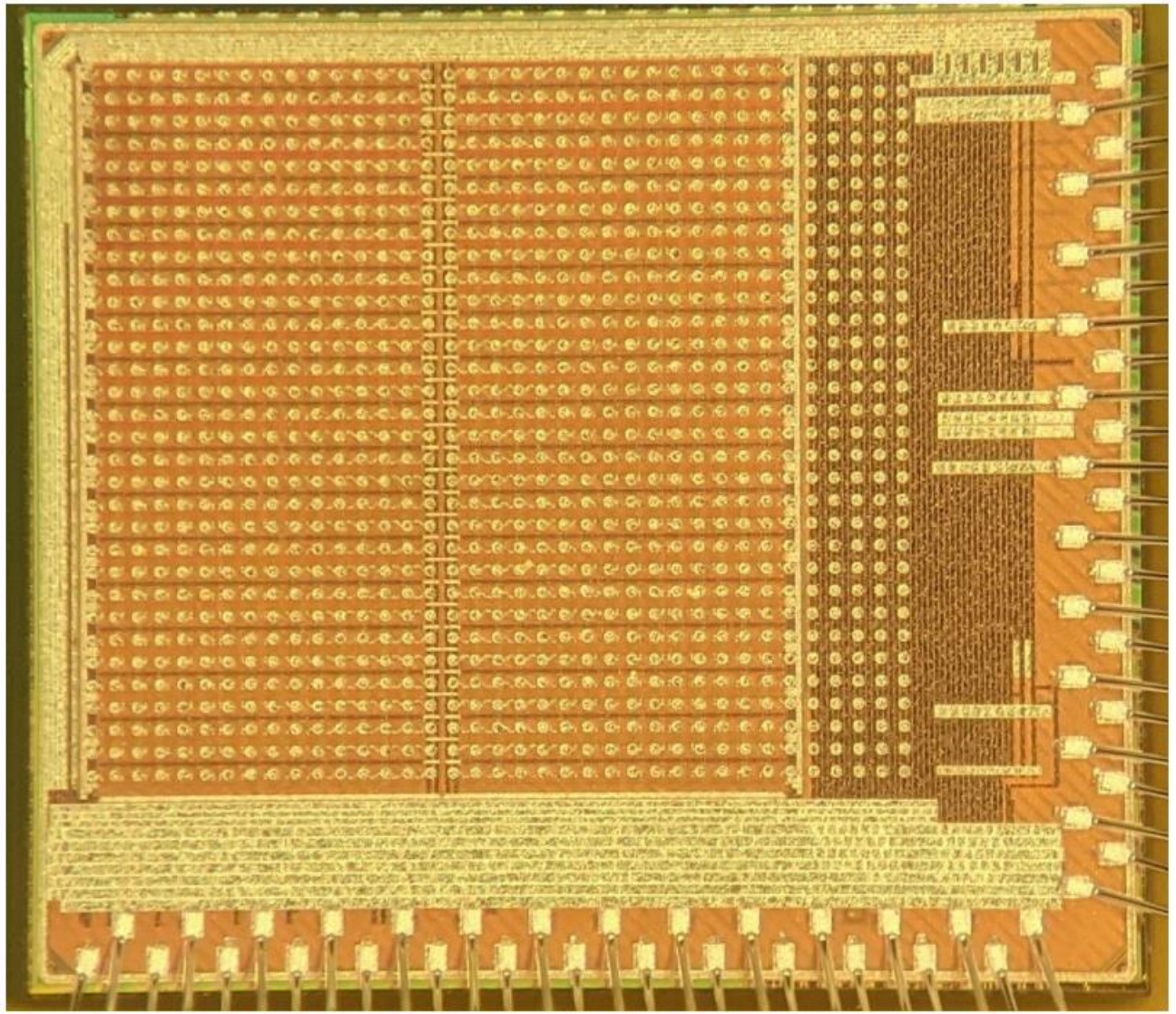


Wafer Layout



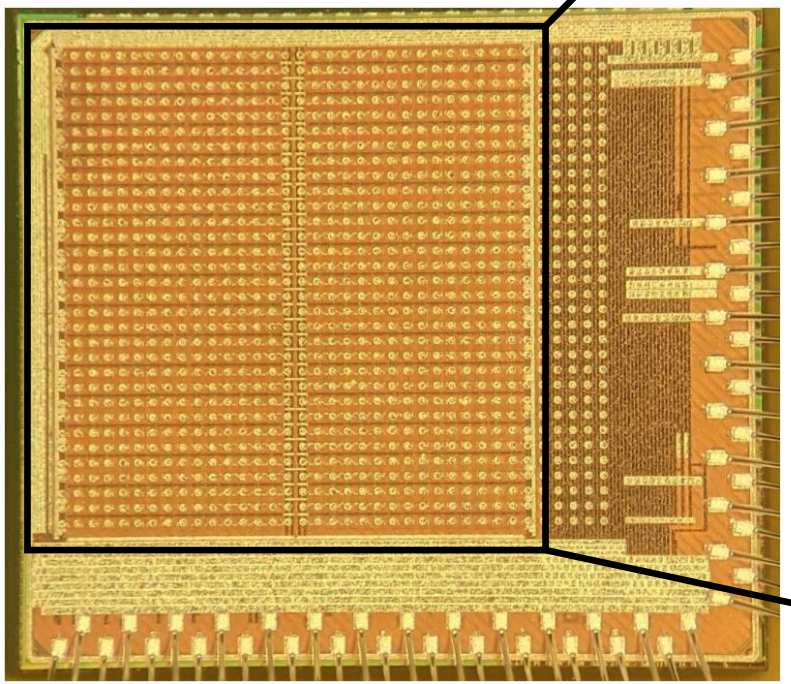
iLGAD Third Generation (4iLG3). Second Run

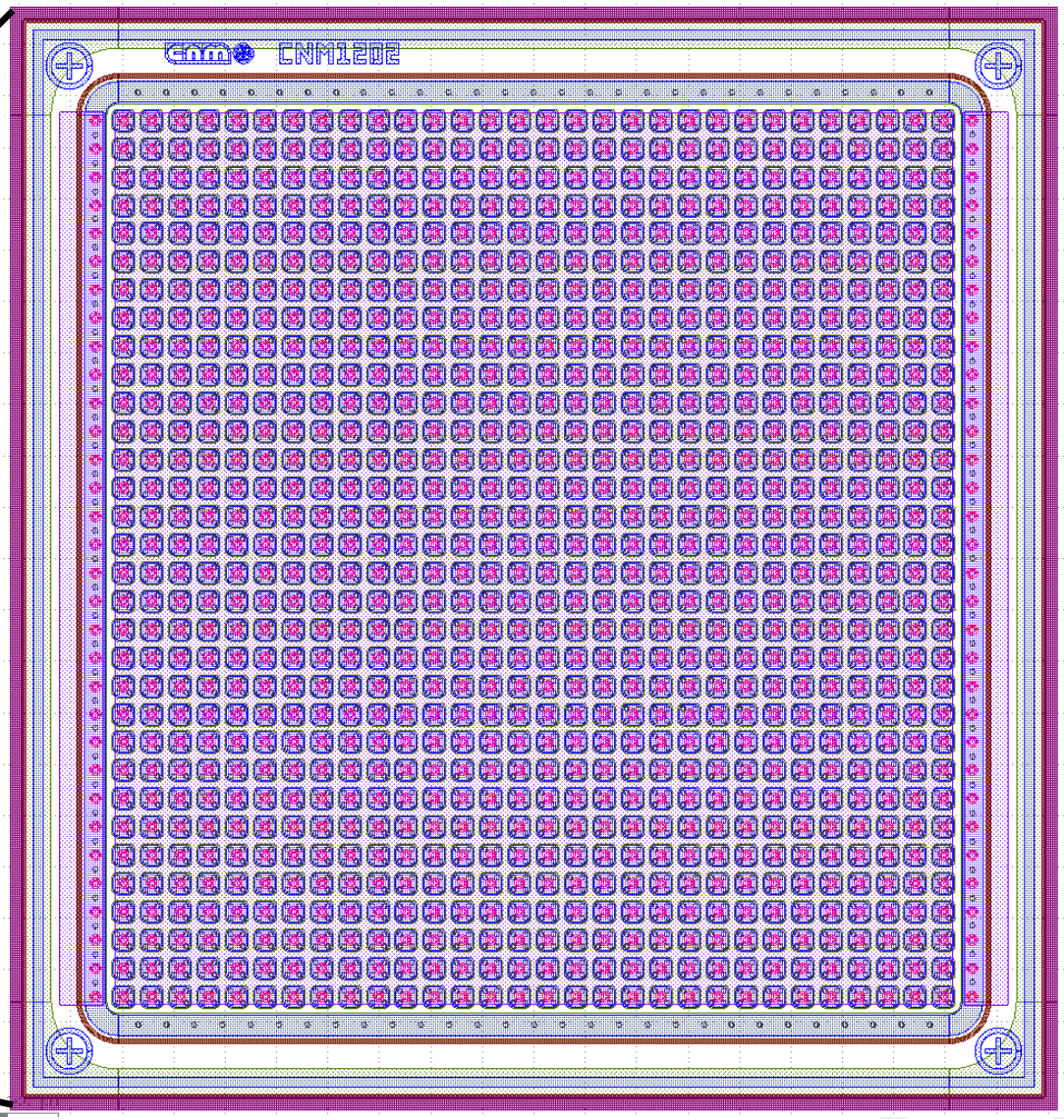
- **TimeSpot1**. 55x55 µm pitch, 32x32 pixels
- The **Timespot1 ASIC** is designed to provide a readout array suitable for chip-to-chip bump-bonding with a pixel size of 55x55 μm^2. It integrates 1024 channels, organized in a 32x32 matrix. The input channels are organized in two blocks of 512 pixels, each consisting of 2 groups of 256 channels.



iLGAD Third Generation (4iLG3). Second Run

- **TimeSpot1**. 55x55 µm pitch, 32x32 pixels
- The **Timespot1 ASIC** is designed to provide a readout array suitable for chip-to-chip bump-bonding with a pixel size of 55x55 µm2. It integrates 1024 channels, organized in a 32x32 matrix. The input channels are organized in two blocks of 512 pixels, each consisting of 2 groups of 256 channels.

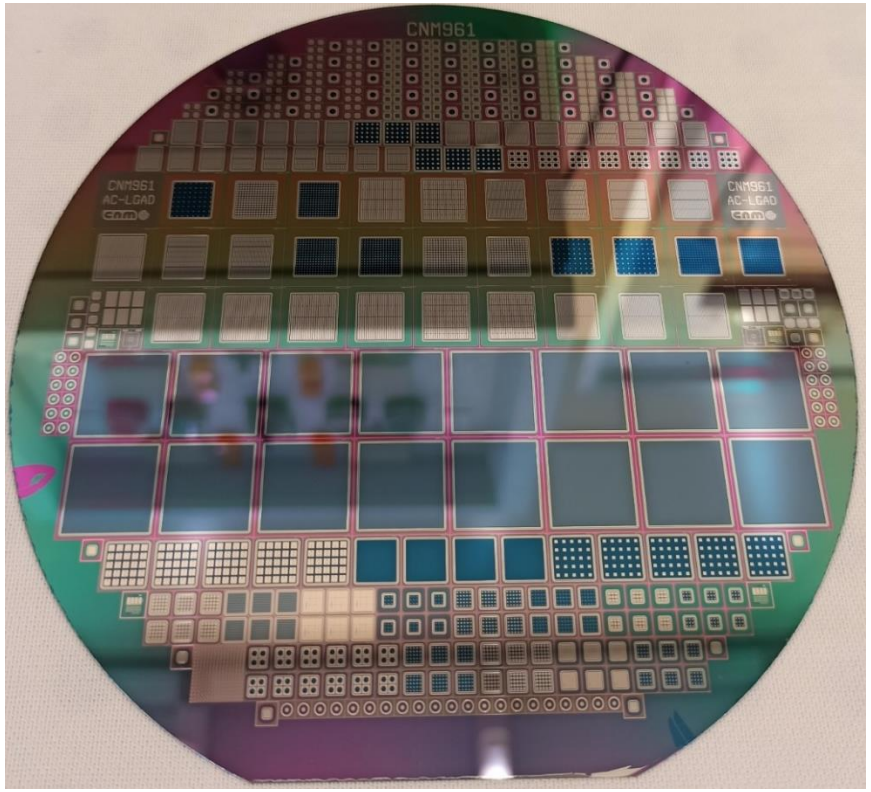


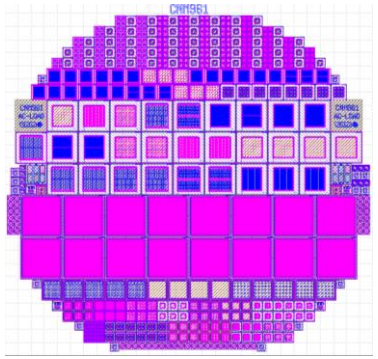


AC-LGAD (6LG4)

- Designed Structures (RUN 16020)
  - 443 Integrated structures
    - 42 Strip detectors
    - 16 Timepix3
      - 1 Timepix3 without gain
    - 5 HGTD, Pad size 0.5 mm
    - 5 HGTD, Pad size 1 mm
    - 61 DC-Pad diodes
    - 6 AC-Pad diodes
    - 12 DC-Arrays
    - 296 AC-Arrays

- **First deep LGAD at CNM** – 400keV Multi Implant.
- **Three different doses**
  - **Low – 2.0 e12/cm2**
  - **Medium – 2.1 e12/cm2**
  - **High – 2.2 e12/cm2**





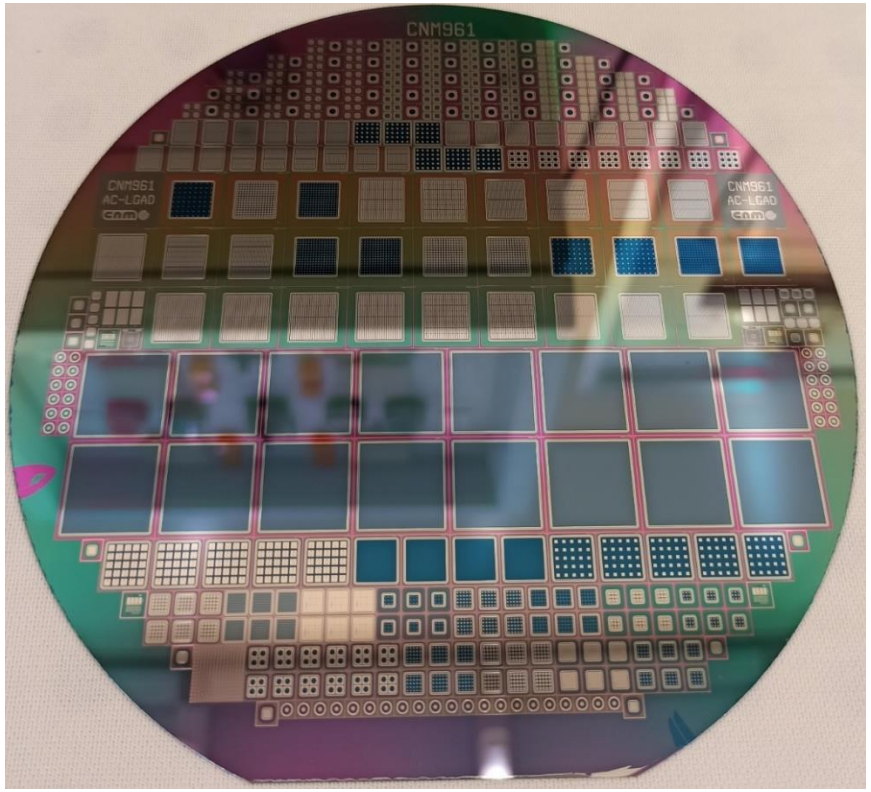
Broken

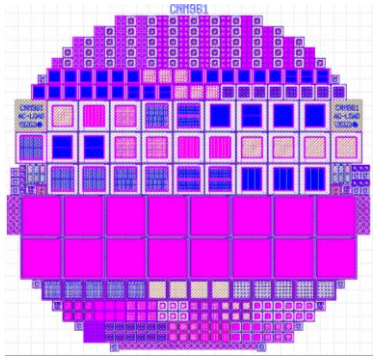
Further Processing Required

Wafer	Multi dose	Thickness
1	Low	Silicon 300 um
2	Low	Silicon 300 um
3	Medium	Silicon 300 um
4	Medium	Silicon 300 um
5	High	Silicon 300 um
6	High	Silicon 300 um
7	Low	Silicon 300 um
8	Low	Silicon 300 um
9	Low	SiSi 50 um
10	Low	SiSi 50 um
11	Medium	SiSi 50 um
12	Medium	SiSi 50 um
13	High	SiSi 50 um
14	High	SiSi 50 um
15	NA	Silicon 300 um

AC-LGAD (6LG4)

- Wafers 6,9 and 14 have been diced.
- Thick wafers (300um) show high current (mA/cm^2), but have a high breakdown voltage (900V)
- Thin wafers (50um) show low current with a breakdown around 500V.
- All wafers show low gain (< 2).
- Characterization underway for AC-coupled pixels.
- Wafers are to be sent for UBM this week, in total 3 50um wafers and 6 300um wafers.
- Wafer 7 to undergo a special backside process for ultra shallow junction using graphene.





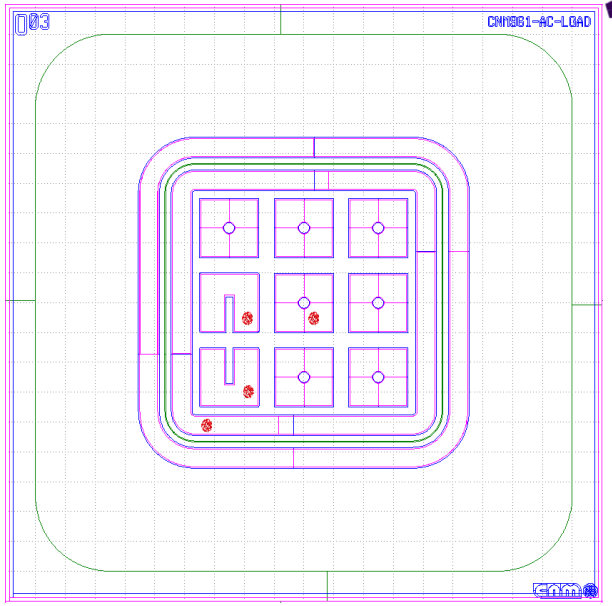
Broken

Further Processing Required

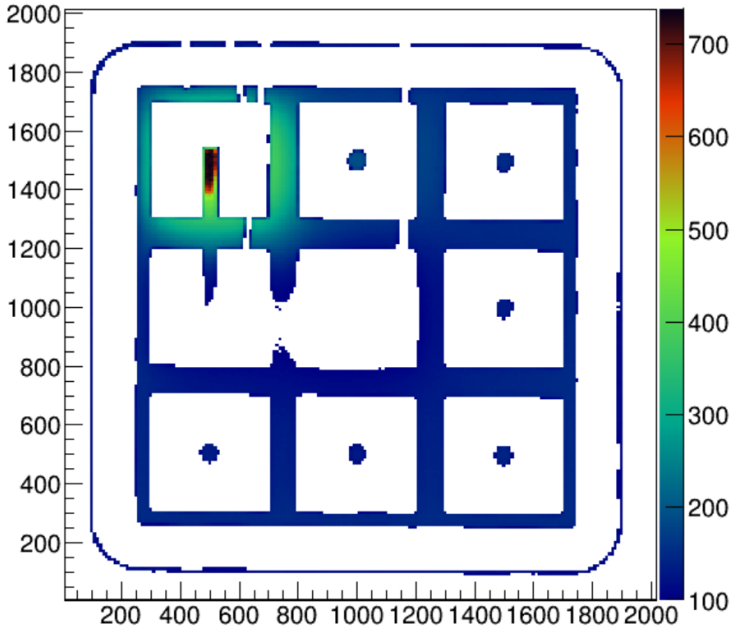
Wafer	Multi dose	Thickness
1	Low	Silicon 300 um
2	Low	Silicon 300 um
3	Medium	Silicon 300 um
4	Medium	Silicon 300 um
5	High	Silicon 300 um
6	High	Silicon 300 um
7	Low	Silicon 300 um
8	Low	Silicon 300 um
9	Low	SiSi 50 um
10	Low	SiSi 50 um
11	Medium	SiSi 50 um
12	Medium	SiSi 50 um
13	High	SiSi 50 um
14	High	SiSi 50 um
15	NA	Silicon 300 um

AC-LGAD (6LG4)

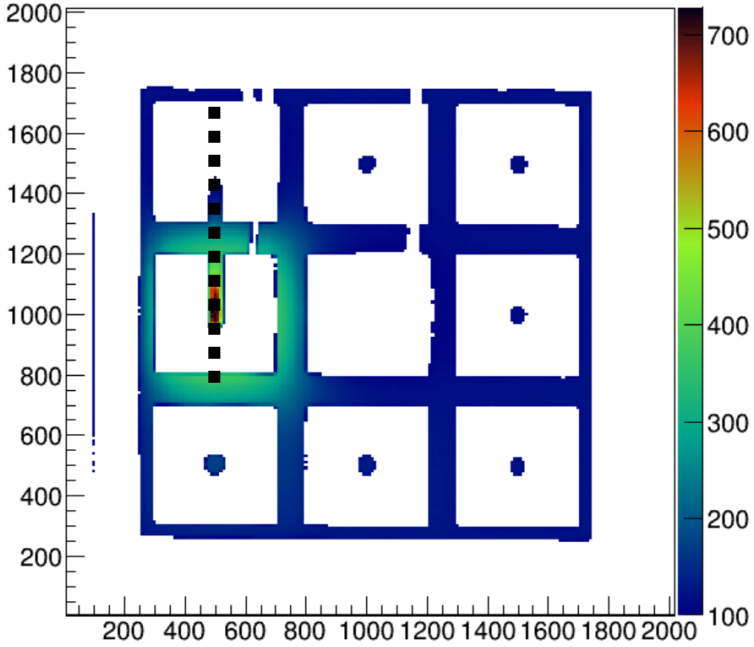
- First TCT results with IR laser.
- 2D scan performed to look at the response of 3 pixels.
- Pixels show a position dependant response.
- Preliminary results show AC-response.
- Work ongoing to determine AC-Response as a function of pixel size/pitch.

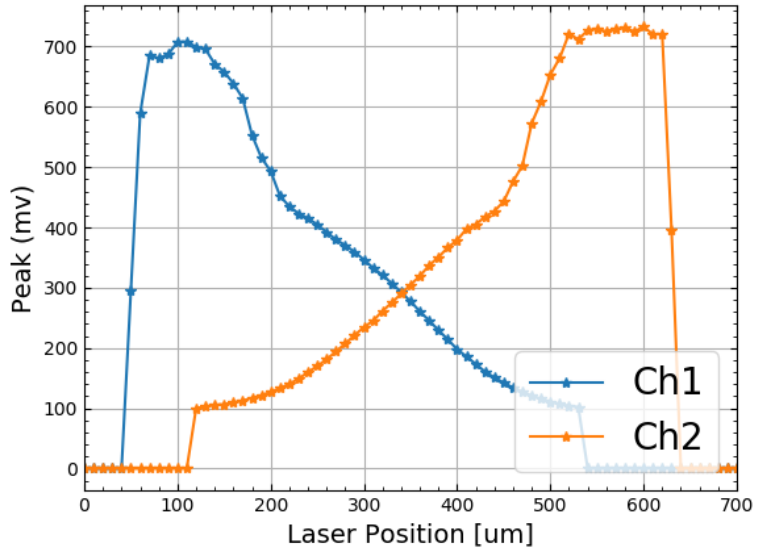


Ch1 Response



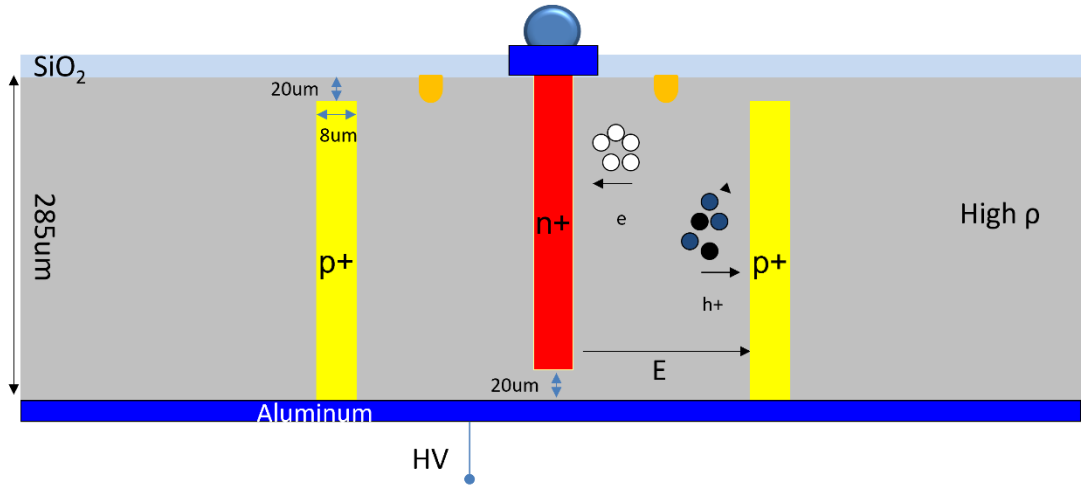
Ch2 Response

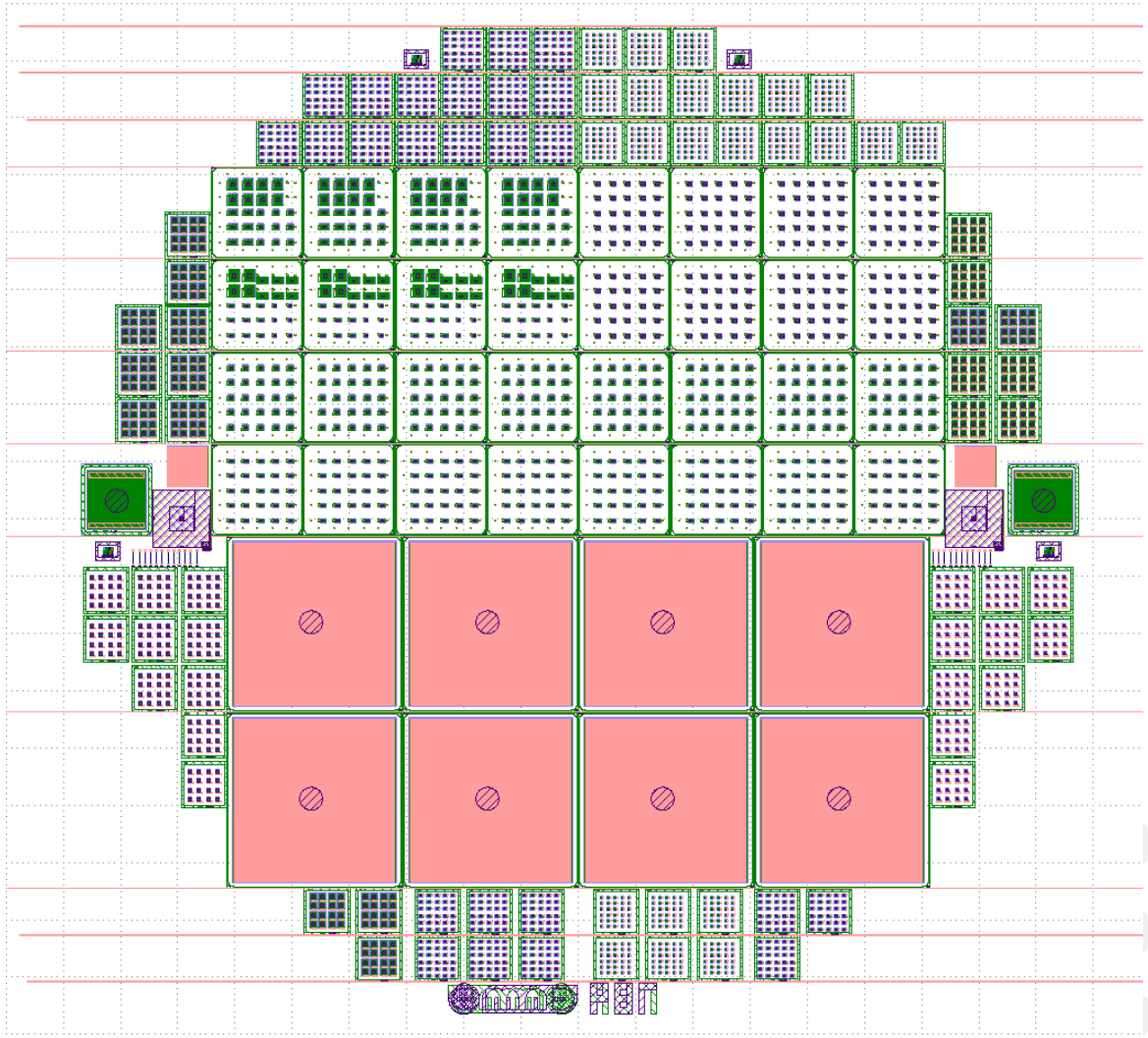




3D - DS Timing - Run 16069

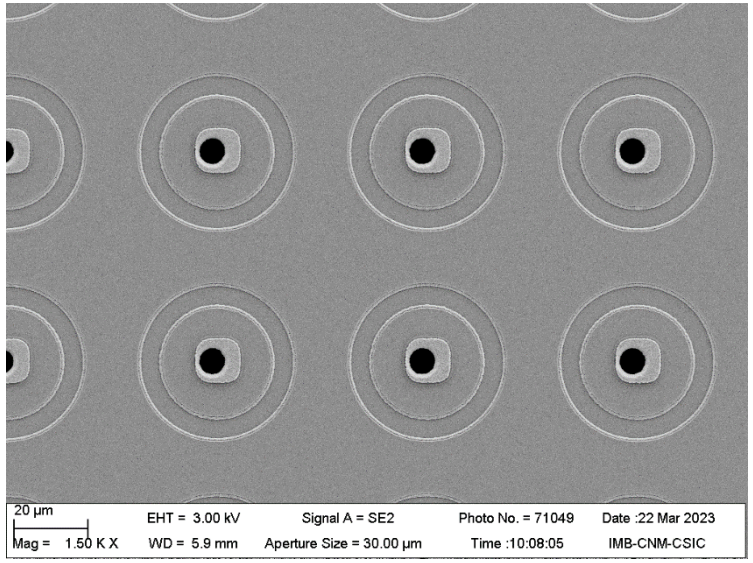
- Double sided technology,
- Wafer thickness : 285um +/-10um
- HRFZ silicon, p-type>5kohm*cm
- P-stop isolation.
- Holes diameter 8/10um
- Metal opening on the back

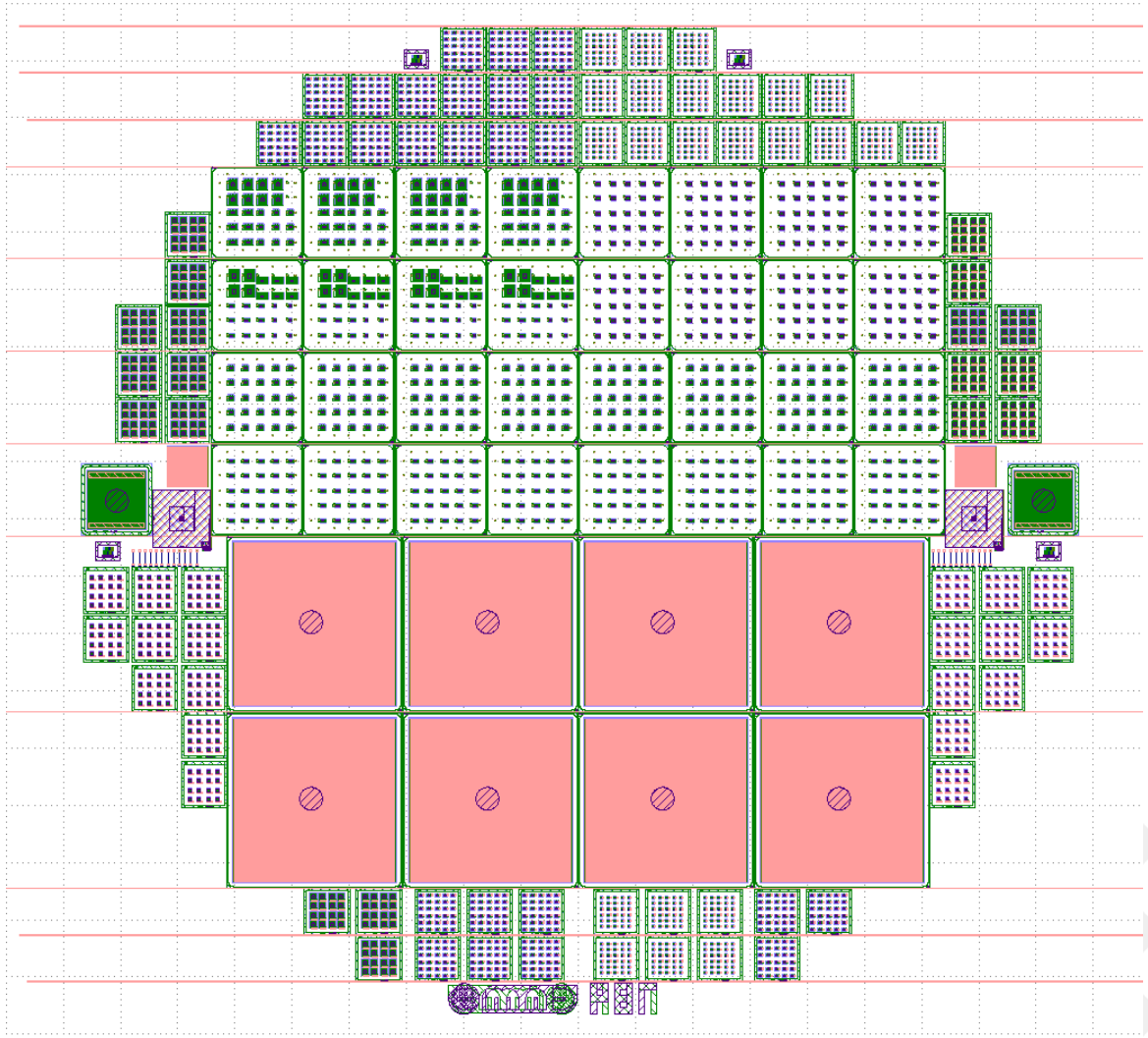




3D - DS Timing - Run 16069

- Run16069: 3 Wafers, 100 mm, CNM987 Mask Set
- Step 105/130
- MediPix3. 55x55 µm pitch, 256x256 pixels: 8 devices.
- Altiroc 1. 300x300 µm pitch, 40x45 pixels: 24 devices.
- 2 weeks are needed for its Production - Only requires the passivation layer.





Acknowledgement

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement No 101004761