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WAFER-TO-WAFER BONDING FOR ULTRA-THIN HYBRID PIXEL DETECTORS

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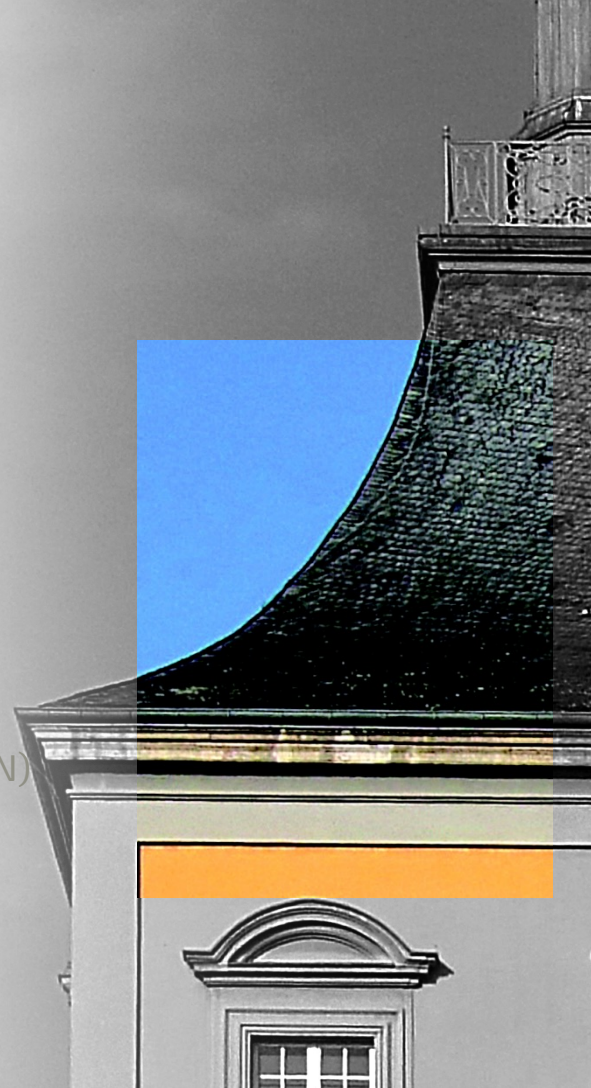
AIDAINNOVA 2ND ANNUAL MEETING,
VALENCIA, 24 -27 APR 2023



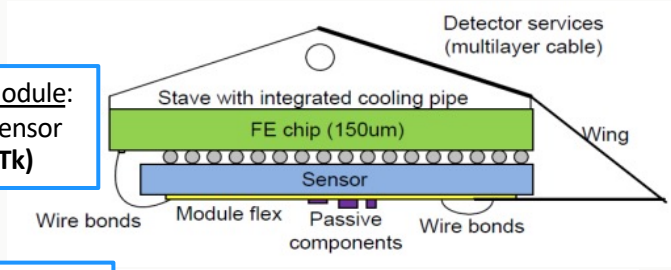
SHORT RECAP: THIN HYBRID PIXEL DETECTORS

- Want to reduce mass, i.e. thickness of pixel detectors as much as possible while keeping the benefits of the hybrid approach:
  - Separate development and optimization of sensors and FE electronics allowing for best performance of FE electronic and sensor.
  - Fine pitch interconnection between FE and sensor pixel with a pitch down to ~20µm.
  - Thinning of FE and sensor parts to the minimum.
  - Can benefit from active CMOS sensor development by integrating some electronic already into the sensor

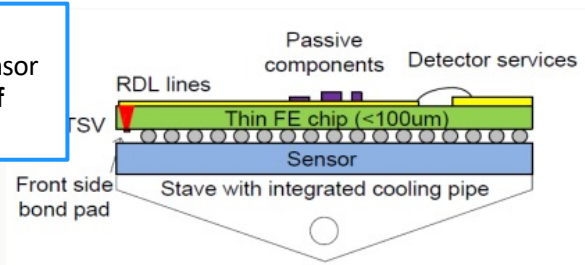
→ Target is the development of ultra-thin hybrid pixel detectors based on:

  - 50 – 100 µm thick pixel sensor on 200 (300) mm CMOS wafers
  - ~20 µm thick pixel FE chip thickness on 200 (300) mm CMOS

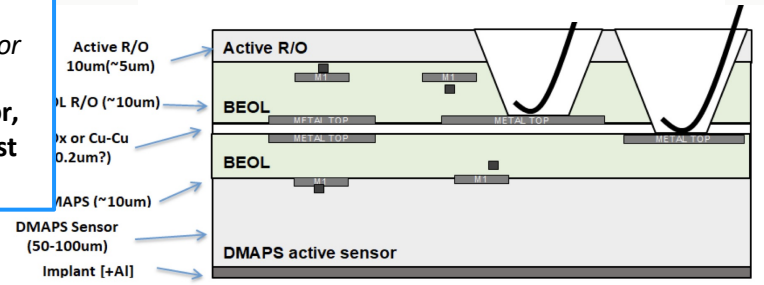
Standard hybrid pixel module:
150 µm FE & 150 µm sensor
2013 (ATLAS IBL & ITk)



TSV hybrid pixel module:
80 -100 µm FE & 150 µm sensor
2019 (AIDA 2020 proof of concept)

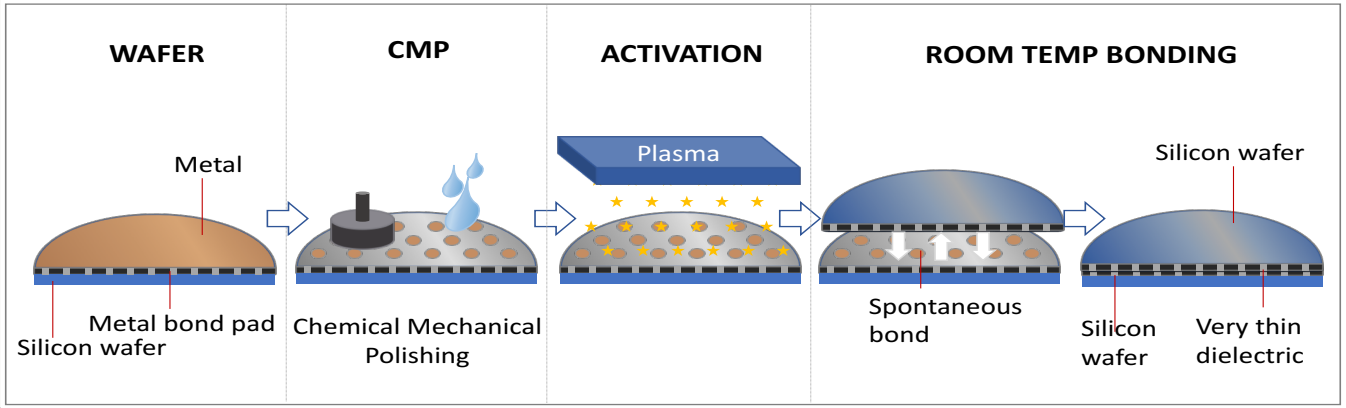


Ultra thin hybrid pixel module:
~20 µm FE &
50 -100 µm sensor
2025 (future tracking detector, esp. in innermost layers)



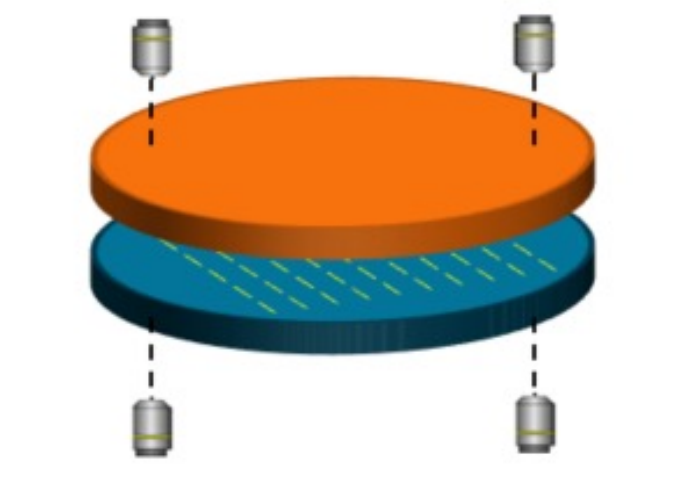
ULTRA THIN HYBRIDS: ENABLING TECHNOLOGIES

- Wafer-to-Wafer bonding between R/O and sensor wafer:
  - Main objective of this project to choose and develop the process for fine pitch W2W bonding with sensor and FE electronic wafers of 200 and 300 mm size.
- Thinning and backside processing of bonded wafer-wafer assembly:
  - Thinning on wafer level is easy, but might need backside process of the sensor backside, i.e. backside implantation and metallization
- Opening and connection to the R/O chip pads (I/0 and power) from the backside after thinning:
  - similar to the TSV pixel module project already demonstrated during AIDA-2020.



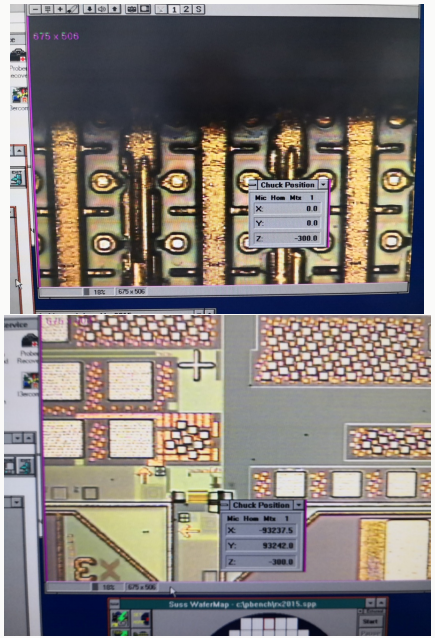
PROOF OF CONCEPT PROJECT FOR AIDAINNOVA

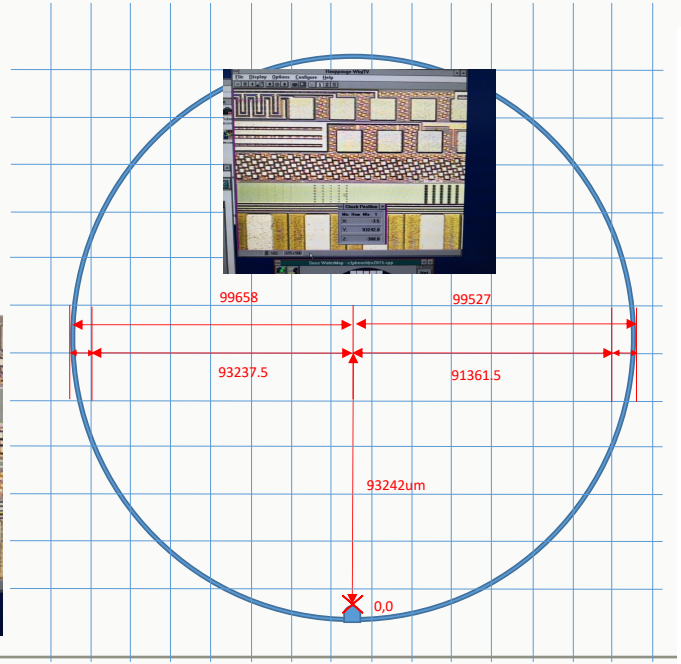
- Develop dedicated CMOS Sensor wafer compatible with a pixel FE chip wafer:
  - Starting point: passive CMOS sensor development on 200 mm wafer with 110/150 nm process node from LFoundry
  - Decided to use TimePix3 chip wafers (GF 130 nm on 200 mm wafers)
  - Keep own FE development on the same wafer as the sensor as backup option
- Developing and optimization of hybridization process including thinning and interconnection from chip's backside at IZM.
- Longer Term: Transfer process to more modern feature size pixel chips (65nm or 28 nm on 300 mm wafers) for smaller pixel pitches and faster electronics

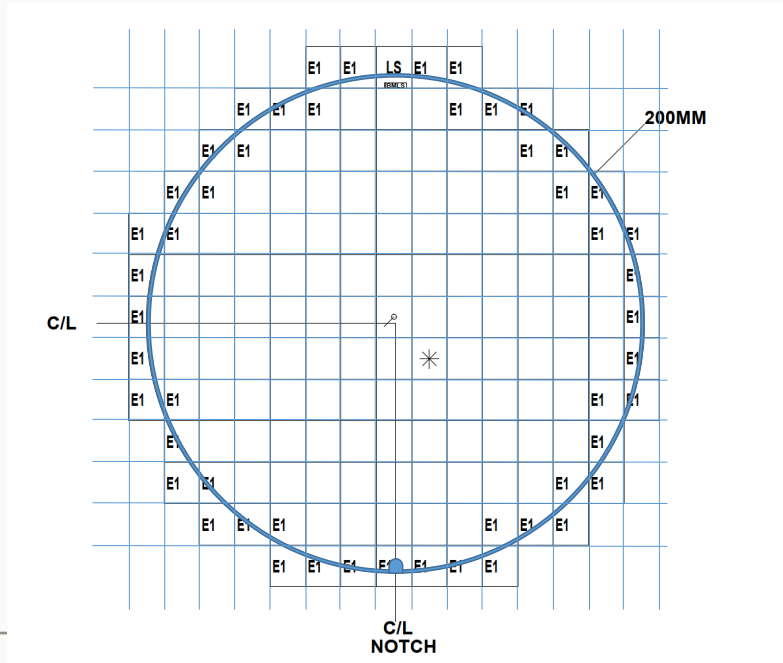


TIMEPIX 3 WAFER EVALUATION

- TimePix3 Wafer have been checked to be compatible with W2W bonding:
  - Several wafers have been measured to confirm the reticule stepping is the same for all wafers
  - Wafer topography have been checked in detail by IZM and TimePix collaboration



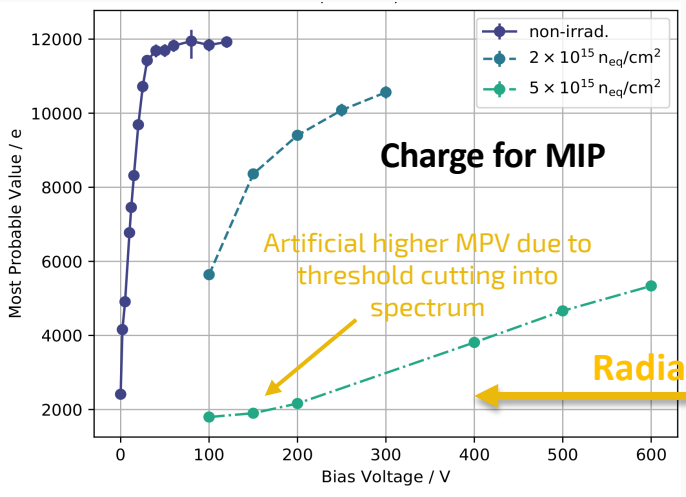


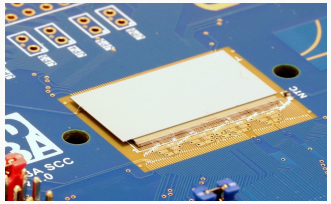


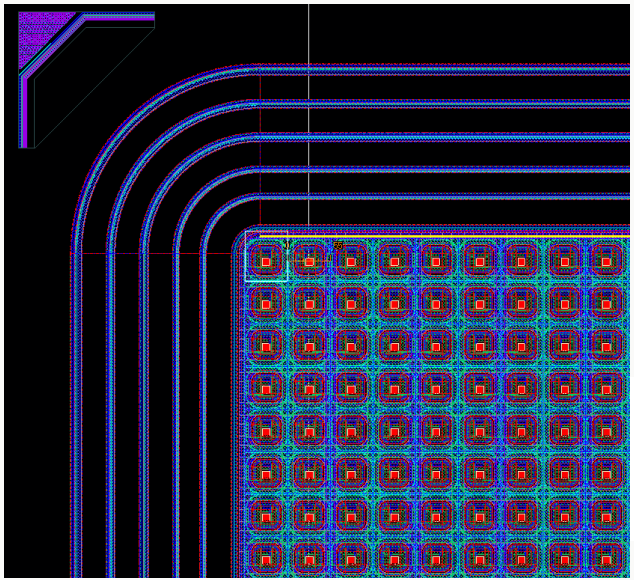
pictures by M. Campbell et al.

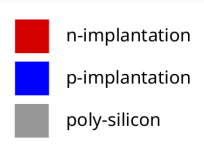
SENSOR WAFER DESIGN

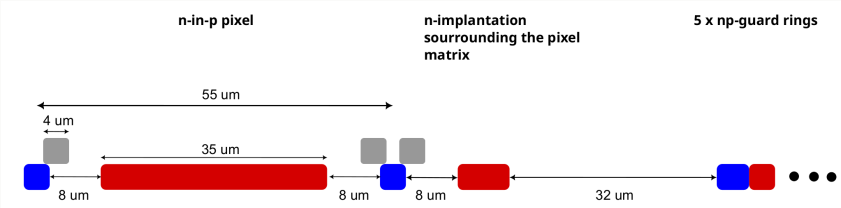
- Layout is derived from former passive CMOS sensor submissions
  - Increase n-implant width from 30 um to 35 um in order to match 55 x 55 pixel
  - 5 x n-p guard ring structure
  - Bias grid + DC-coupling with bias resistor (4 – 5 MΩ)



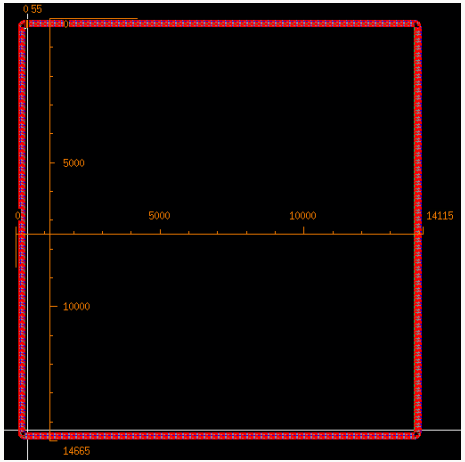






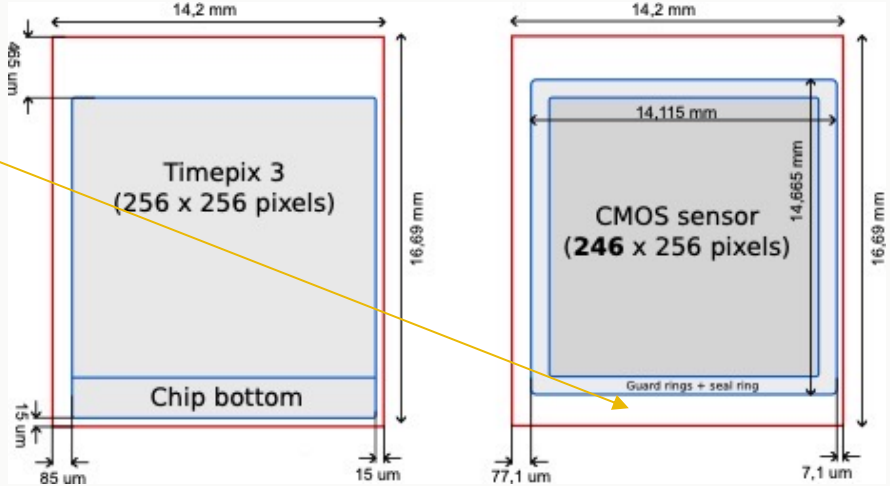


SENSOR WAFER DESIGN



- CMOS sensor has to fit into same reticule as TimePix3 chip
  - use only 246 pixels in horizontal axis, instead of 256

    → All chips can be used after dicing
- Smaller sensor pixel matrix is not a problem for sensor or TimePix chip
- Few things still to be defined:
  - TSV etching through TimePix3 chip such that chip pads are accessible from chip backside
  - sensor backside HV contact requires the usage of fully processed sensors incl. thinning, backside implantation and metallization for the W2W bonding process
- Status:
  - Design ready only a few design rule checks missing
  - Dicsussion with foundry aboute quote and details of the submission



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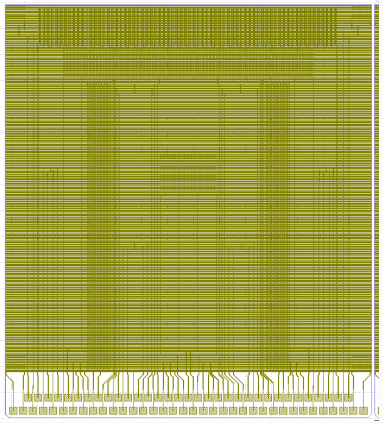
W2W BONDING PROCESS DEVELOPMENT AT IZM

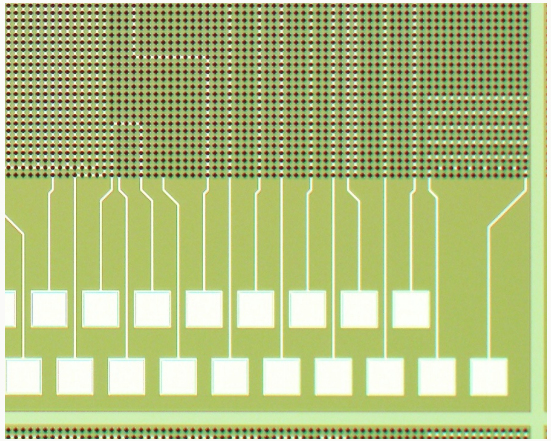
- **WP1: Design development and manufacturing of process qualification wafer, design preparation of functional TIMEPIX3 and DMAPS sensor wafer**
  - 1.1 Definition of technological approach for ultra-thin low-mass hybrid pixel detectors
  - 1.2 Process qualification design including test structures
  - 1.3 Fabrication of process development wafer
  - 1.4 Design and mask preparation for TIMEPIX3 readout electronics and DMAPS active sensor wafer
- **WP2: Wafer bonding and thinning process**
- **WP3: Wafer bonding with capacitive coupled IOs and conductive IOs**
- **WP4: Backside wafer process with TSV-etching and backside metallisation process**

WP1: PROCESS DEVELOPMENT - DESIGN

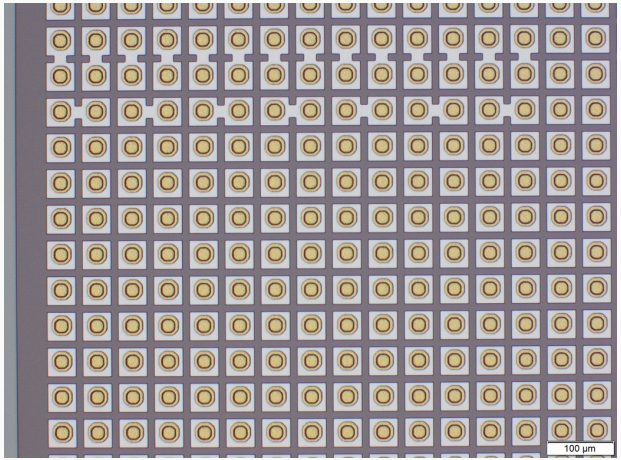
Basic Design – MEDIPIX3 adapted Daisy Chain Design

- Design input: MEDIPIX adapted test design used for Indium bump bonding process development
- Daisy Chain Layout for sensor und ROC chip available
- Electrical measurement of single interconnects, daisy chains and open/short structures included





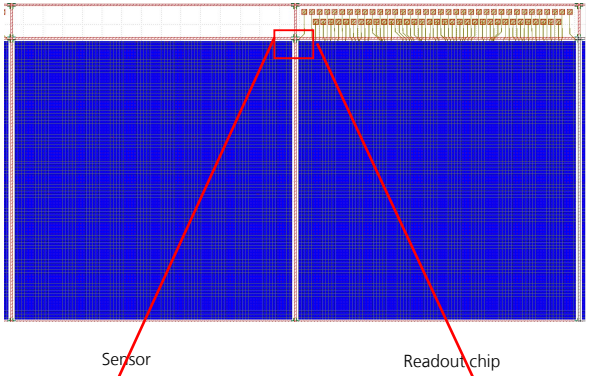
Daisy Chain Readout Chip (ROC) with probe pads

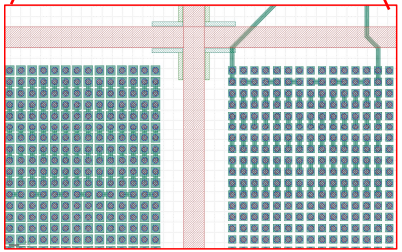


Daisy Chain Sensor Chip

WP1: PROCESS DEVELOPMENT - DESIGN

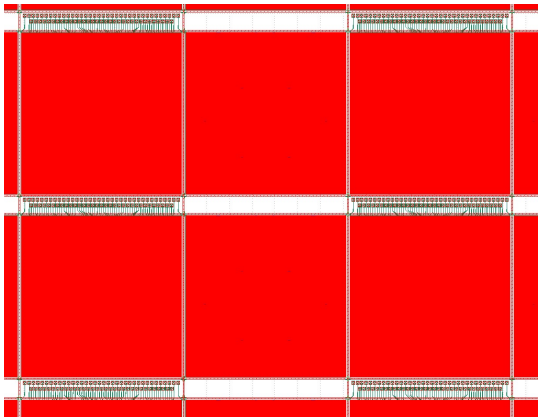
Reticule



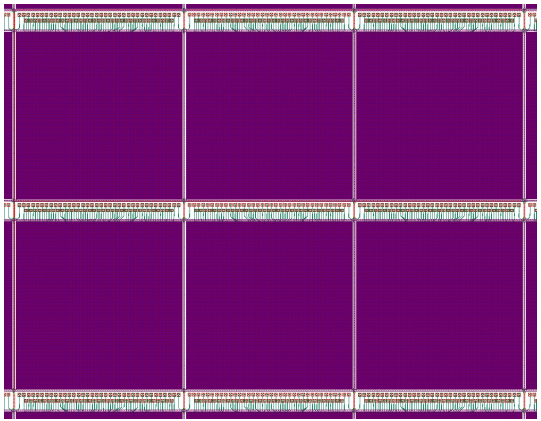


Sensor and Readout chip
Daisy chain corner feature

Full wafer design – wafer to wafer bondable



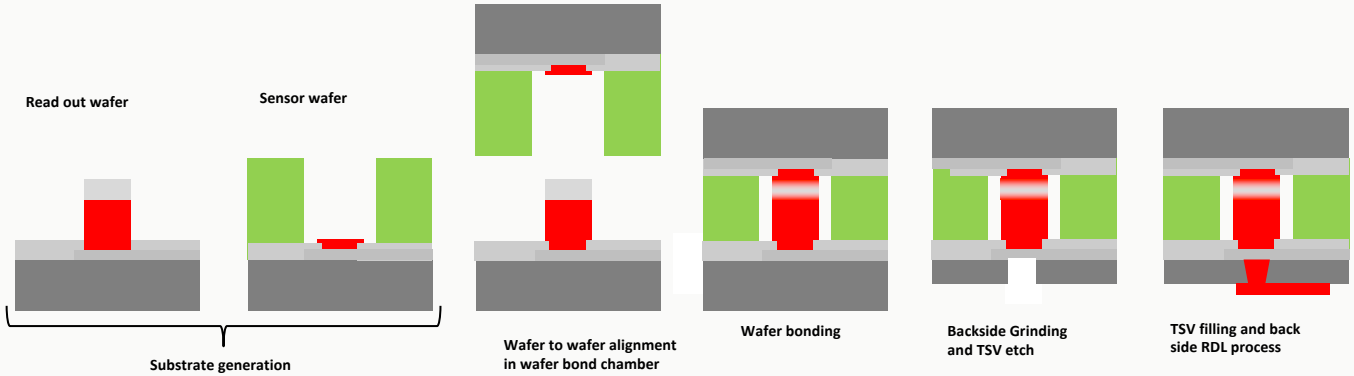
- Single wafer



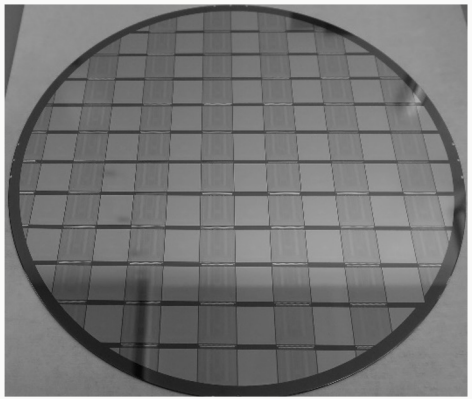
- bonded wafer

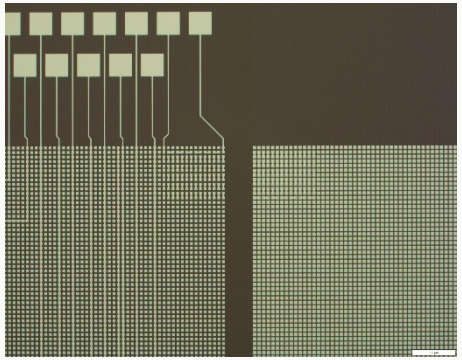
GENERAL PROCESS FLOW

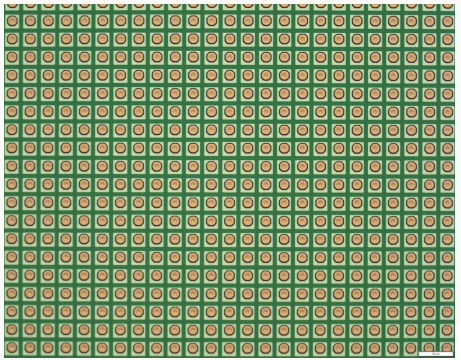
- The Cu/Sn wafer bonding is a well established process
- The Cu/Sn bond will be supported by spin coated, photo-structured polymer layer which is joined simultaneously (polymer hybrid wafer bonding)
- Depending on total wafer stack thickness a mechanical support during TSV formation and backside RDL process will be required



TECHNOLOGY SETUP WAFER: IZM RUN 2022_250 AL RDL

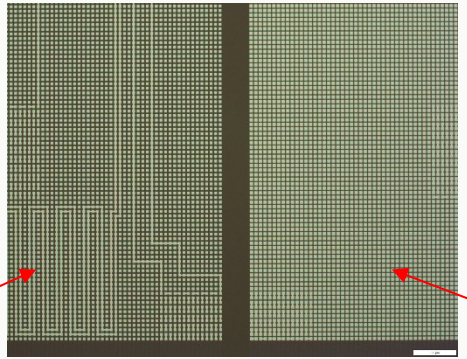






Top Wafer UBM Pads

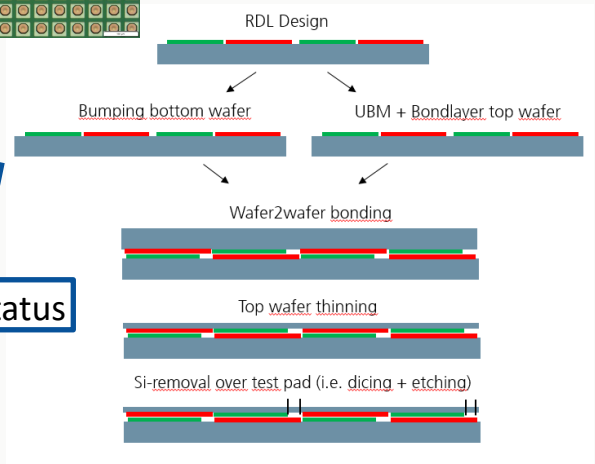
- Al-RDL with oxide passivation
- Design wafer cantered for W2W bonding process development



Daisy Chain ROC Chip

Daisy Chain Sensor Chip

Current process status



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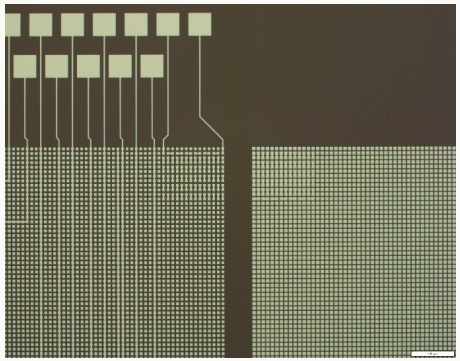
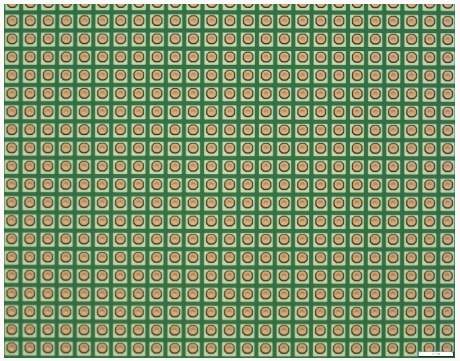
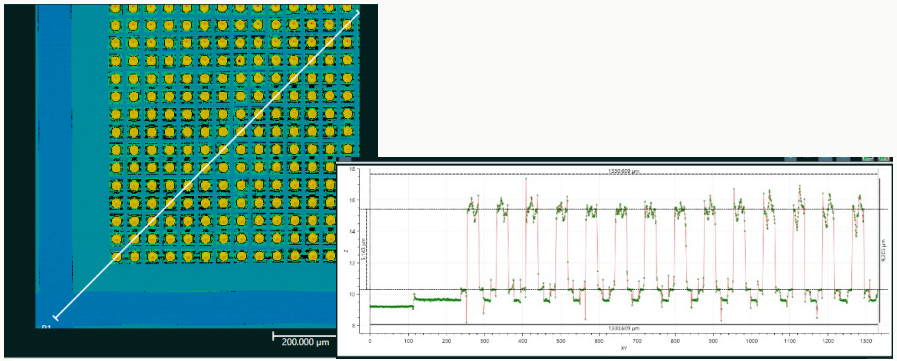
TECHNOLOGY SETUP WAFER



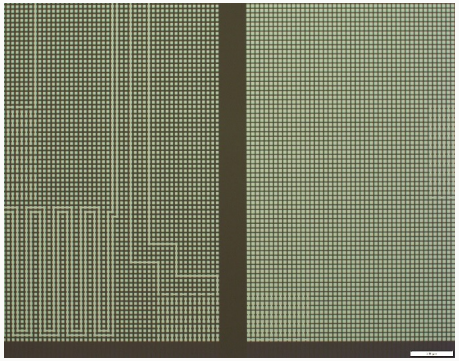
Al RDL top wafer



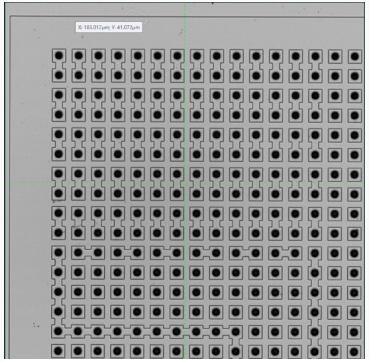
Top Wafer UBM Pads



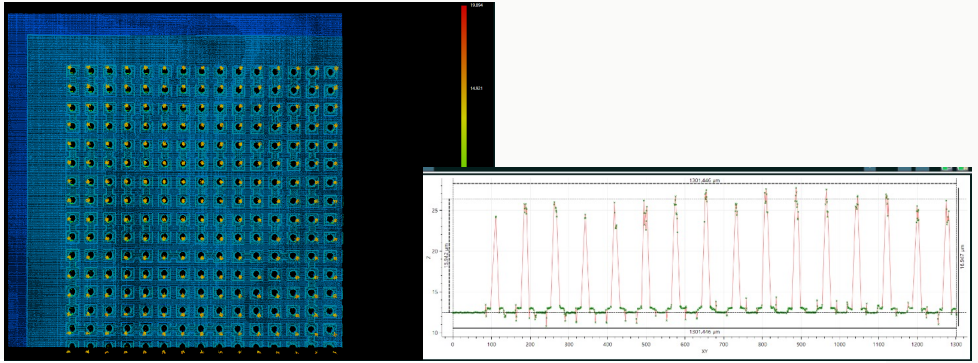
UBM topography measurement: UBM height ~5µm



Al RDL bottom wafer



Top Wafer Cu-SnAg bumps
(plating base still present)

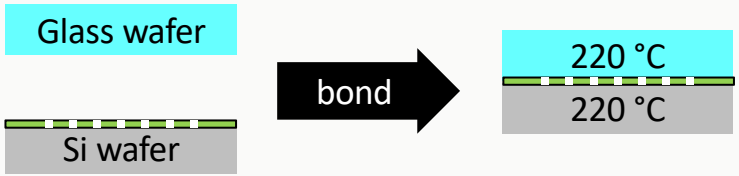


Bump topography measurement. Bump height ~14µm

BOND POLYMER MATERIAL EVALUATION

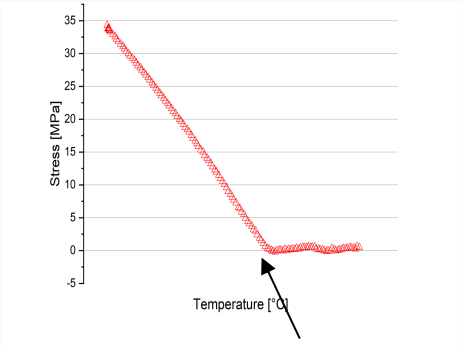
- Evaluate photosensitive polymers for CD down to 30 µm from different vendors
- Check void free bonding with photo-patterned polymer
- Prove the compatibility with the Cu/Sn solder process conditions

W2W Bonding Test:



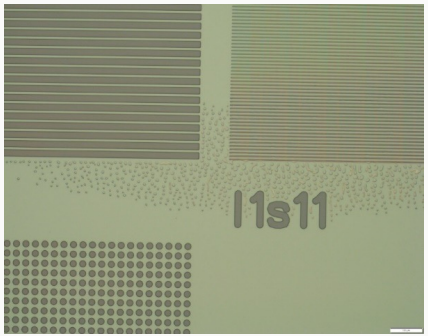
Sn-reflow temp.
@ ~220 °C

Material behaviour:



Softening point → material becomes sticky for bonding

Bond results:

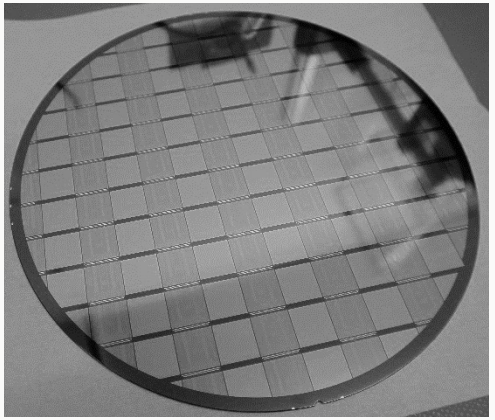


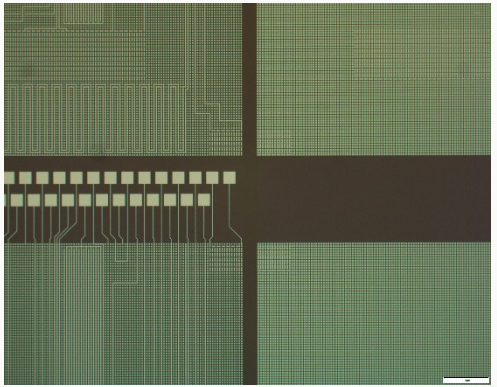
W2W bonding of a patterned polymer layer, looking through the glass wafer

STATUS + NEXT STEPS

- Current status:
  - Top wafer UBM metallization finished + topography scan ongoing
  - Bottom wafer in pillar bumping process
  - Polymer material screening:
    - material which was intended to use is not available anymore (R&D stopped)

    → 2 alternative polymer materials identified which are currently under test
- Next steps:
  - Finishing pillar metallization on bottom wafer + topography scan
  - Polymer material screening and test of alternatives





MILESTONE WP 6 MS25

- MS25 “Availability of parts and definition of technologies for wafer-to-wafer hybridization” is considered achieved with the daisy chain wafers as sensor replacement for the use of the process development at IZM
- Milestone report prepared and feedback from internal reviewers addressed
- Submitted and accepted

AIDA innova

AVAILABILITY OF PARTS AND DEFINITION OF TECHNOLOGIES FOR WAFER-TO-WAFER HYBRIDIZATION

Date: xx/xx/2022

Grant Agreement No: 101004761

AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

AVAILABILITY OF PARTS AND DEFINITION OF TECHNOLOGIES FOR WAFER-TO-WAFER HYBRIDIZATION

MILESTONE: MS25

Document identifier:	
Due date of milestone:	End of Month 18 (September 2022)
Report release date:	xx/xx/2022
Work package:	WP6: Hybrid Pixel Sensors for 4D Tracking and Interconnection Technologies
Lead beneficiary:	UBONN
Document status:	Draft [Final when fully approved]

Abstract:

Within WP6 (Development of Monolithic Active Pixel Sensors) Milestone MS25 contains the availability of parts and definition of technologies for wafer-to-wafer hybridization.

This milestone has been successfully achieved and is reported.

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SUMMARY

- Project has achieved clear progress over the last months:
  - Timepix3 wafers are at IZM and has been proven to be suitable for the W2W bonding process
  - Sensor wafer design is well advanced and processing of dedicated sensor wafers will start soon
  - W2W technology definition is completed and process development at IZM is ongoing
  - Test batch with daisy chain wafers has been produced and process development run is ongoing at IZM
- MS25 *"Availability of parts and definition of the technologies for wafer to wafer hybridization"* is now fully completed
  - Milestone report has been delivered in 12/2022 to management
  - Real sensor wafers are only required after WP1 have been completed in ~9-12 months and LFoundry sensors wafers will be available not before Q3/Q4 2023
  - Final deliverable of thin hybrid pixel prototype detectors is not at risk yet