CoolFPGA: results from experiments and simulations

G. Baldinelli, M. Boscardin, F. Bosi, A. Coccaro, M. Crivellari, P. Francavilla, P. Mammini, M. Massa, F. Palla, C. Turrioni

on behalf of the INFN Perugia, Pisa and Genova and FBK Cool FPGA group

WP10 – advanced mechanics for tracking and vertex detectors

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CoolFPGA - Microchannels on the surface of the die

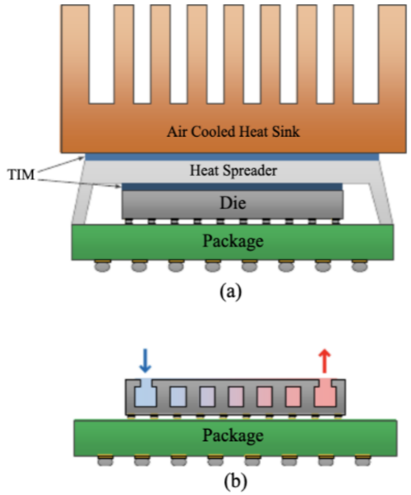
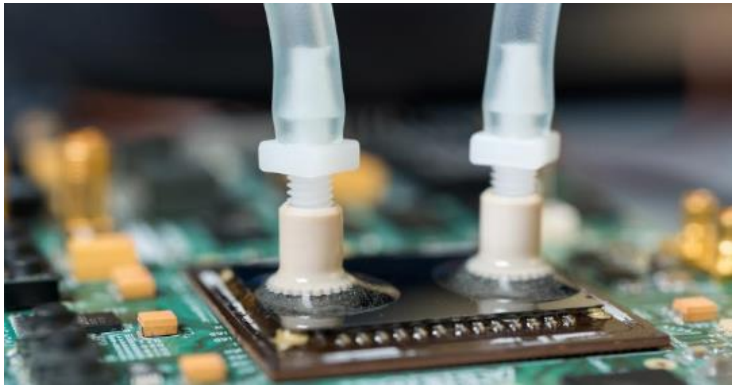


Fig. 1. (a) Traditional microelectronic system (b) Microelectronic system with monolithically integrated microfluidic heat sink



***Pros compared to traditional heat-sinks*:**

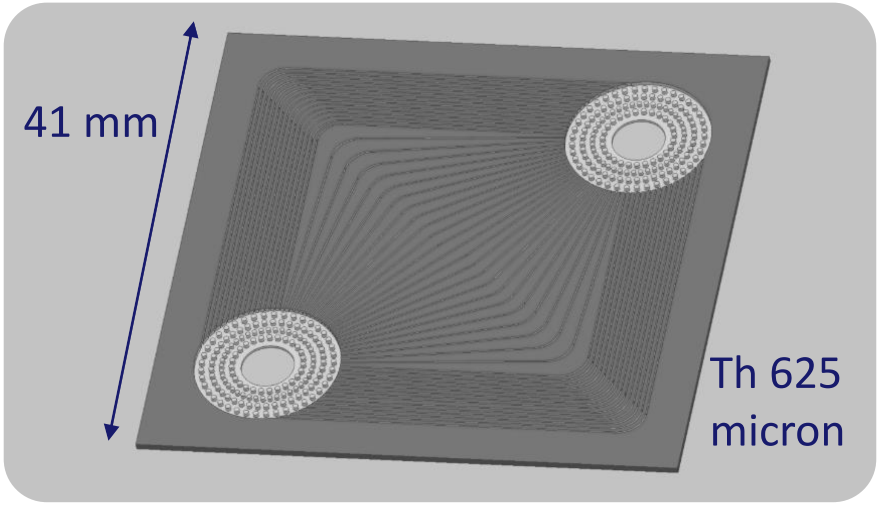
- ✓ More efficient way to cool down the device (e.g. high surface/volume ratio, low thermal resistances between the fluid and the circuit dissipating power)
- ✓ Less obstruction for traditional air-based cooling for other boards components
- ✓ It overcomes limitations on device density on PCB due to the limited air-based cooling capability of crates

***Cons compared to traditional heat-sinks*:**

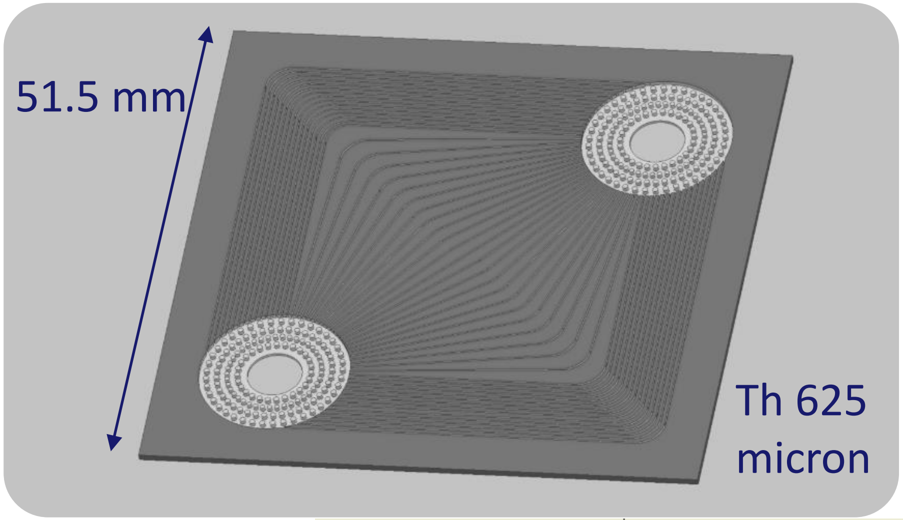
- ✗ Risks due to manipulation of the bare die
- ✗ Probably less suitable for large scale systems (in case we need to manipulate O(1k) devices)

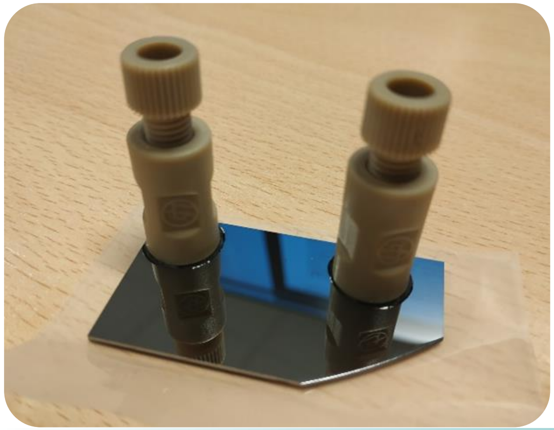
CoolFPGA – Specifications & Status

Silicon - DRIE process for CHIP XILINX KINTEX ULTRASCALA XCKU040



Silicon - DRIE Process for CHIP INTEL STRATIX10 MX

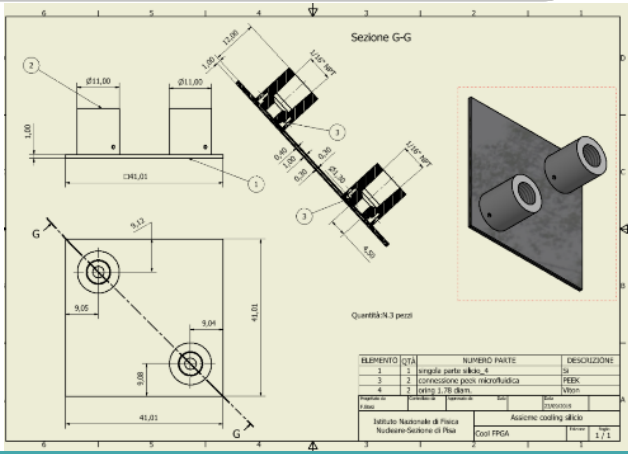




Specific peek connection By Cole-Parmer Company on a test structure

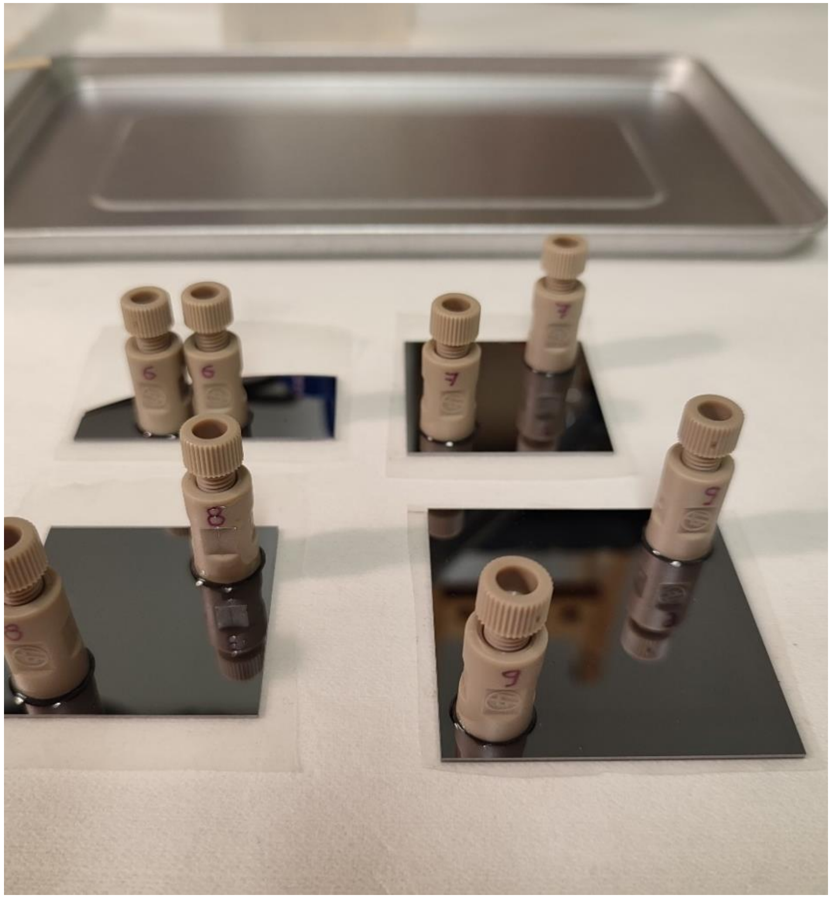
Tested Plugs in silicon and pyrex

General assembly for 41 mm silicon



CoolFPGA – Tests

4 samples: double sheet of silicon

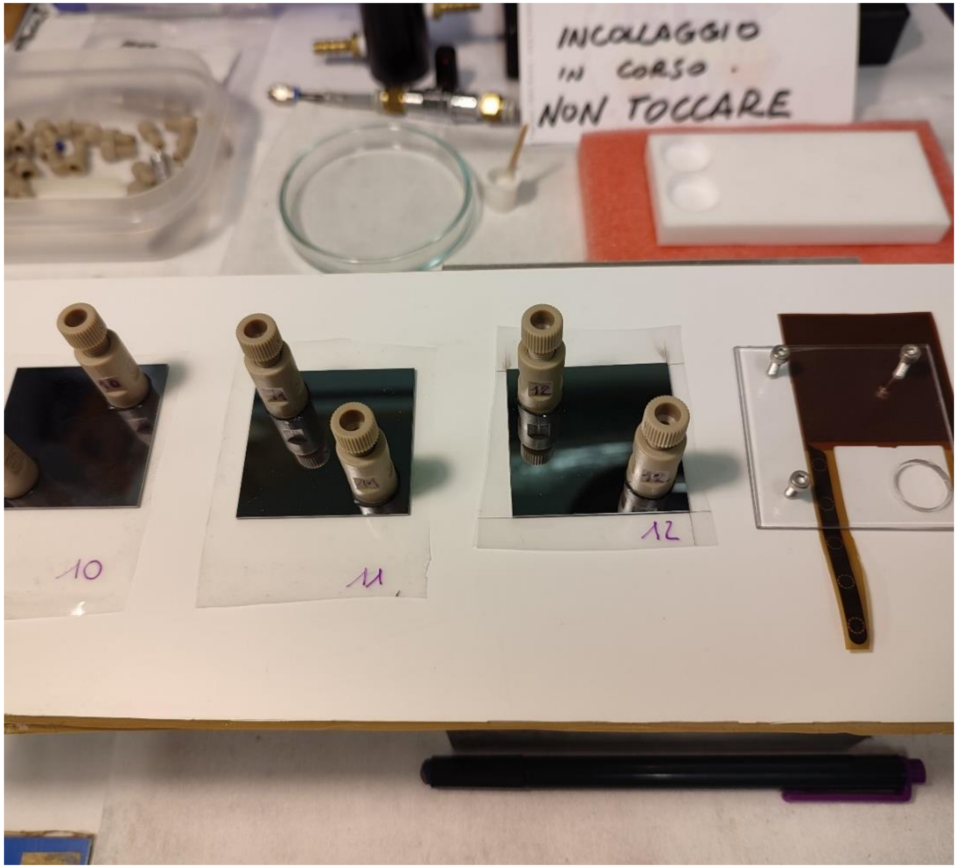


Load and breaking tests have been caried out, inserting pressurized liquid which demonstrated extreme fragility of the bond between the two layers of silicon.

None of the specimens resisted at pressures higher than 1 bar.

Each sample showed showy cleavages with relative leakage of liquid.

4 samples: double sheet of silicon



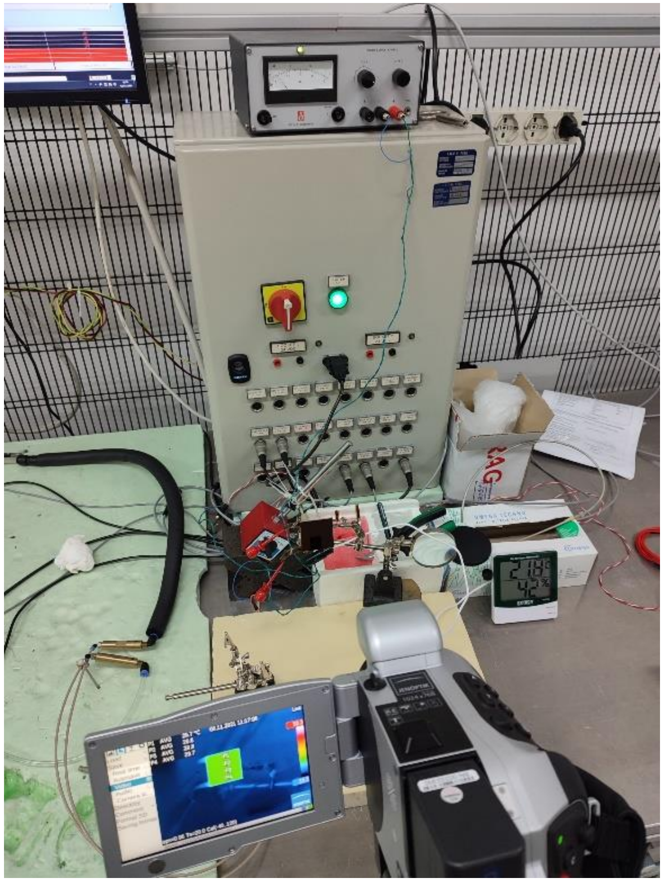
The idea of the silicon double layer has been abandoned.

3 more specimens have been assembled: silicon - pyrex (300 μm) type.

Samples equipped with heaters for the simulation of electronics, glued with Masterbond EP30TC, a thermally conductive glue.

CoolFPGA – Tests

Setup



Temperature detected with an infrared camera at a distance of 30 cm;
Temperature of the external environment = 21.4°C;
relative humidity = 51%;
Sample emissivity = 0.96.

Power test

Samples 4x4 =**16 cm^2**;
Cooling liquid (Novec 7100) at 5°C, mass flow rate = 0.33 kg/min;
Voltage an current increased to reach the desired dissipated power.

Coolant at 5°C, mass flow rate = 0.33 kg min.

- 1 W/cm^2; theoretical: 16 W
- **18.8 V; 0.85 A = 15.98 W** real
- **$T_{average}$ 5 points: 18.9°C**
- **Liquid pressure**:
  Inlet 3.43 bar; Outlet -0.03 bar

CoolFPGA – Tests

Coolant at 5°C, mass flow rate = 0.33 kg min.

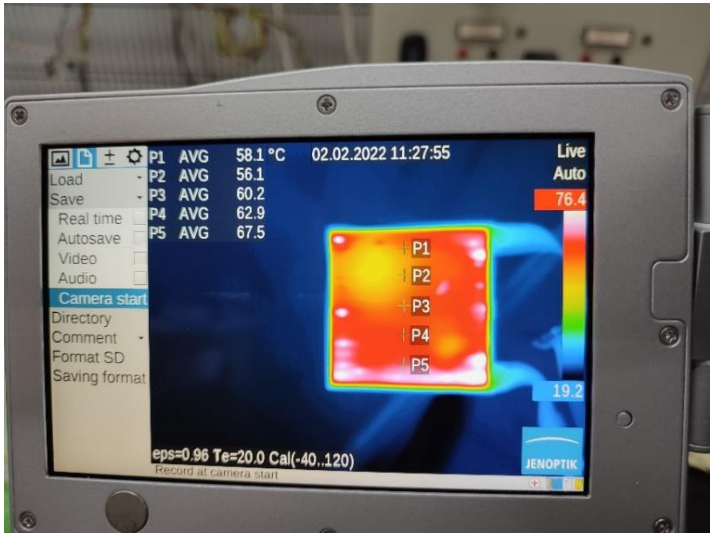
$T_{average}$ **5 points hot side: 40.1°C**

- 3 W/cm^2; theoretical: 48 W
- **34.3 V; 1.41 A = 48.36 W** real
- **Liquid pressure**:
  Inlet 3.44 bar; Outlet -0.02 bar

$T_{average}$ **3 points cold side: 17.7°C**

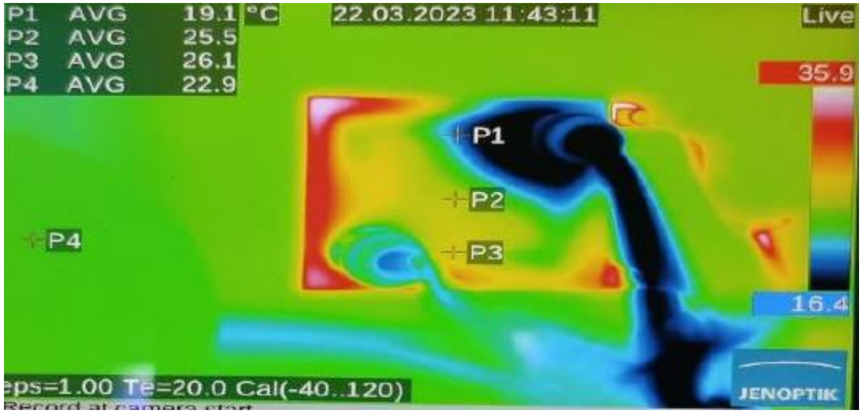
CoolFPGA – Tests

Coolant at 5°C, mass flow rate = 0.33 kg min.



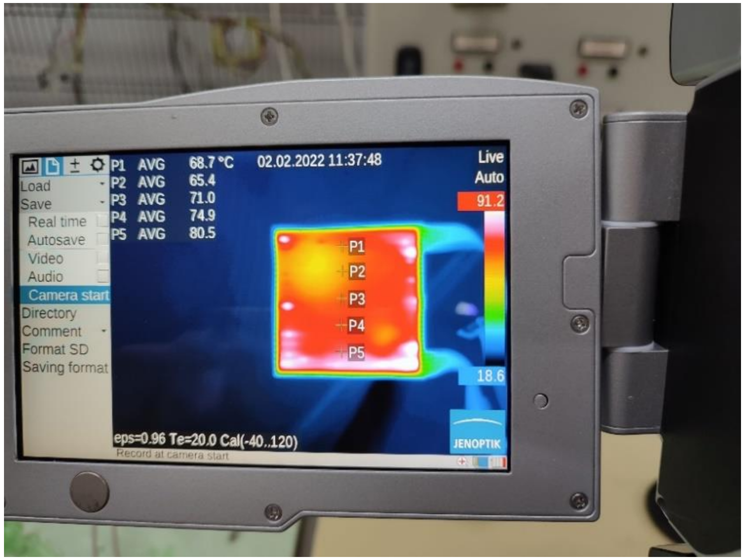
- 5 W/cm^2; theoretical: 80 W
- **46.0 V; 1.474 A = 80.04 W** real
- **Liquid pressure**:
  Inlet 3.35 bar; Outlet -0.03 bar

$T_{average}$ 3 points cold side: 23.6°C



$T_{average}$ 5 points hot side: 61.0°C

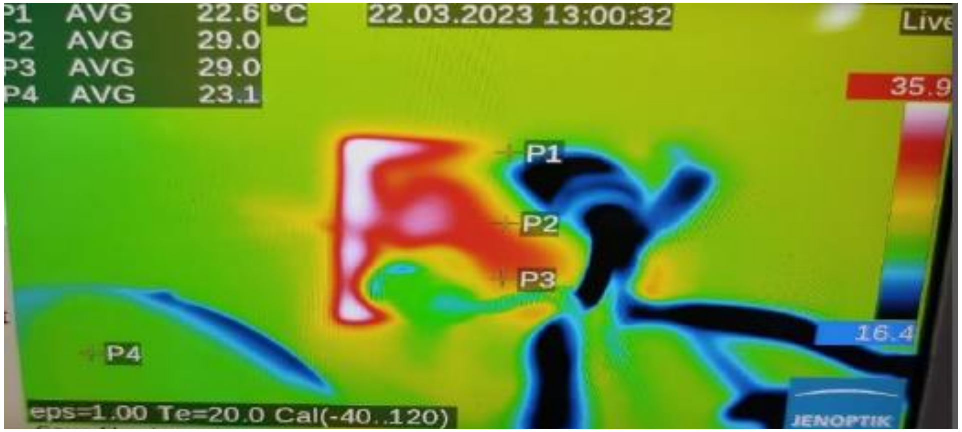
Coolant at 5°C, mass flow rate = 0.33 kg min.



- 6 W/cm^2; theoretical: 96 W
- **51.9 V; 1.87 A = 97.1 W** real
- **Liquid pressure**:
  Inlet 3.42 bar; Outlet -0.02 bar

$T_{average}$ 3 points cold side: 26.9°C

$T_{average}$ 5 points hot side: 72.1°C



MODEL AND PROPERTIES

- CAD geometry provided by Pisa group
- Fluid volume added to the model

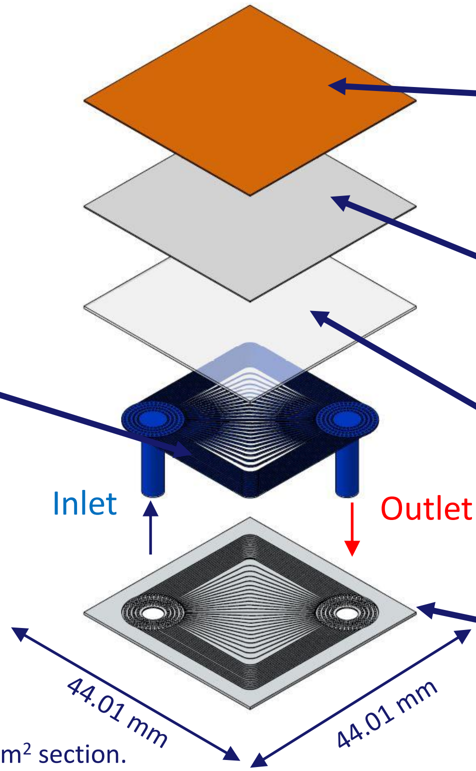
FLUID DOMAIN (Novec 7100):

Novec 7100
- ρ = 1510 kg/m^3
- μ = 0.00058 kg/(m·s)
- C_p = 1183 J/(kg K)
- k = 0.069 W/mK
- Laminar flow

Inlet:
- Velocity Inlet
- V_{in}= 0.29 m/s*
- T_{in}= 5°C

Outlet:
- Pressure Outlet

*Considering constant mass flow of 0.33 kg/min on a 12.5 mm^2 section.



SOLID DOMAINS:

Resistor
- S = 0.25 mm
- k = 0.2 W/mK
- Volumetric Heat Source: 98 W

Glue Masterbond EP30TC
- S = 0.05 mm
- k = 2.7 W/mK

Pyrex
- S = 0.50 mm
- k = 1.14 W/mK

Silicon
- S = 0.50 mm
- k = 148 W/mK

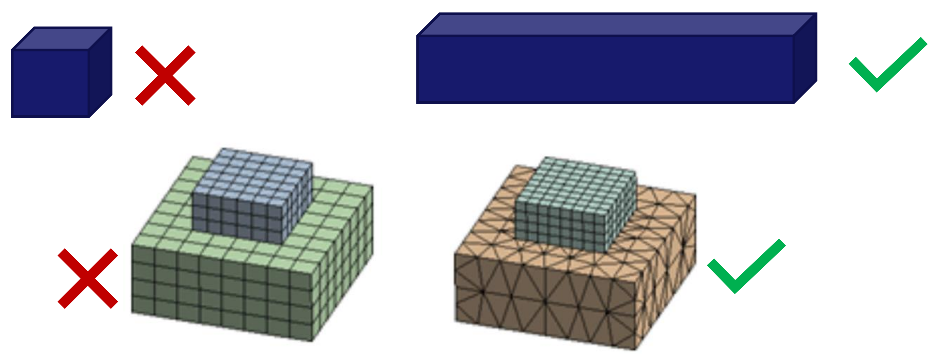
CoolFPGA – Simulations

GRID CREATION

- Probably the most challenging part of this work, why?
- Total volume fo the model is 2.23 cm^3
- In order for the fluid dynamics to be well reconstructed, each channel must be divided into a fairly large number of cells.
    - The width of the channel is the smallest dimension, equal to 0.1 mm.
    - Supposing a division it into 10 parts, cubic cells with each edge equal to 0.01 mm will result.
- Thus, if the whole volume would be divided with cells with 0.01 mm edge, this will result in $\approx 2 \cdot 10^9$ cells, not sustainable by calculators.

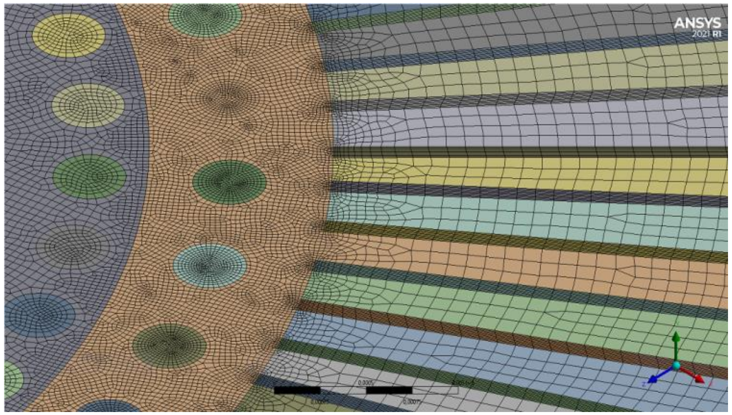
Some tricks are used:

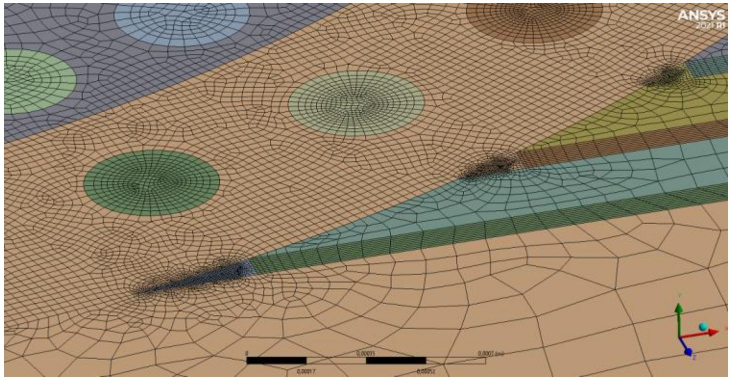
- Elongated parallelepiped instead of cubes (main dimension aligned with channel direction)
- Bigger element size in the silicon volume (possible with non-conformal meshing method)



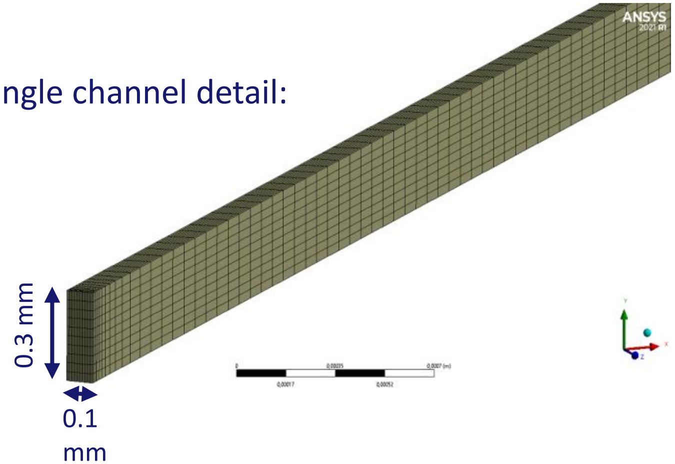
GRID CREATION

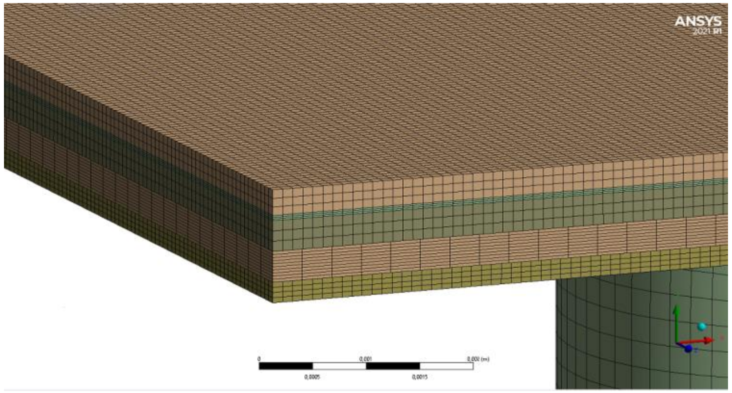
- At the end 7’060’226 cells are created in the grid.
- The grid works, some adjustments to improve convergence still needed.





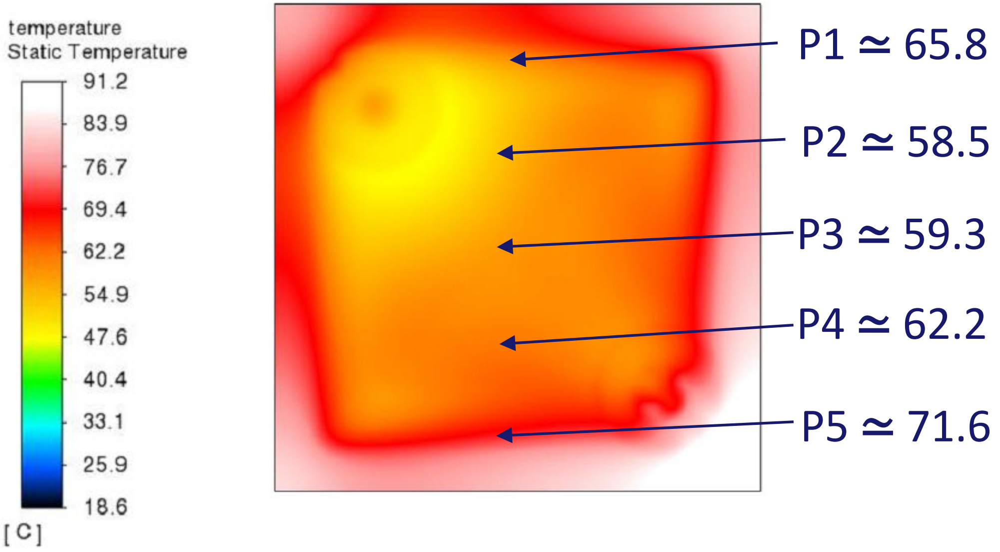
Single channel detail:

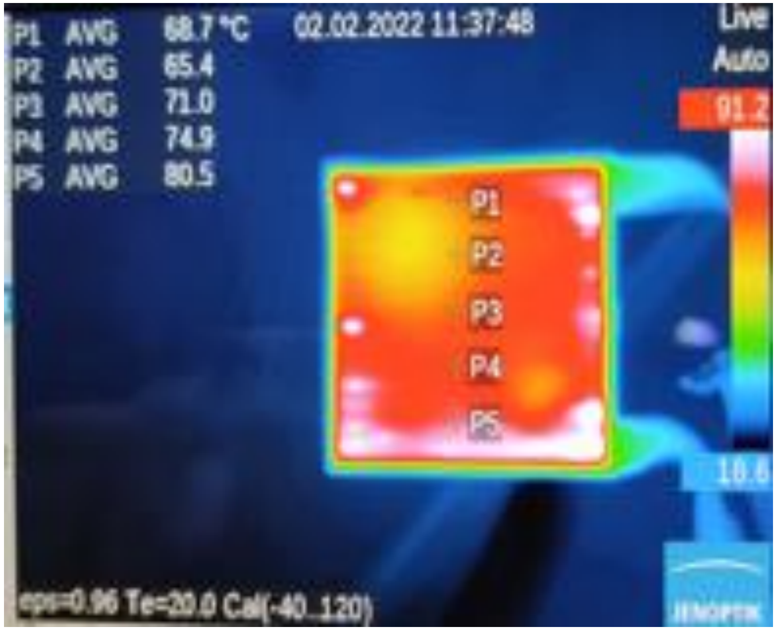




RESULTS - TEMPERATURE

Resistor side

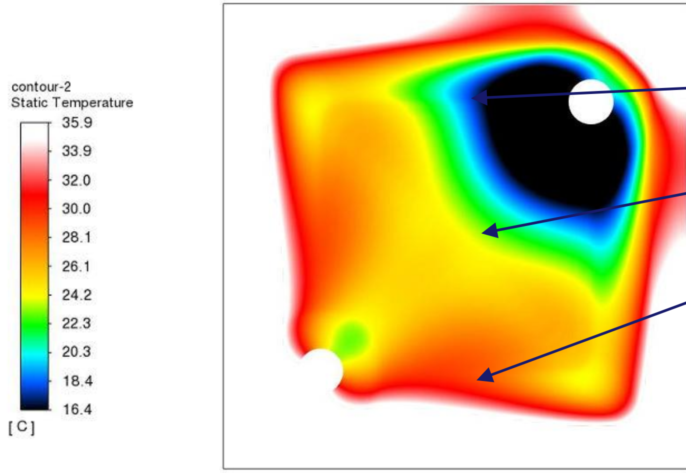




Reasonably good agreement

CoolFPGA – Simulations

RESULTS - TEMPERATURE

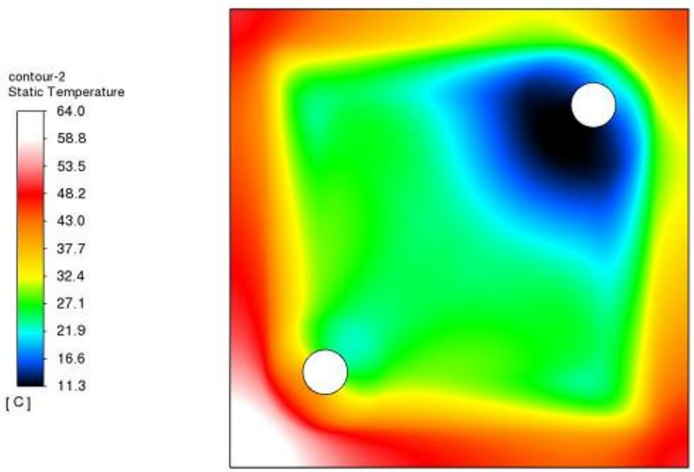


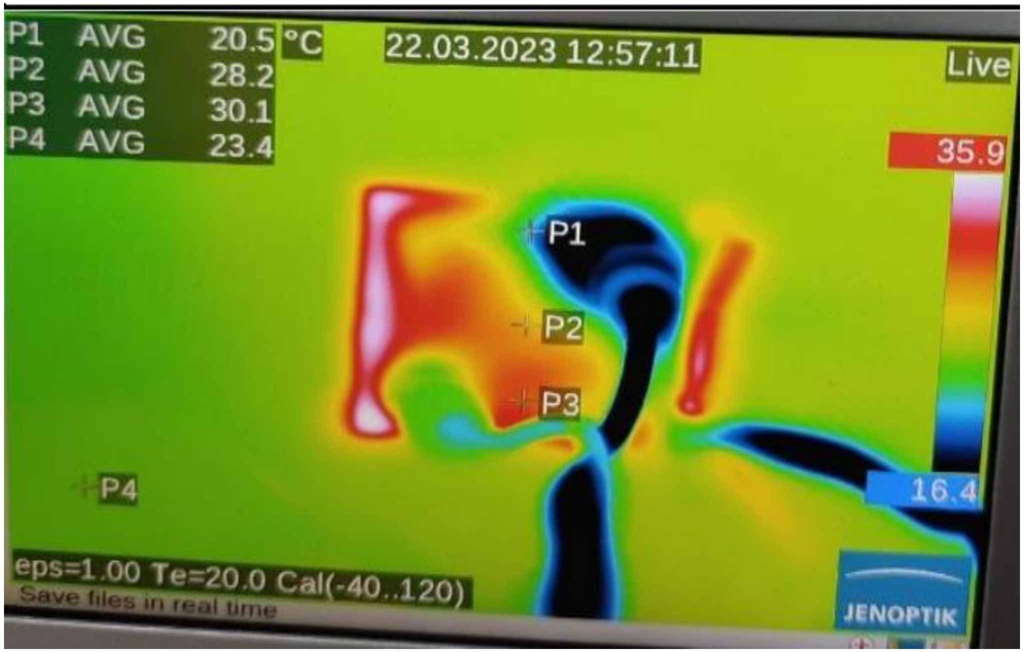
P1 ≃ 19.8

P2 ≃ 24.5

P3 ≃ 29.8

Silicon side





Simulations seem overstimating the higher lateral temperatures: further investigations needed

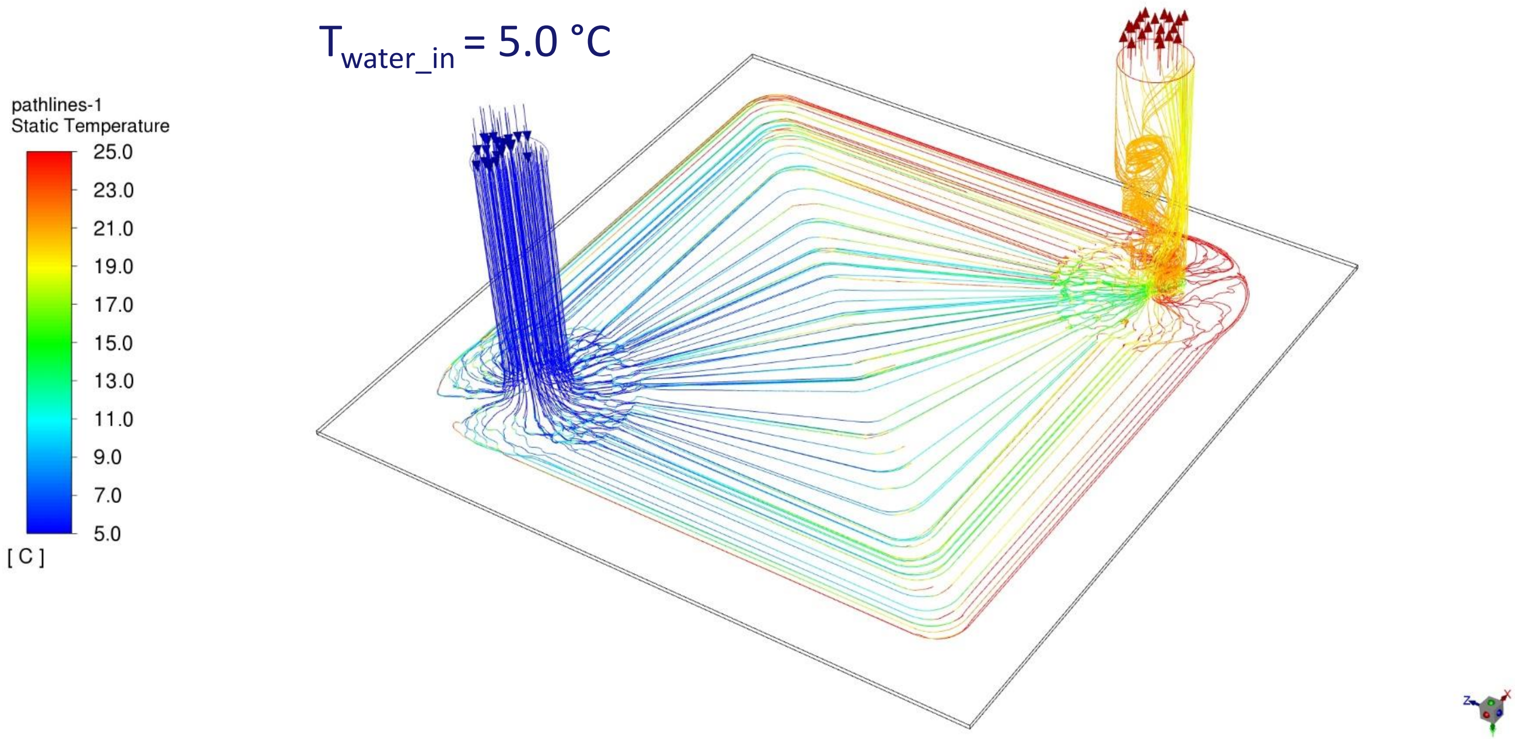
CoolFPGA – Simulations

RESULTS - PATHLINES

T_{water_out} = 20.4 °C

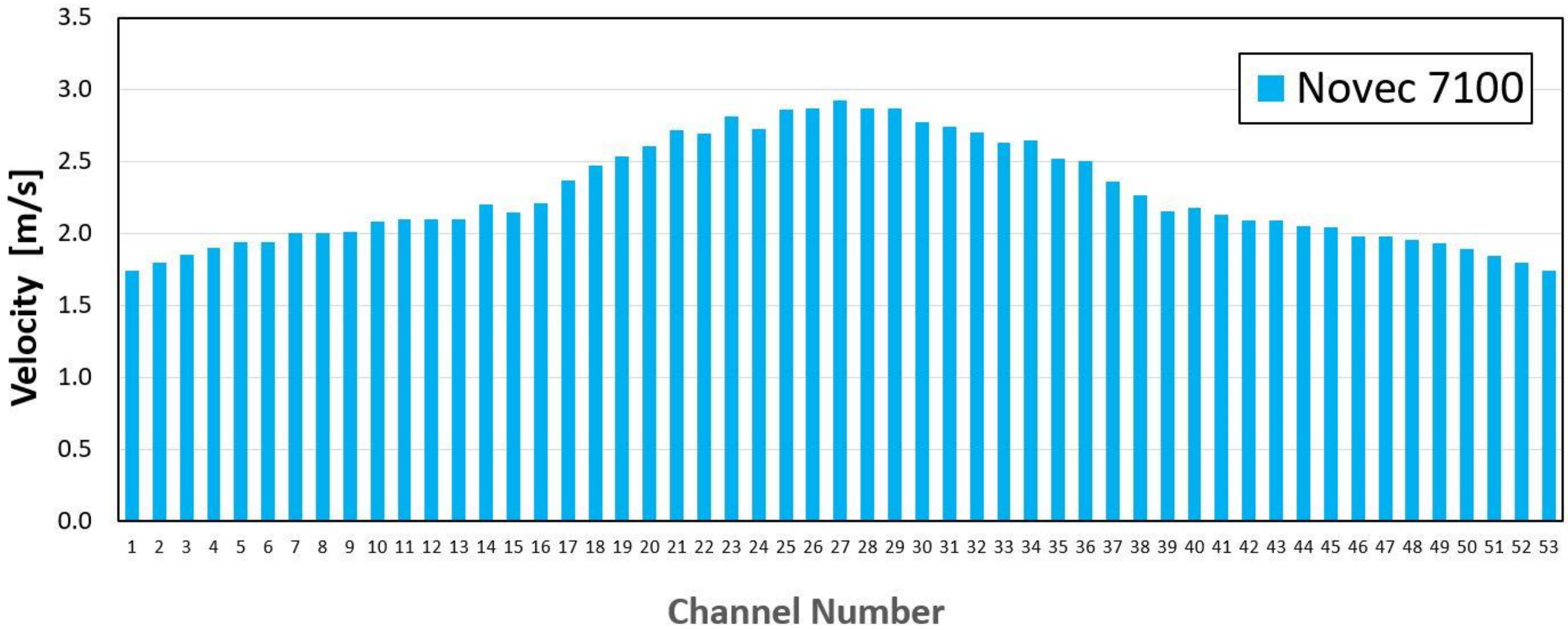
Ansys 2023 R1

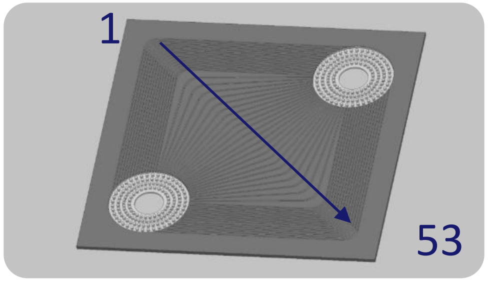
T_{water_in} = 5.0 °C



Tests: T_{water_in} = 5.0°C, T_{water_out} = 20.0°C: good agreement with tests

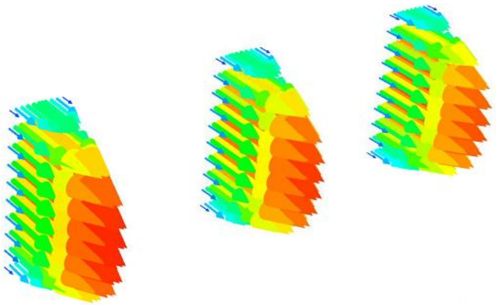
RESULTS – VELOCITY PROFILES

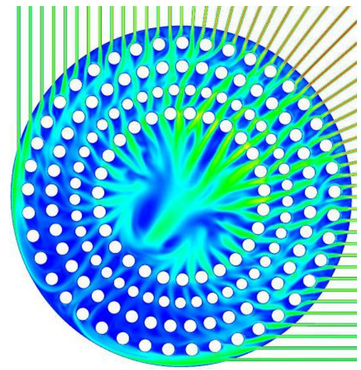


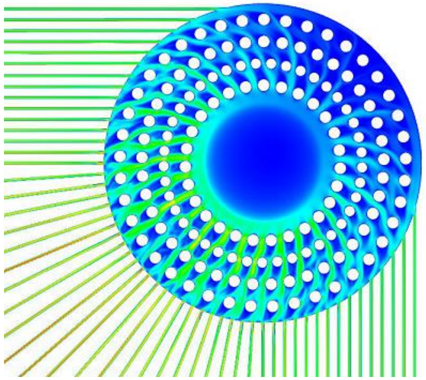


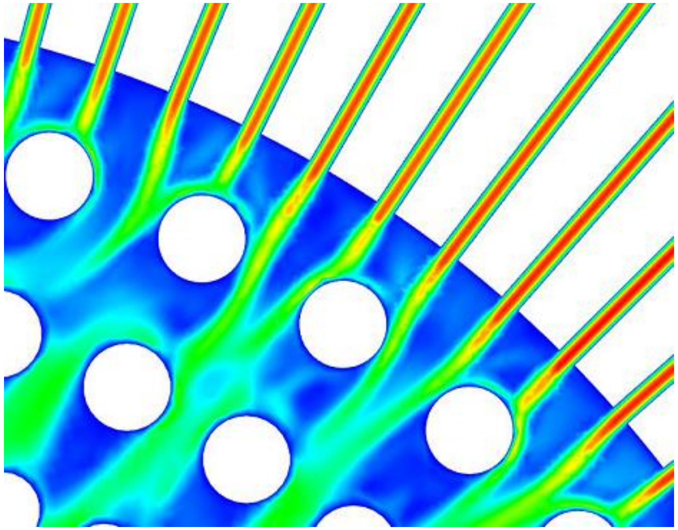
CoolFPGA – Simulations

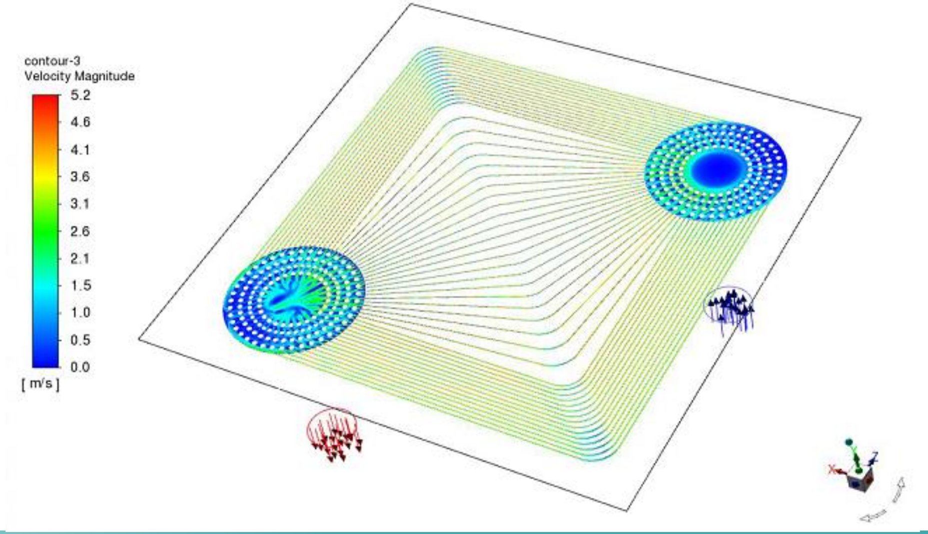
RESULTS – VELOCITY PROFILES





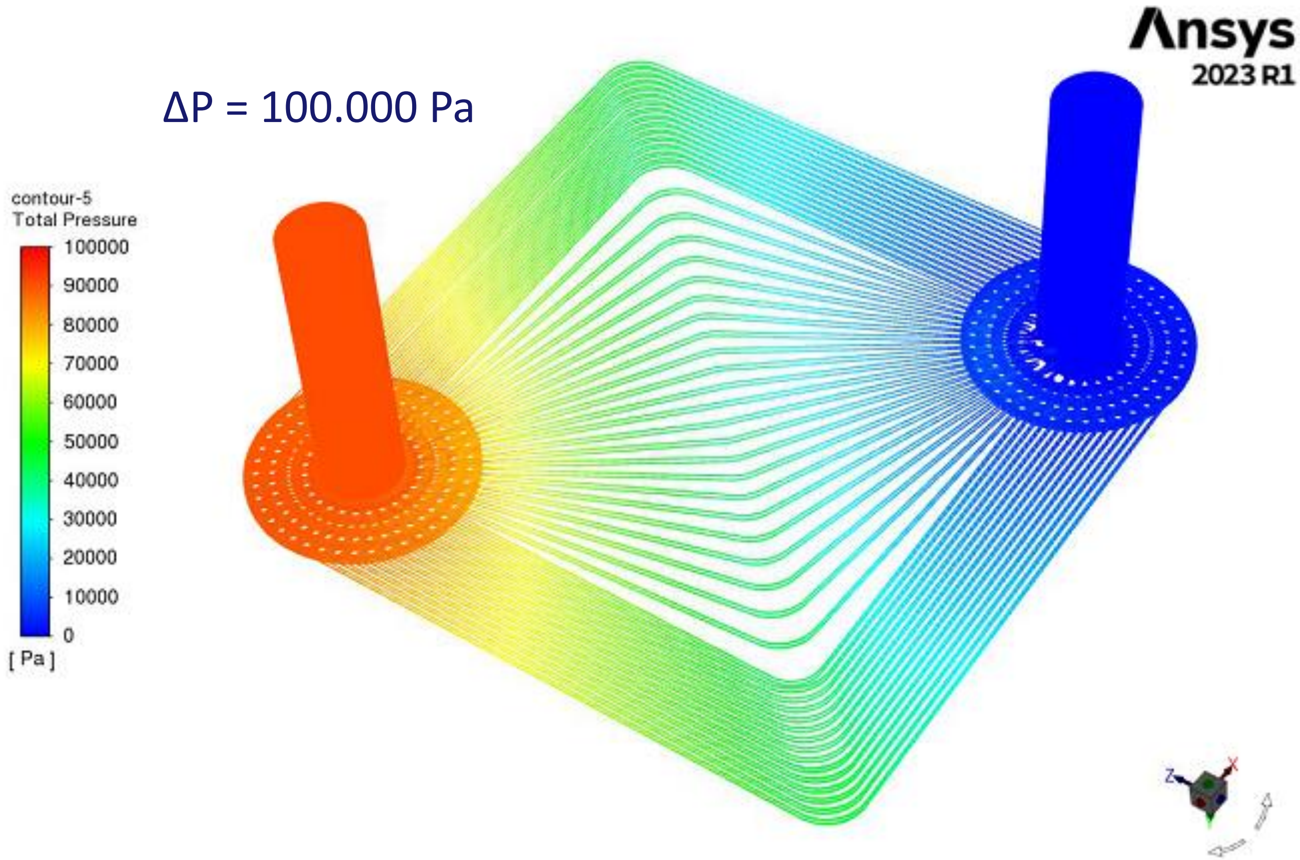






RESULTS – PRESSURE DROP

ΔP = 100.000 Pa



Tests: ΔP = 344.000 Pa: simulations seem underestimating the pressure drop: further investigations needed

CONCLUSIONS

- Tests on the performance of microchannels on the surface of the die;
- fragility of the bond between the two layers of silicon;
- good performance of the systems tested up to 6 W/cm^2.

- Preliminary CFD simulations repeated in the same conditions:
  - ❑ good agreement in terms of temperatures with the experiments (with some discrepancies);
  - ❑ Underestimation of pressure drops respect to the tests (to be investigated).

- Future investigations on different geometries for microchannels path (easier) and their shape (harder), trying to go to higher heat fluxes.