Centro Nacional de Microelectrónica CSIC

CONSEJO SUPERIOR DE INVESTIGACIONES CIENTÍFICAS

Status of Micro-Channel Cooling Developments at IMB-CNM

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…and the invaluable contribution of the personnel of IMB-CNM's Micro-Fabrication Facility.

Scope

- Introduction and previous work
- Objectives
- Technology and test methods
- Current status and results
- Future work

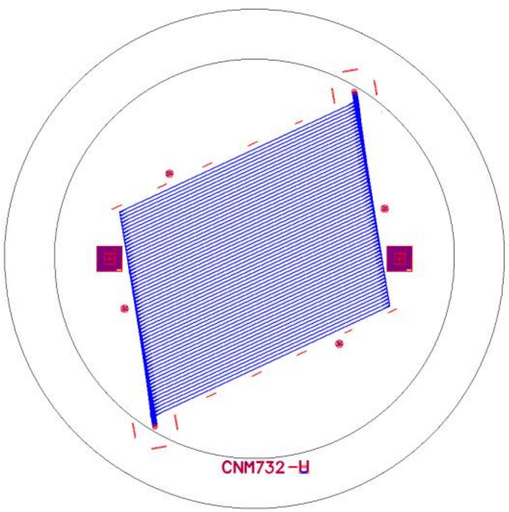
Framework

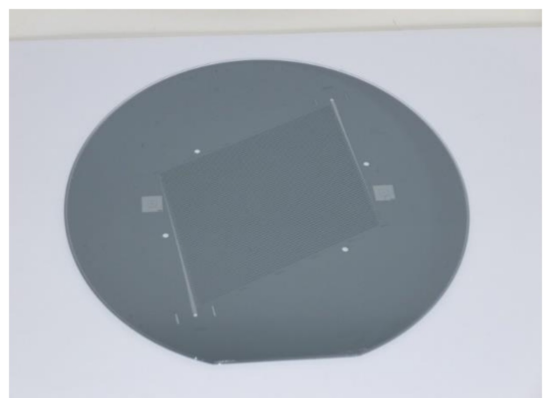
- In current HEP experiment there is a need to keep the silicon detectors at low temperature
  - ➢ Leakage current increase with temperature and irradiation
    - ⇒ Power needs → partial depletion → inefficiency
    - ⇒ Thermal runaway
  - ➢ -10 ºC to -40 ºC
- Different solutions
  - ➢ Air cooling
  - ➢ Liquid cooling
  - ➢ Bi-phase cooling
- Complex setups at module level
  - ➢ Technology limits for pipe reduction and coverage
  - ➢ Thermal connection with sensors and electronics
  - ➢ Complex assembly process

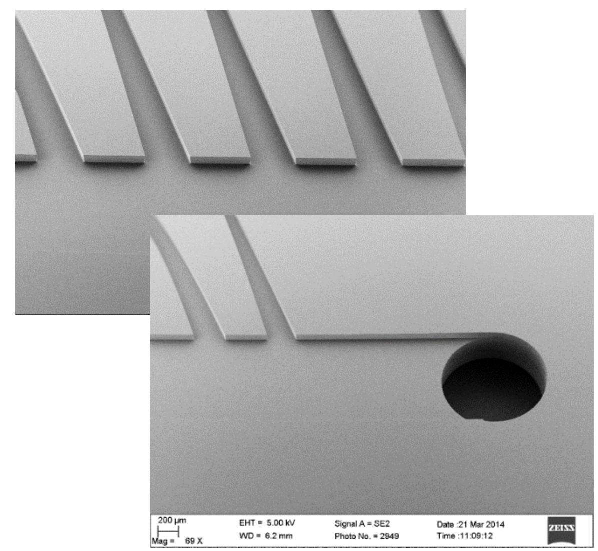
Micro-channel cooling

- In Electronics:
  - ➢ Scaling
  - ➢ High power (heat) densities
  - ➢ Heat transfer efficiency
- In HEP
  - ➢ Reduce material (radiation length)
  - ➢ Many thermal cicles + position resolution → small (no) CTE mismatch
  - ➢ Large areas to refrigerate (low heat density)
  - ➢ Thermal Uniformity → Non-uniform heat removal – “capilars”
  - ➢ Assembly
- At CNM
  - ➢ Micro-channels basic technology development and prototyping
  - ➢ Using the technological capabilities (DRIE, wafer bonding, processing)
  - ➢ In collaboration with IFIC and DESY (Hamburg) for tests

- In the past, we developed the technology of micro-channel cooling for High Energy Physics detectors in collaboration with DESY (Hamburg)
  - N. Flaschel, et al. ”Thermal and hydrodynamic studies for micro-channel cooling for large area silicon sensors in high energy physics experiments”, NIMA, vol. 863, pp. 26-34, 2017. http://dx.doi.org/10.1016/j.nima.2017.05.003
  - Ph.D Thesis: Micro-channel Cooling For Silicon Detectors. Nils Flaschel. Hamburg University. 2017

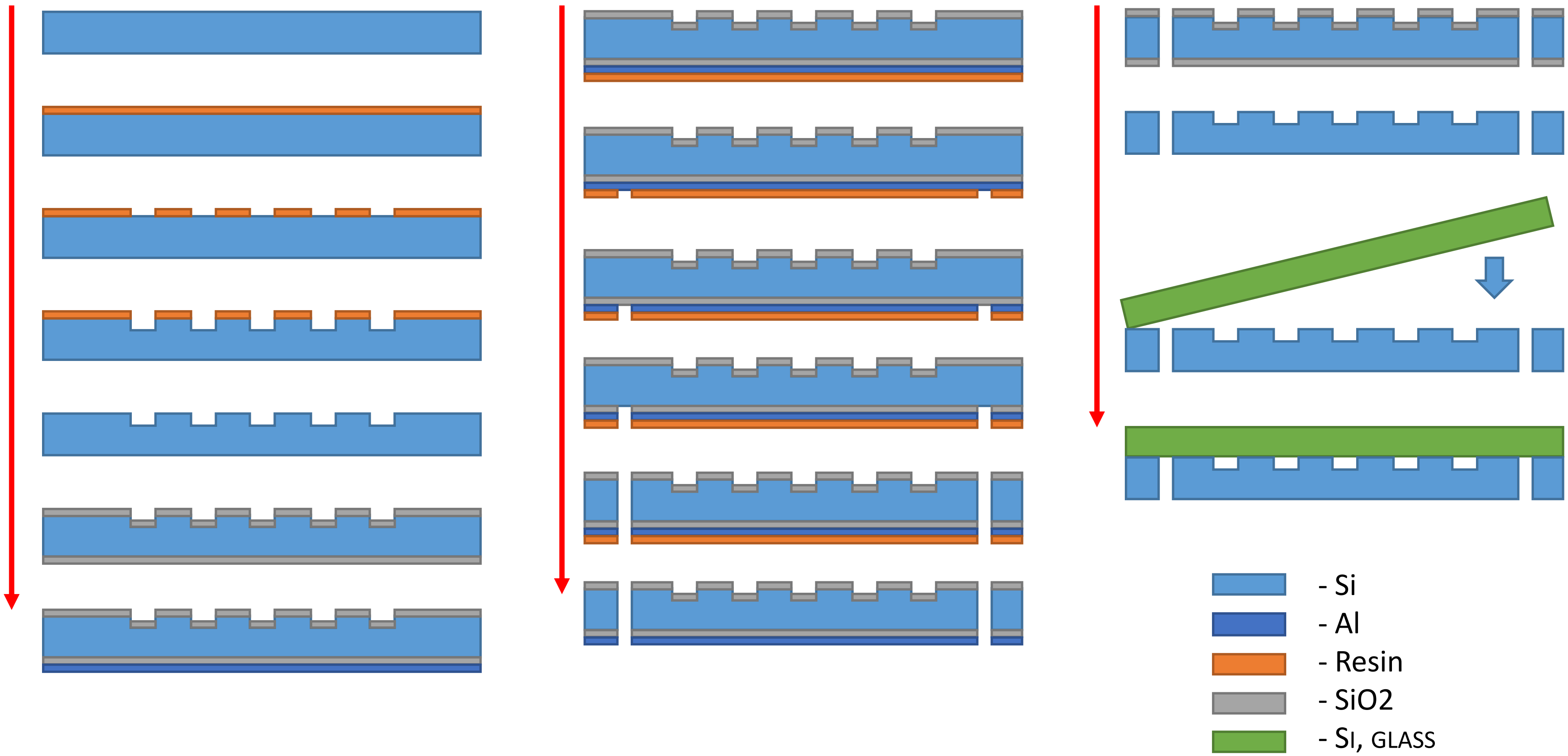






Technological process

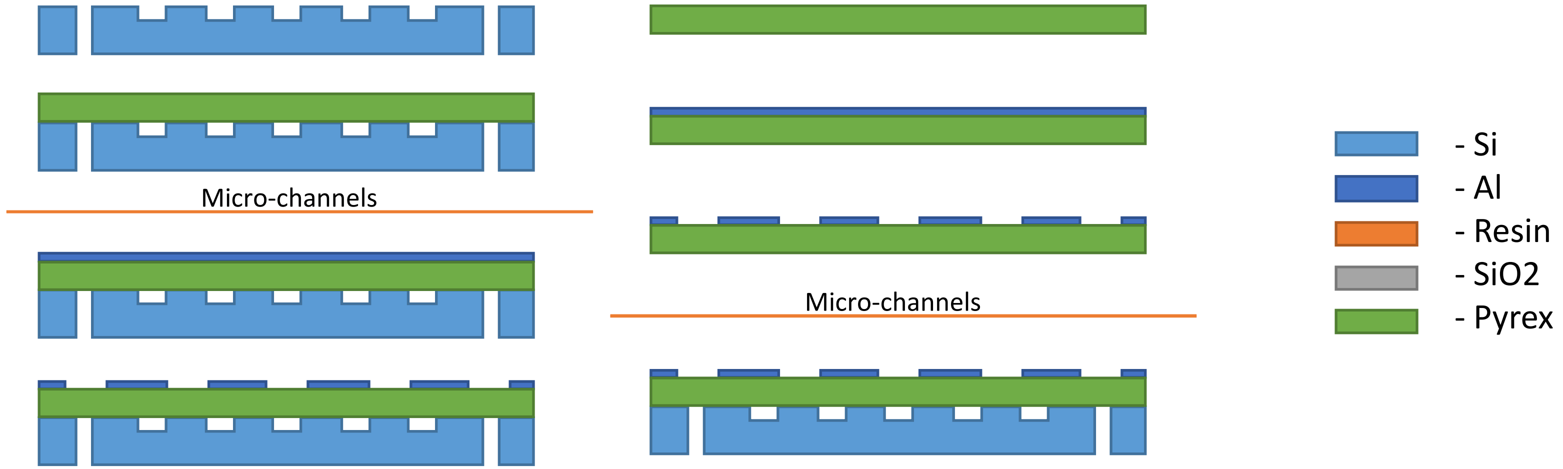
- Technological steps for buried micro-channels at CNM



Objectives

1. Integration of micro-channels in silicon interposers with integrated signal and power routing (RDL)

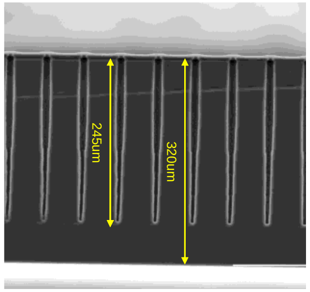
“Pre-Processing” & “Post-Processing” technology



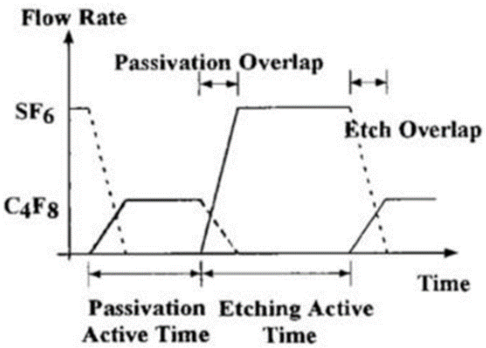
2. Full integration of the sensor (CMOS technology) with the cooling in a single piece

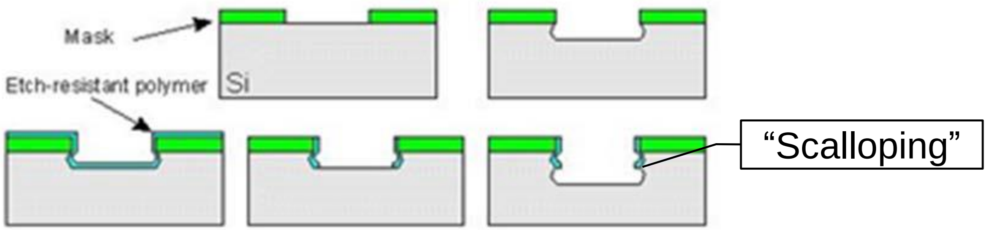
Methods –micro-channels

Creation of micro-channels



- Deep Reactive-Ion Etching (DRIE) (Alcatel 601 E)
  - Chemical-Physical etch of silicon
  - Very anisotropic → high aspect ratio (deep and vertical holes)
  - Bosch process: alternating between etching (SF_6) and passivation (C_4F_8)



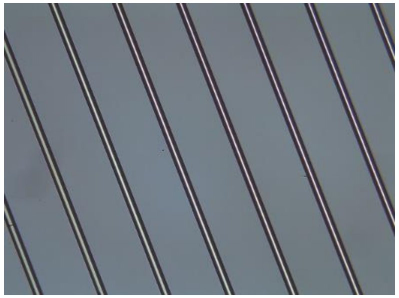
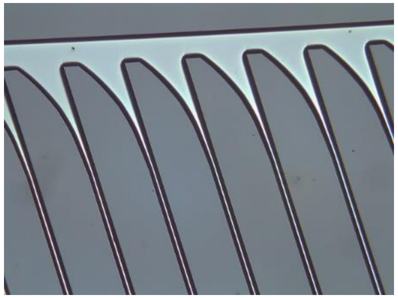
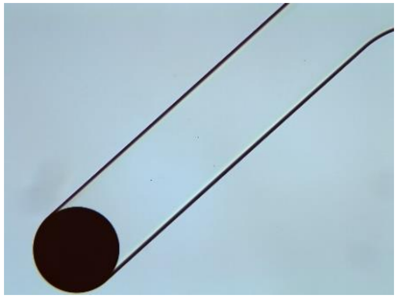


- 2 Si-etching processes
  - 1st to create the channels (100 um deep)
  - 2nd to form the inlet and outlet:
    - ✓ Through hole
    - ✓ "double-side" alignment

Methods –micro-channels

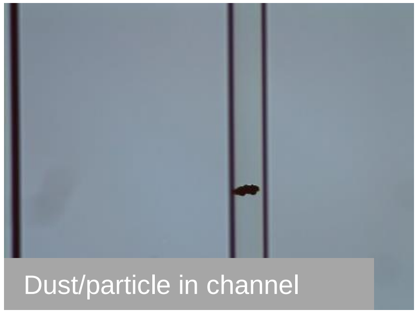
Micro-channels evaluation

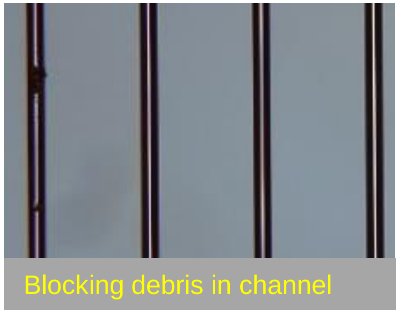
- Microscope – defect/yield analysis

- Yield analysis made on 10 wafers (49 channels, 2 manifolds)
  - Non-critical minor defects and dust seen in several channels
  - Blocking debris seen in 3 channels (can be cleaned)
  - “Columnar” channel etch defect seen in 7 channels (Not blocking)


In channel minor defect


Dust/particle in channel

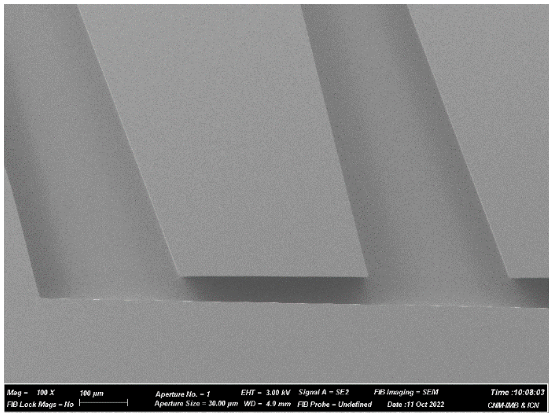

Blocking debris in channel

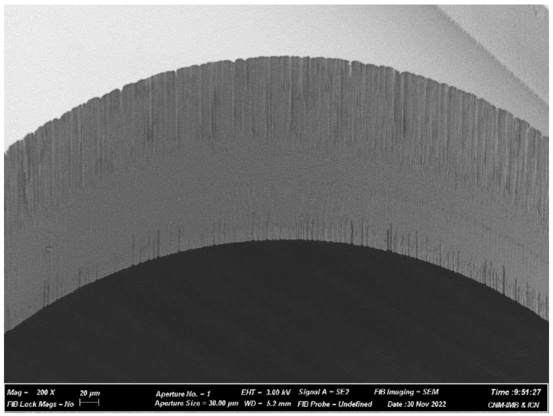

Bad channel etching

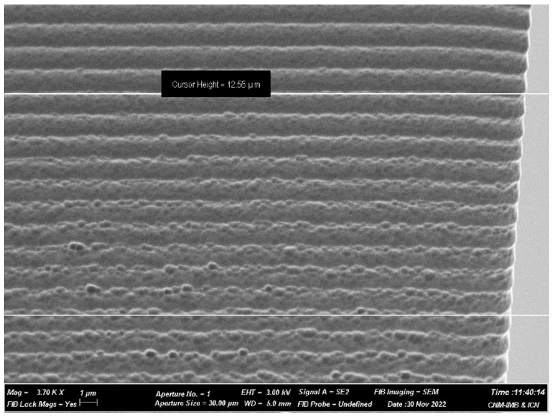
Methods –micro-channels

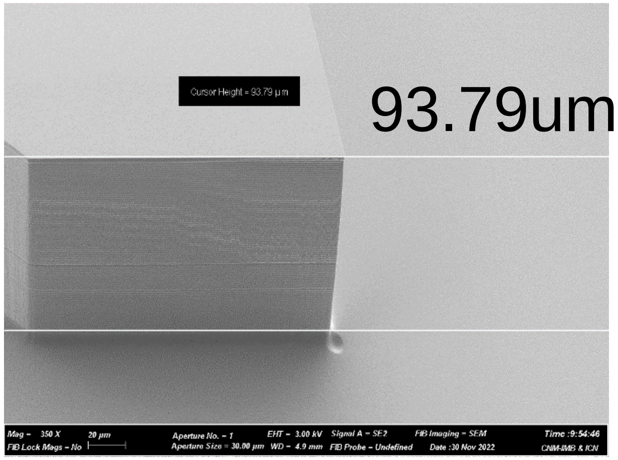
Micro-channels evaluation

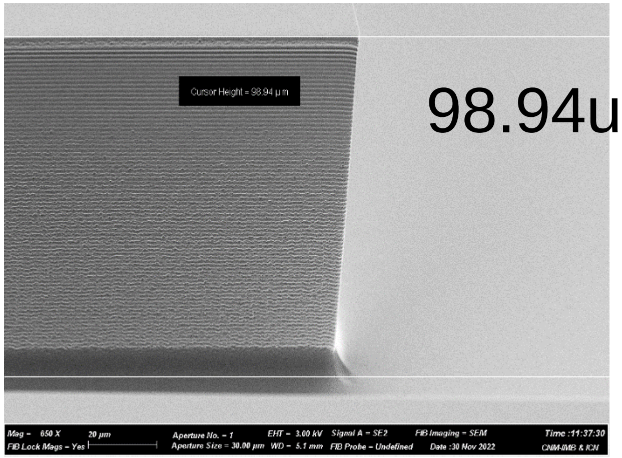
- SEM (Scanning Electron Microscopy) (Zeiss Auriga 40)

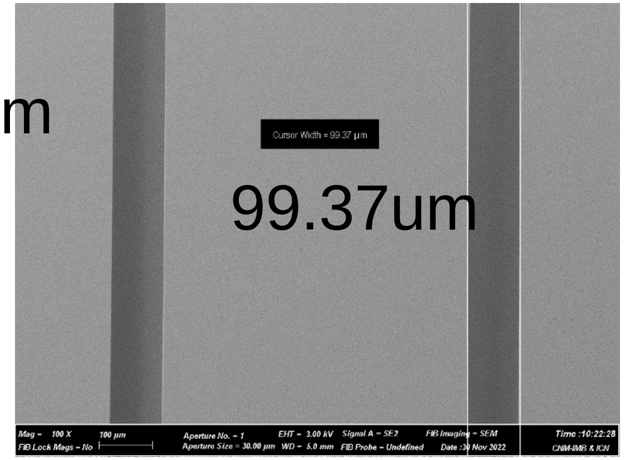










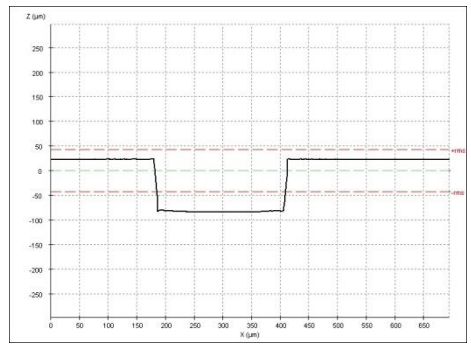


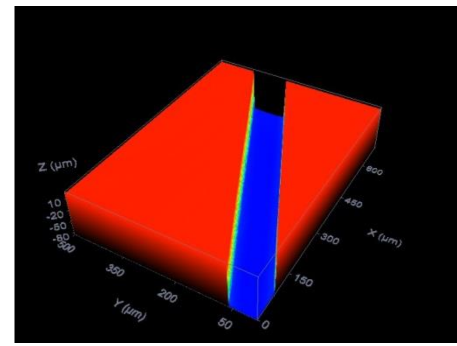
Methods –micro-channels

Micro-channels evaluation

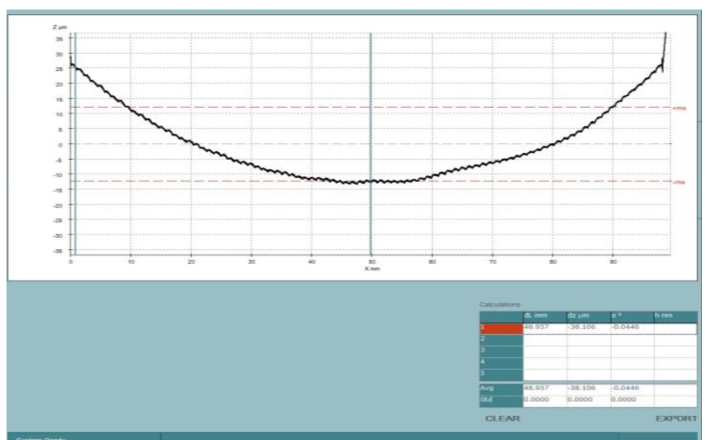
- Profilometer – Confocal microscopy
  - ➢ Vertical profile measurements

Run7188 - etp9 - Medidas confocal							
Oblea	Profundidad trincheras (um)						
	p1	p2	p3	p4	p5	Media	sd
1	107,0	108,5	107,5	106,5	109,0	107,7	1,0
2	107,0						





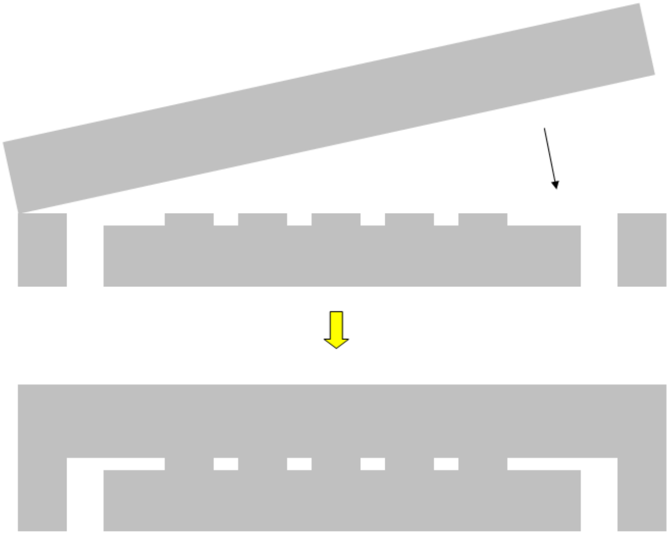
  - ➢ Wafer bowing



Methods – Wafer Bonding

Wafer bonding (Süss Microtech Sb6e)

- Anodic: Borosilicate Glass – Si
  - High V (1000 V), Low T (~**350 ºC**),
  - PYREX®, MEMpax®
  - ☞ Micro-machining in the glass wafer?
- Eutectic: Metal-Si
  - Low T (~400 ºC), Au
  - ☞ Al?
- Fussion: Si-Si
  - High pressure (2-5 Bar), Low T (~450 ºC),
  - ☞ Surface preparation is critical

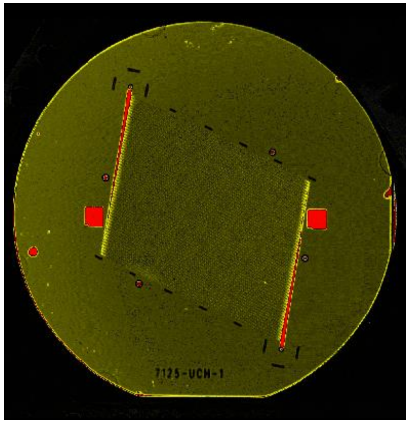


Methods – Wafer Bonding

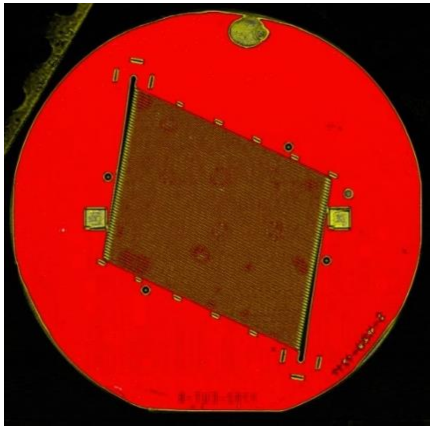
Wafer bonding evaluation

- SAM (Scanning Acoustic Microscopy) (Sonoscan-Gen5)

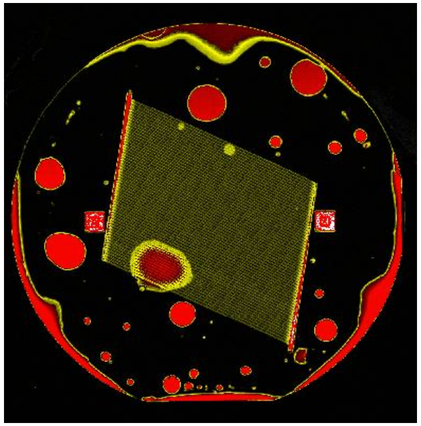
Anodic bonding:



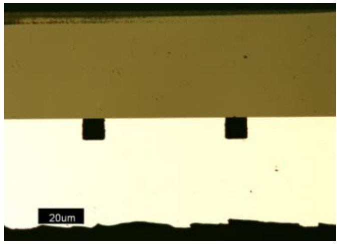
Eutectic bonding:

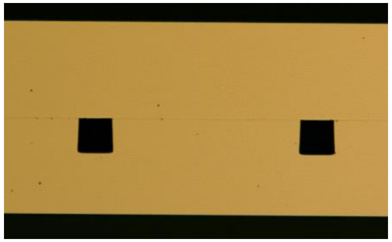


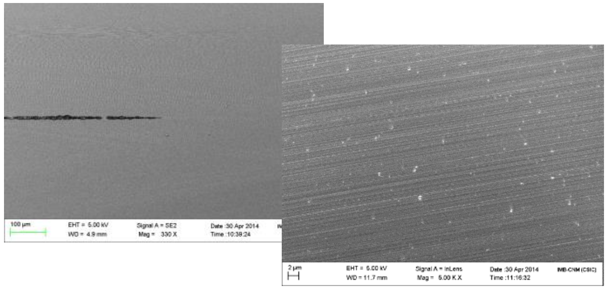
Fusion bonding:



- Cross sections (Reverse engineering)

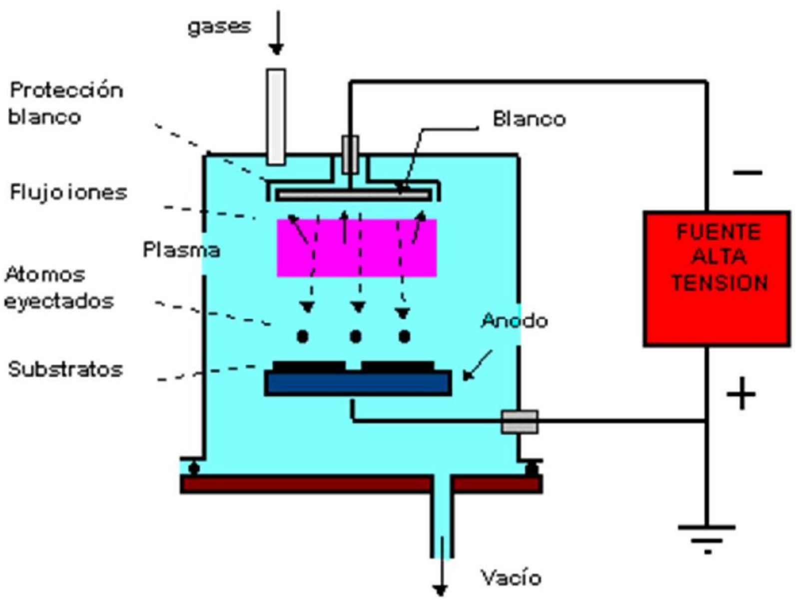






Metal deposition

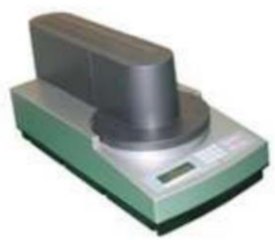
- Sputtering process (Kenosistec KS800H)
  - ➢ Sputtering system to deposit metallic layers
  - ➢ Target used: Al (99.5%) / Cu (0.5%)
  - ➢ Other targets available: Au, W, Ti, …
  - ➢ Better adherence than evaporation



Methods – Metal w/ μ-channels

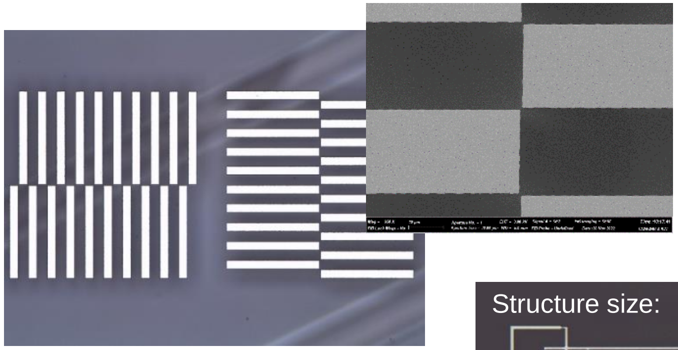
Metal evaluation (in assembly with micro-channels)

- Four point probe Resistivity Measurement (Chang Min Four)
  - Metal sheet resistance

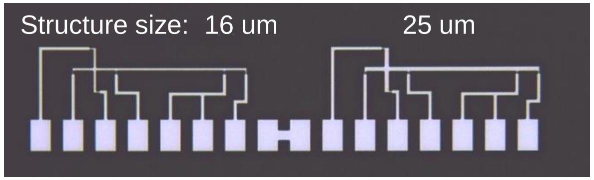


Al 1 um	Rs (Ω/□)	Rs St. deviation (Ω/□)
A-11	33.1E-3	1.3E-3
A-13	42.3E-3	4.4E-3
A-14	42.3E-3	4.9E-3

- Test structures (optical, CBR)

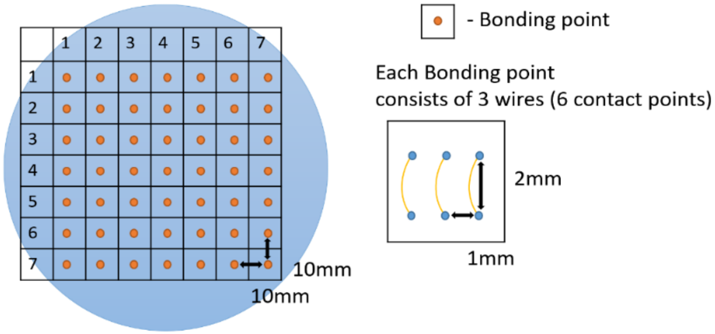


A-20, Al 0.5um	Small (avg.)	Wide (avg.)
Rs (Ω/□)	62.74E-3	63.18E-3
Rs St. deviation (Ω/□)	3.44E-3	3.48E-3
Weff (um)	15.02E+0	24.32E+0
Weff St. deviation (um)	236.31E-3	321.04E-3

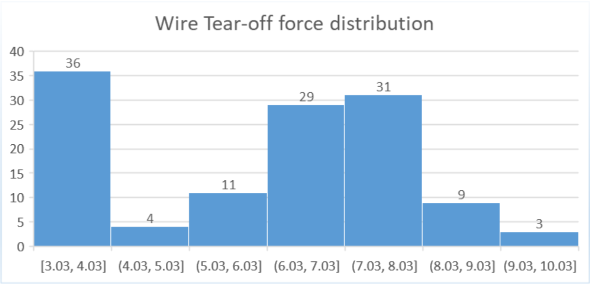


Methods – Metal w/ μ-channels

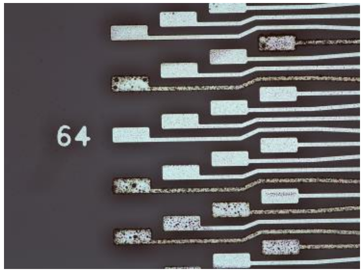
Metal evaluation (in assembly)



- Wire-bonding – pull tests
  - 7x7 array, 3 wires in each point. 25 um Al wire.
  - Test performed on **Pre-processing** blanket sample
    - Bonding on full wafer
    - No parameter optimization

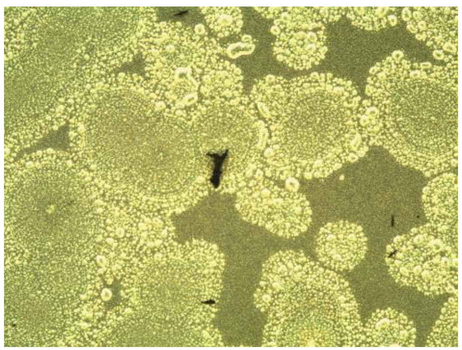


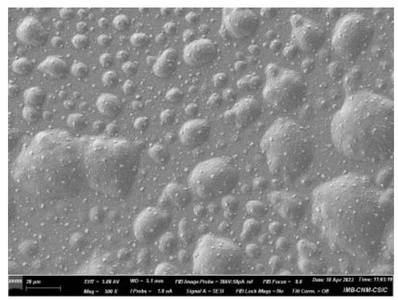
  - Test performed on **Post-processing** blanket sample
    - ☞ Problematic wire-bonding & pull tests
    - ☞ Bad adherence of Al layer on Silicon.

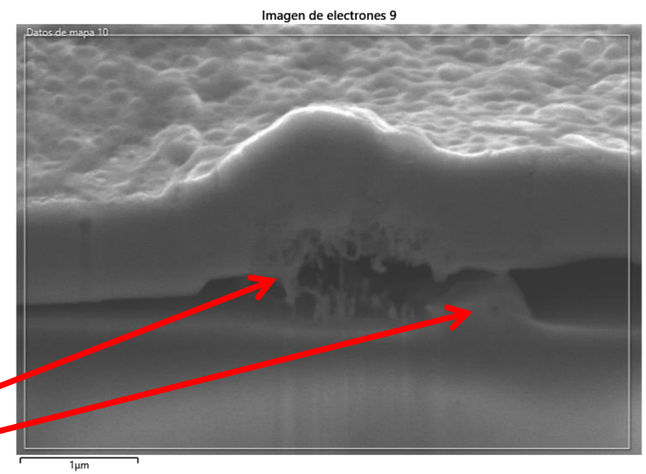


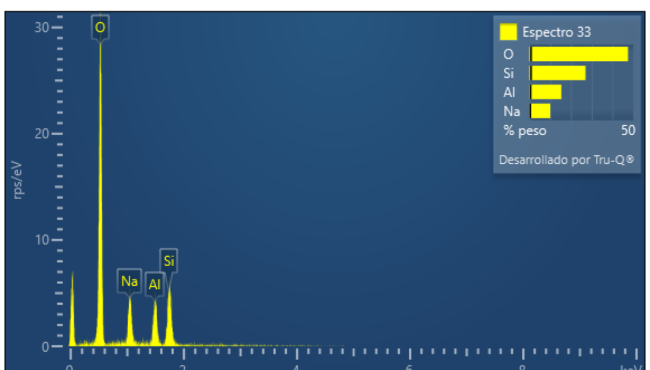
Metal evaluation (in assembly)

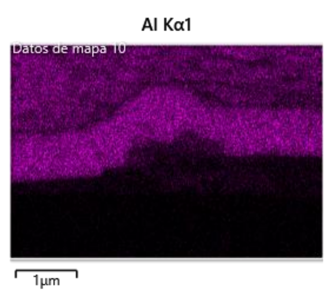
- EDX (Energy dispersive X-ray spectroscopy – SEM – FIB)
  - ➢ Degraded aluminum after w. bonding (post-processing)
  - ➢ Sodium precipitation, Al stress



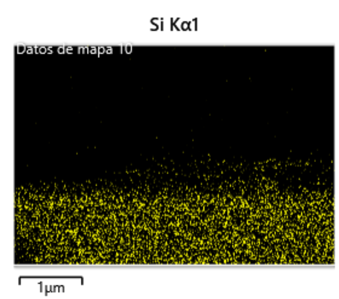




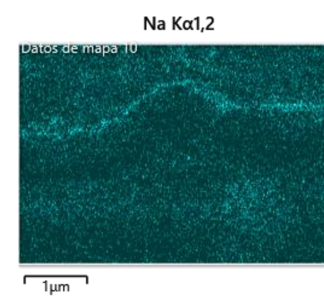




Al



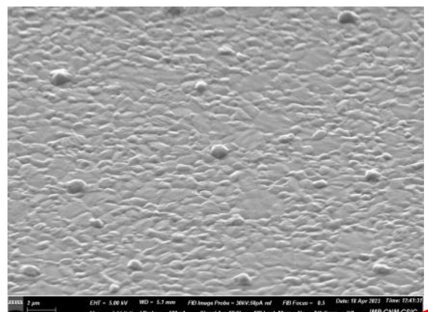
Si

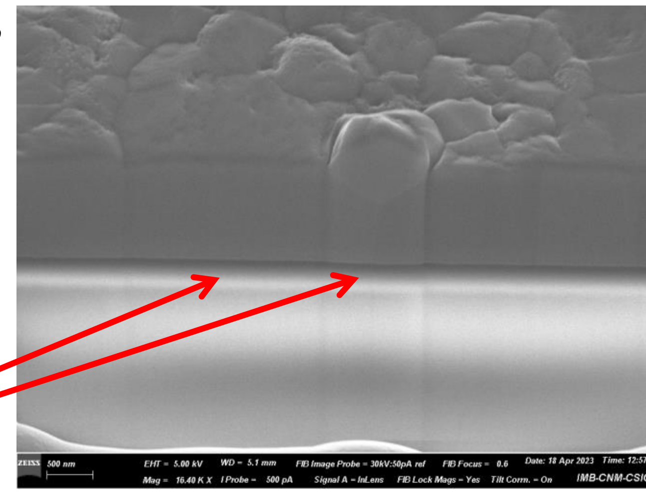


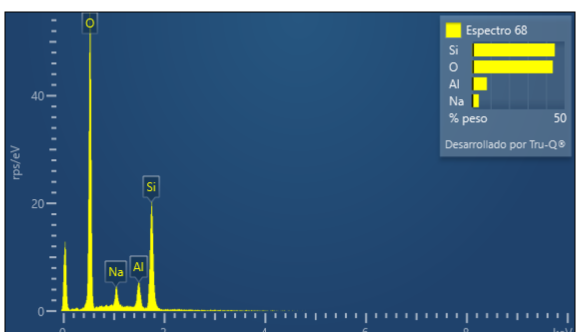
Na

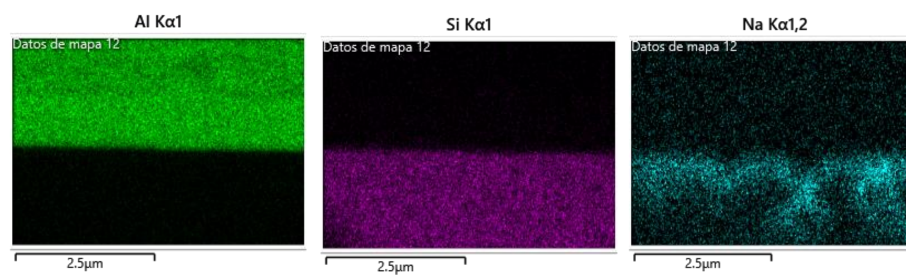
Metal evaluation (in assembly)

- EDX (Energy dispersive X-ray spectroscopy – SEM – FIB)
  - Heated substrate sputtering, MEMpax wafer
  - Less Al stress, No Sodium precipitation,





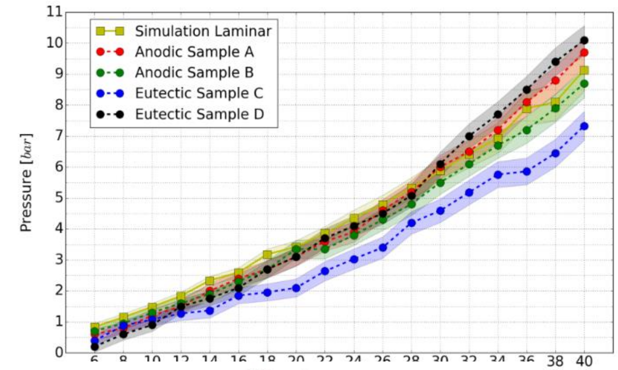




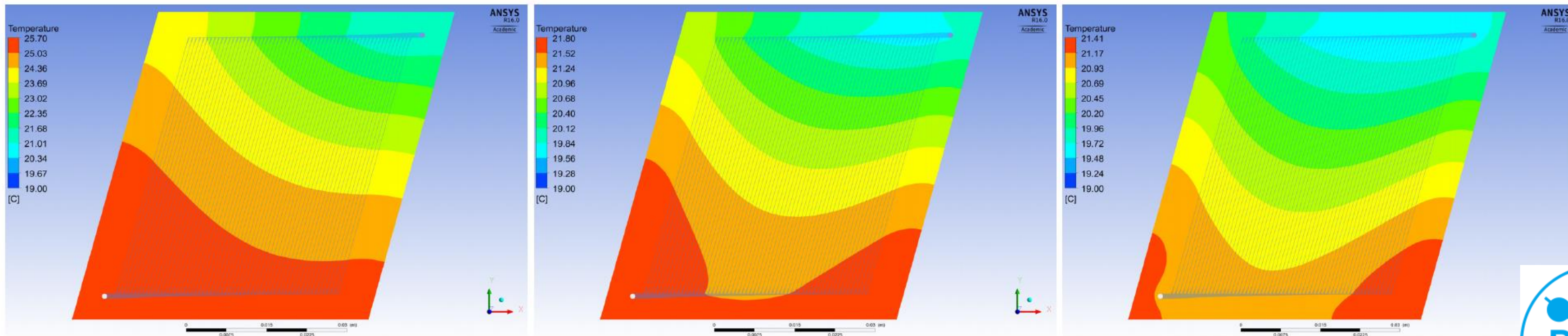
Al Si Na

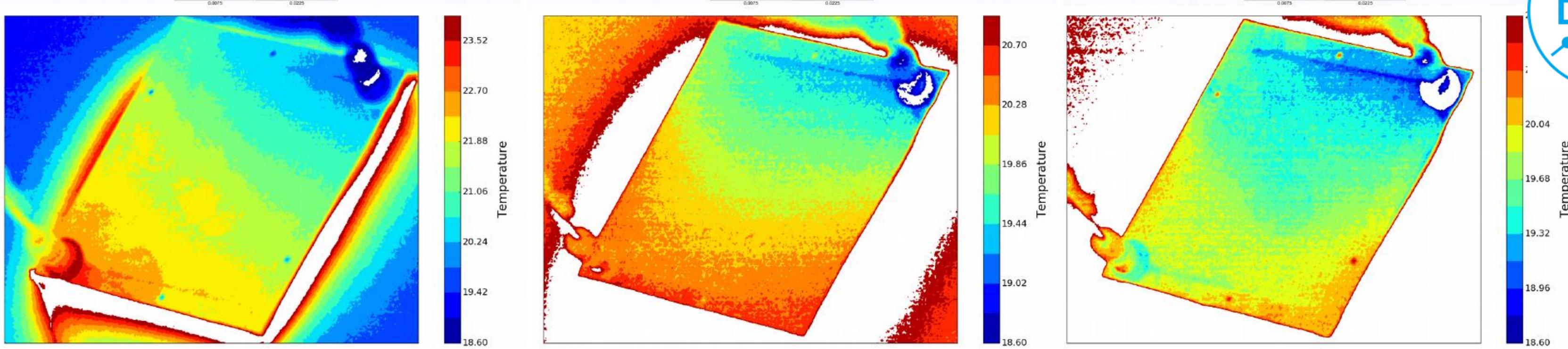
Methods – Fluidic & Thermal

- Previous results on fluidic and thermal tests
  - Laminar flow
  - Thermal homogeneity across the sample, < ±1 ºC (for lowest flow rate)



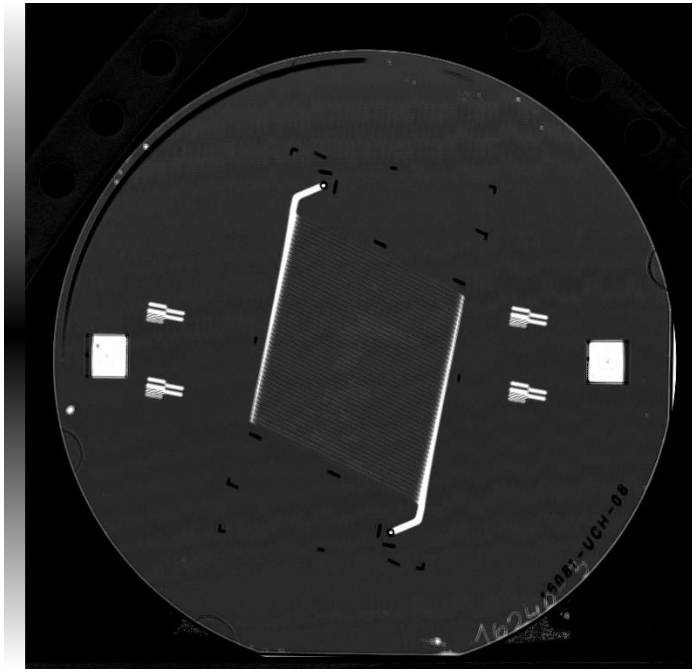
10 ml/min | 30 ml/min | 50 ml/min



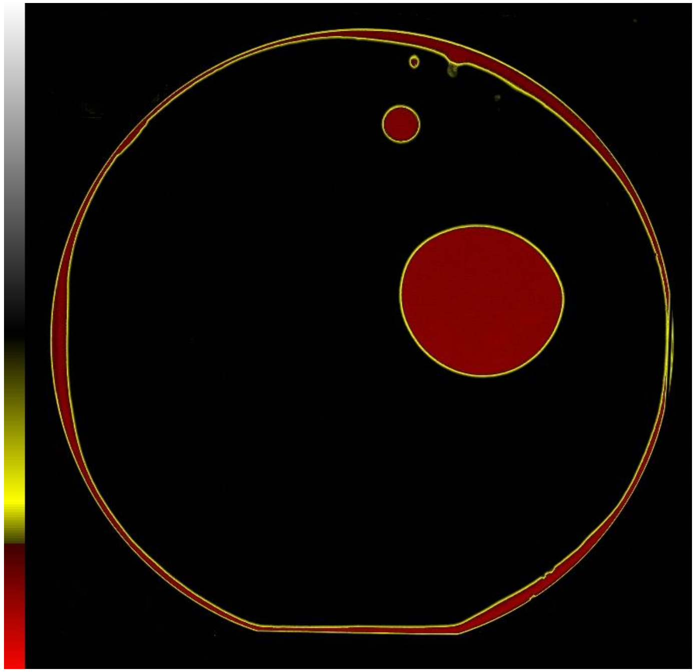


Wafer bonding evaluation

- SAM (Scanning Acoustic Microscopy)



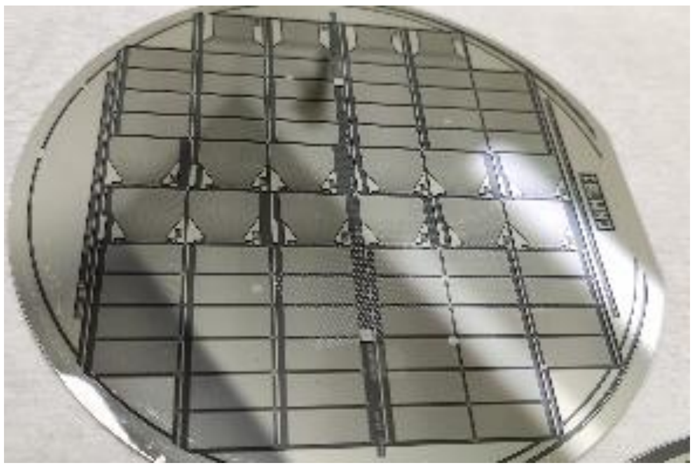
Anodic bonding with micro-channels

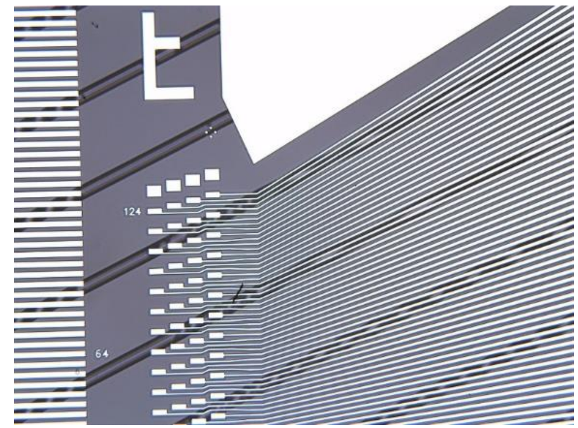


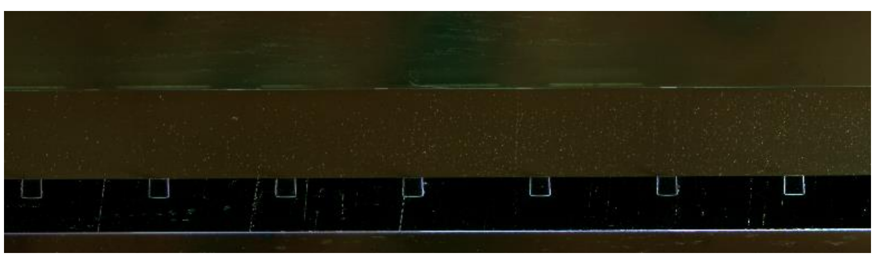
Eutectic bonding blanket

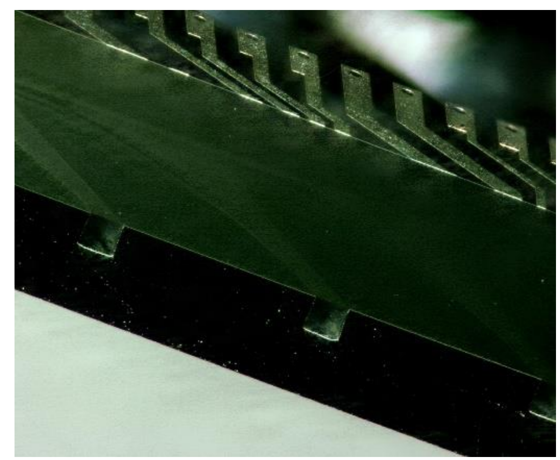
Current status - Results

- Successful integration of micro-channels in silicon interposers with integrated signal (RDL) – Pre-processing







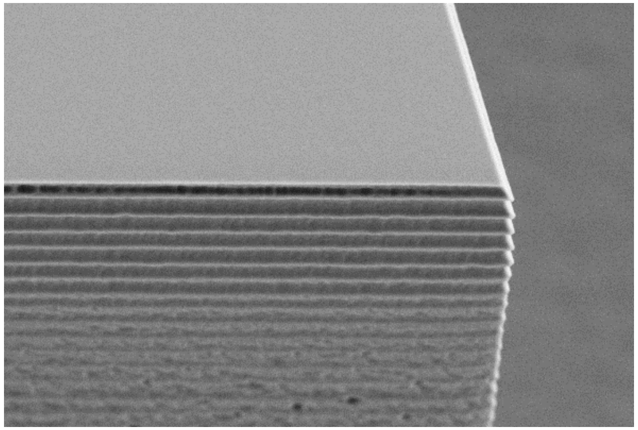


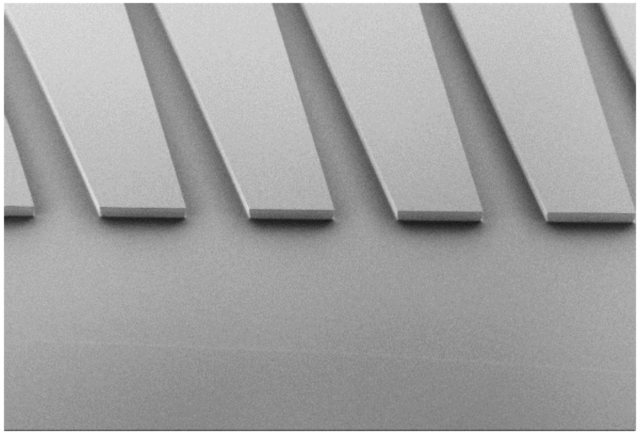
Future work

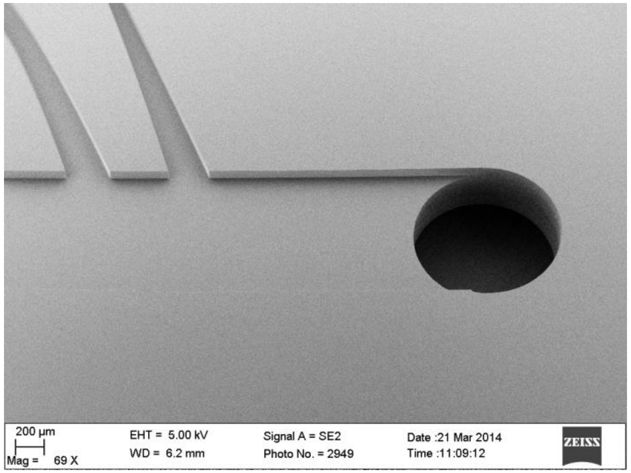
- Post-processing
  - ➢ Metal degradation seems solved
  - ➢ Doing additional tests
  - ➢ Further processing, next
  - ➢ Possibility of depositing the metal in the silicon side
- Improve Eutectic bonding
- Fluidic and thermal tests (in collaboration with IFIC)
- Work towards the compatibility with CMOS process

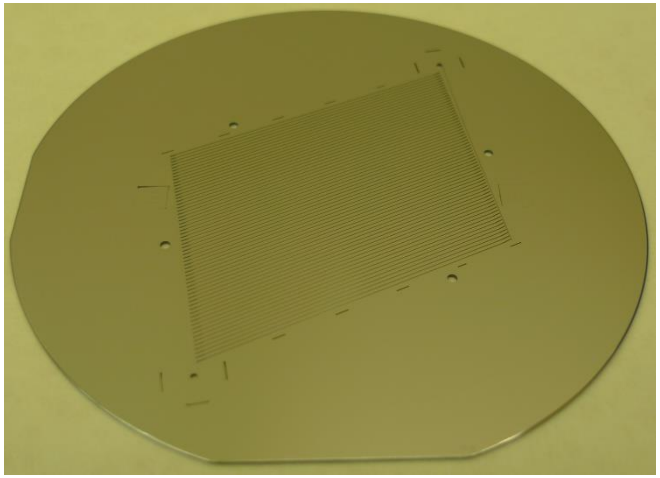
Backup

Micro-channels



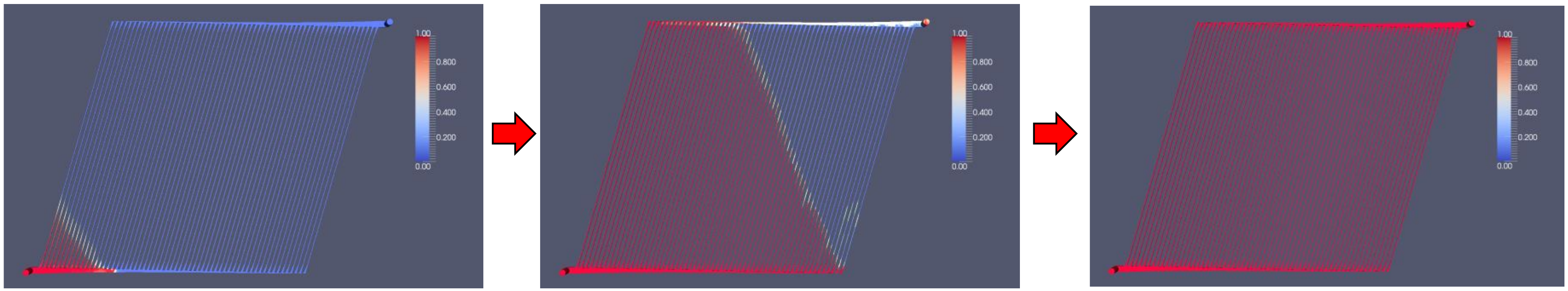




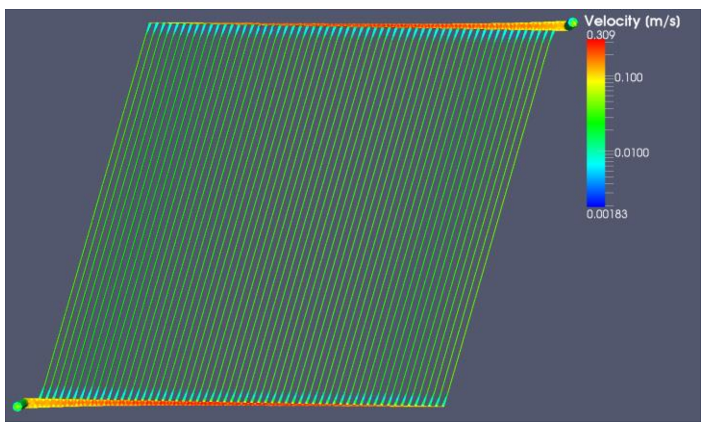


Simulations (DESY)

- Initial filling of micro-channels
  - No “clogging” (air voids)



- Velocity distribution

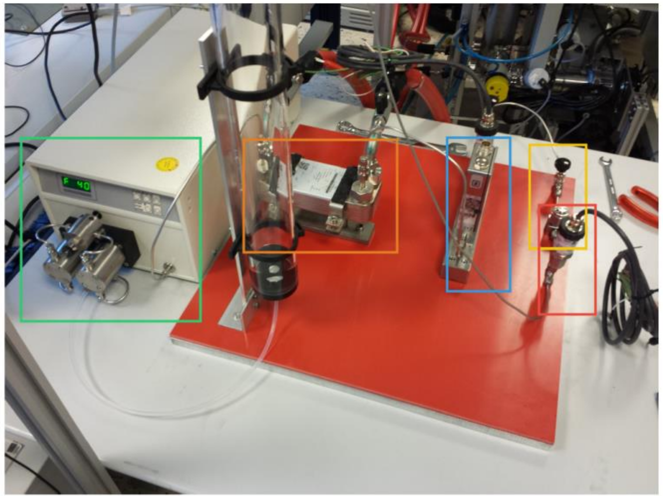


- Flow and thermal simulations (in comparison with tests)

Hydrodynamic tests

Setup

- Green: Pump
- Orange: Heat Exchanger
- Blue: Flow Meter
- Yellow: Valve & Filter
- Red: Pressure Sensor
- Transparent column: Fluid Reservoir



Pressure vs. Flow

- ➢ Simulation with laminar flow model
- ➢ Good simulation agreement with prototype A, B and D
- ➢ Most likely prototype C has some flow problems
- ➢ Critical pressure around 31 bar