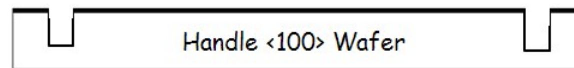
AIDAinnova WP10 @ MPG HLL, Munich

- direct wafer bonding and post-processing –

Laci Andricek for the HLL team

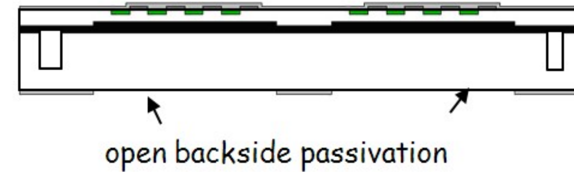
Current Processing Scheme

a) oxidation and back side implant of top wafer

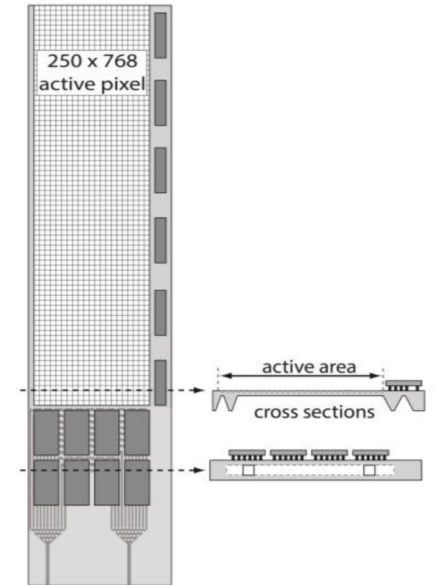


b) wafer bonding and grinding/polishing of top wafer

c) process ➔ passivation



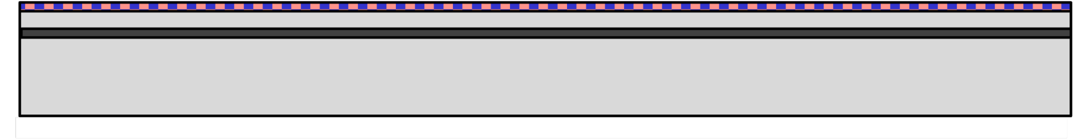
d) anisotropic deep etching opens "windows" in handle wafer



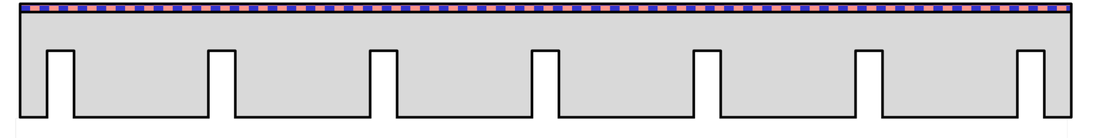
- ▷ Designed for DEPFET sensors for HEP applications
  - ▷ Back side implant first
  - ▷ Wafer bonding/SOI fabrication first, processing of wafers with cavities (C-SOI)
- ▷ C-SOI wafer design and fabrication specific for each project
- ▷ **More flexibility, if cavities are introduced in a post-process step**

Post-processing – key technology modules

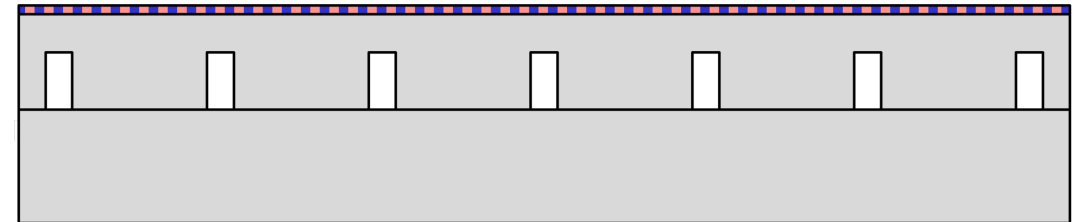
- ▷ Finished SOI wafer with backside implant (DEPFET-like)
- ▷ CMOS wafer w/o backside implant
  - ↳ Up to 8" wafers, polished backside



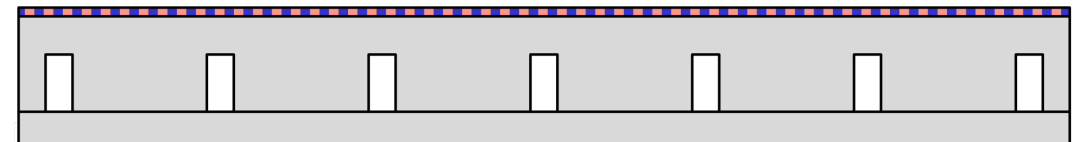
- ▷ ICP-DRIE of micro-channels → to be installed at HLL
  - ↳ Stop on BOX or just after desired etch depth



- ▷ Direct wafer bonding (oxide-oxide) → to be installed at HLL
  - ↳ Has to be a low temperature process, < 400 °C
    - ↳ metals on top, implants …



- ▷ Optional thinning of wafer stack



Direct Wafer Bonding - reminder

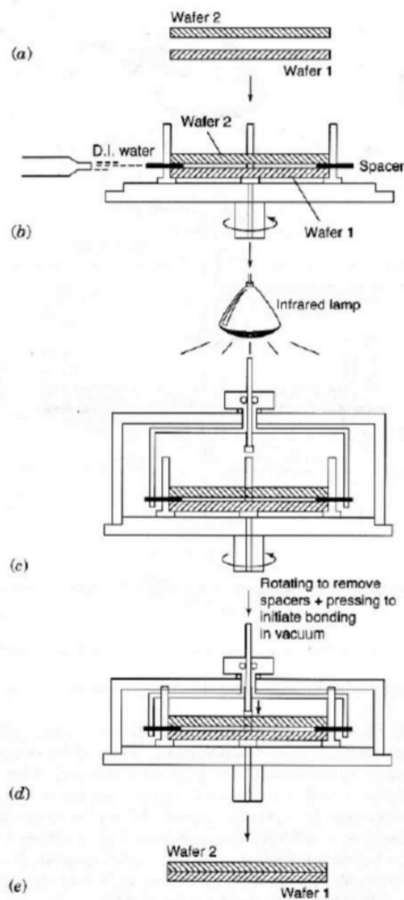
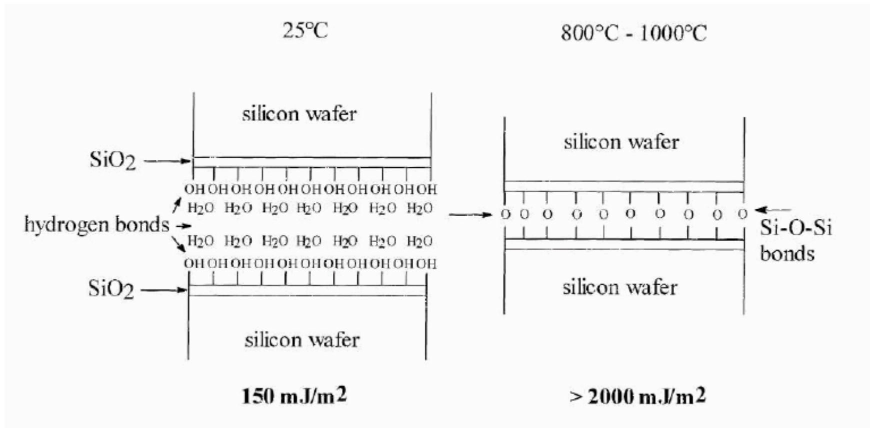


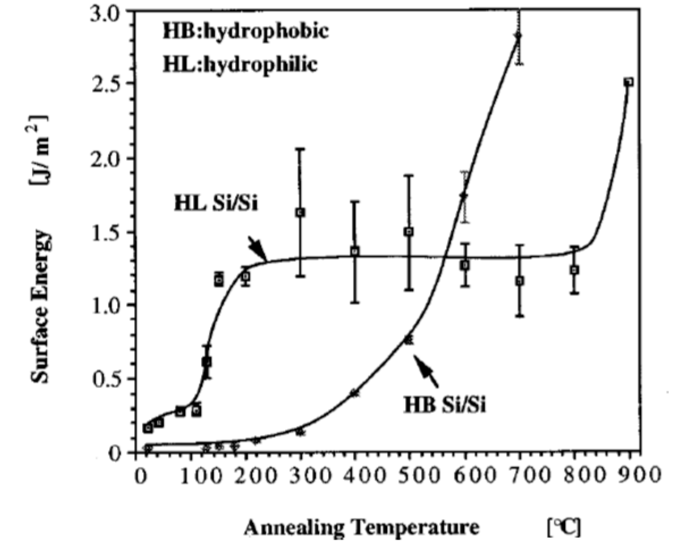
Fig. 4.20 Process flow of wafer bonding in low vacuum.

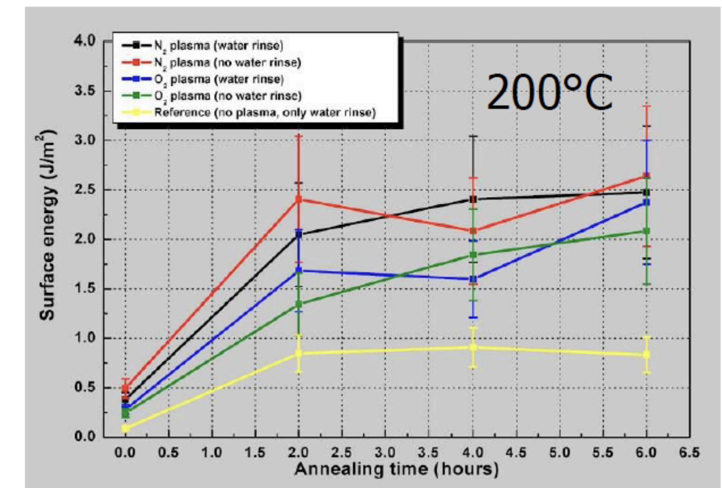
Q.-Y. Tong and U. Gösele "Semiconductor Wafer Bonding" John Wiley & Sons, Inc.



- Relatively simple process
  - ↳ Needs just clean, (very) smooth surfaces
- High Temp. for good bonding (>2 J/m^2)
  - ↳ → not BEOL compatible
- bonding in UHV or with prior plasma treatment reduces annealing temp. well below 400°C

U. Gösele and Q.-Y. Tong, Annu. Rev. Mater. Sci. **28**, 215 (1998)

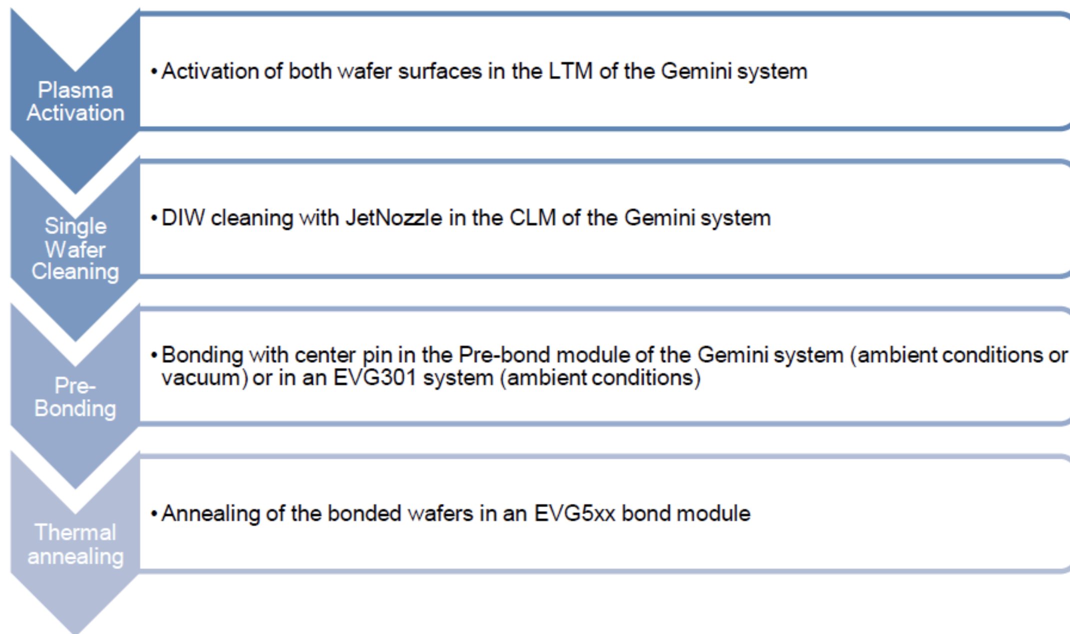




"Plasma Activation – An Enabling Technology for Wafer Bonding", Eric F. Pabo, EV Group, Semicon West 2010

2nd round of testing at EVG, Austria

- ▷ 1st DWB tests at equipment manufacturer EVG very successful
  - ↳ Focused on bonding of implanted oxide, tests still yielded surface energies of about 1 J/cm^2 (reported at last workshop)
- ▷ 2nd round to optimize surface energy at low annealing temperature
  - ↳ Twelve 6" DSP FZ wafer pairs prepared at HLL (oxidation, cleaning)
    - ↳ six pairs as path finder for best parameter set (plasma/atmosphere/temperature)
    - ↳ six pairs to confirm and increase statistics



Gemini

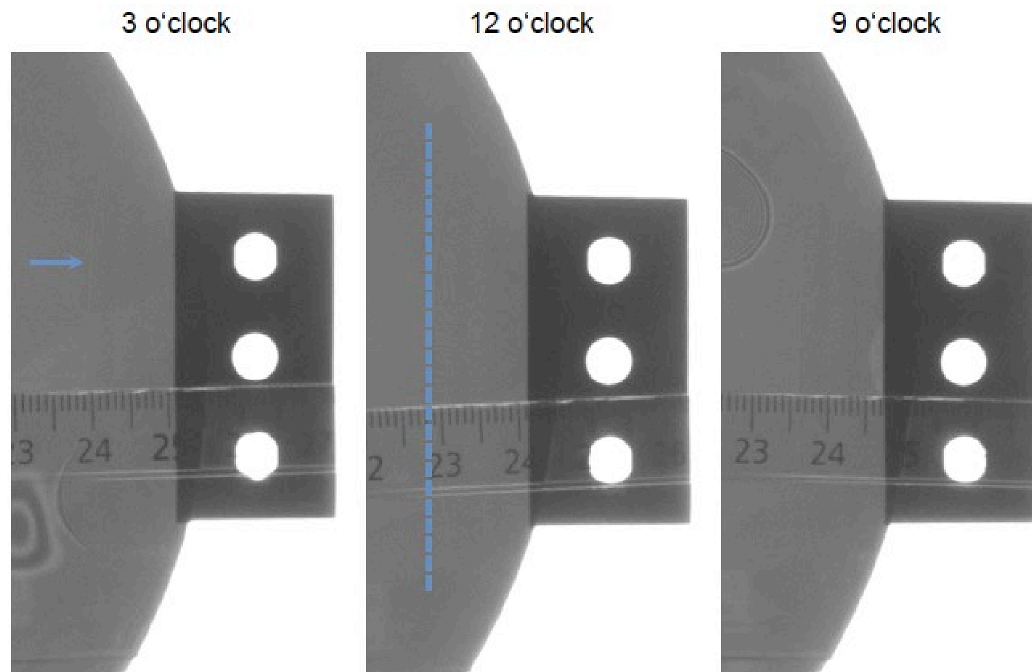
EVG301

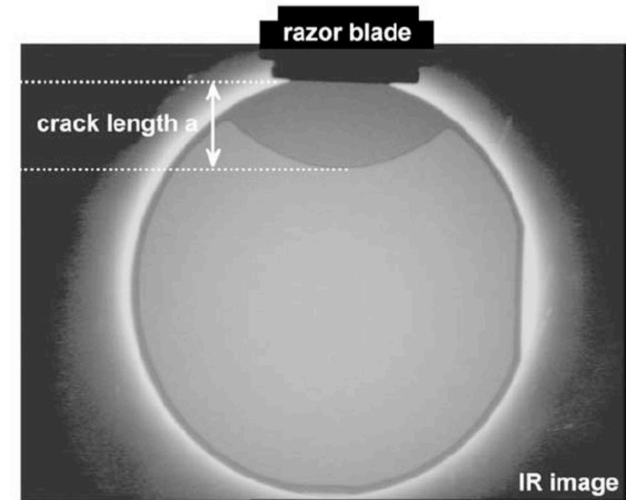
Determination of bond strength – Maszara method

- After bonding and annealing insert blade and measure resulting crack length, simplified:

$$\gamma = \frac{3}{32} \cdot \frac{E t_w^3 t_b^2}{a^4}$$

- In real life more difficult to see, measured at three locations along the wafer circumference





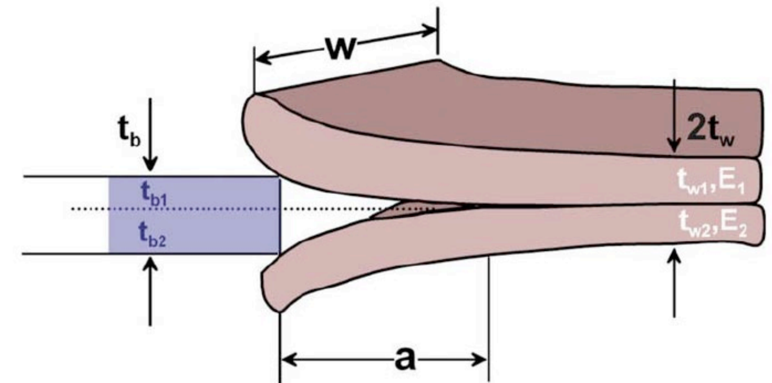
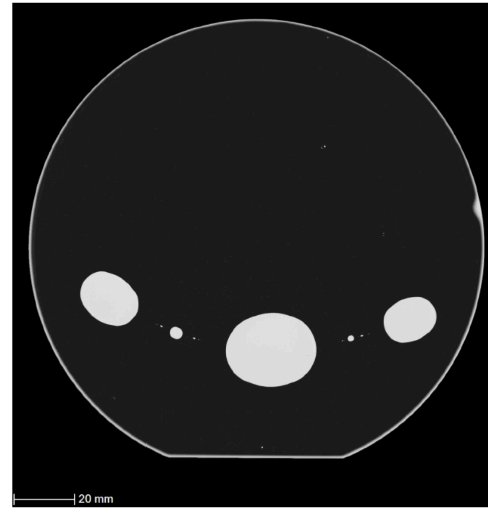
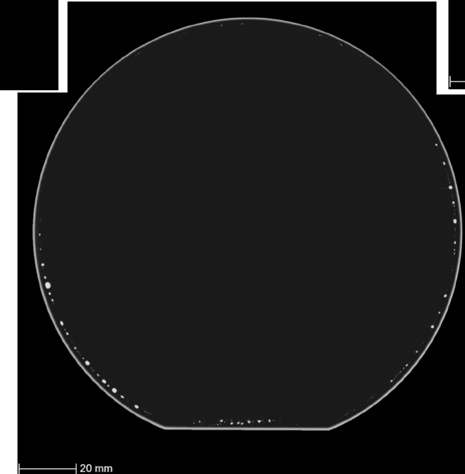


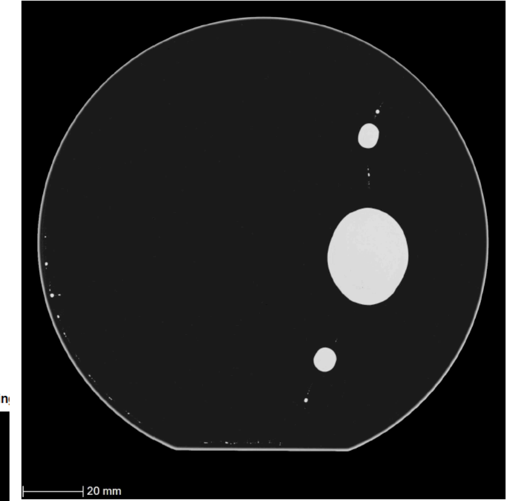
Fig. 24. (Top) IR image of a crack opening initiated by a razor blade. Crack length can be measured as indicated. (Bottom) Schematic diagram of the crack opening method (also known as double-cantilever beam test).

Christiansen et al.: Wafer Direct Bonding, Vol. 94, No. 12, December 2006 | Proceedings of the IEEE

Bond results







- ▷ 9/12 bonds look like this
- ▷ 3/12 bonds with edge voids and larger area voids due to particles or surface quality variations

Bond quality

bond #	plasma	environment	annealing	bond (J/m²)	voids
1	EVG baseline	ambient	200°C/5h	1.76	edge voids
2	EVG baseline	ambient	150°C/5h	1.72	large area voids
3	EVG baseline	vacuum	EVG baseline	1.56	zero
4	high ion flux	vacuum	200°C/5h	1.20	zero
5	med. ion flux, low energy	vacuum	150°C/5h	1.23	in handling area
6	**EVG baseline**	**ambient**	**EVG baseline**	**2.20**	**few edge, one center**
7	EVG baseline	ambient	EVG baseline	2.15	large area voids
8	EVG baseline	ambient	EVG baseline	2.28	edge voids
9	EVG baseline	ambient	EVG baseline	1.93	edge voids
10	EVG baseline	ambient	EVG baseline	2.14	edge voids
11	EVG baseline	ambient	EVG baseline	1.87	edge voids
12	EVG baseline	ambient	EVG baseline	1.83	edge voids

In Summary

- HLL is establishing a 200 mm post-processing line for integration of fluidic channels in sensor wafers, CMOS wafers or active interposers
- Key technology modules are ICP-DRIE ("Bosch process") and plasma assisted direct wafer bonding
  - ↳ ICP-DRIE not reported here
- Qualification runs with low temperature bonds at the equipment manufacturer EVG showed very promising results
  - ↳ Bond energies of plasma activated bonds after low temperature annealing (below 350 °C) are around 2 J/cm^2, comparable to high-temperature annealed bonds.
- Next steps:
  - ↳ Prepare C-SOI wafer with realistic micro-channel geometry, wafer bonded at low temperature, and conduct pressure tests
  - ↳ in parallel continue qualification, purchasing and installation of DRIE and DWB equipment.

- Thanks for your attention –

- This is the way 😉 -