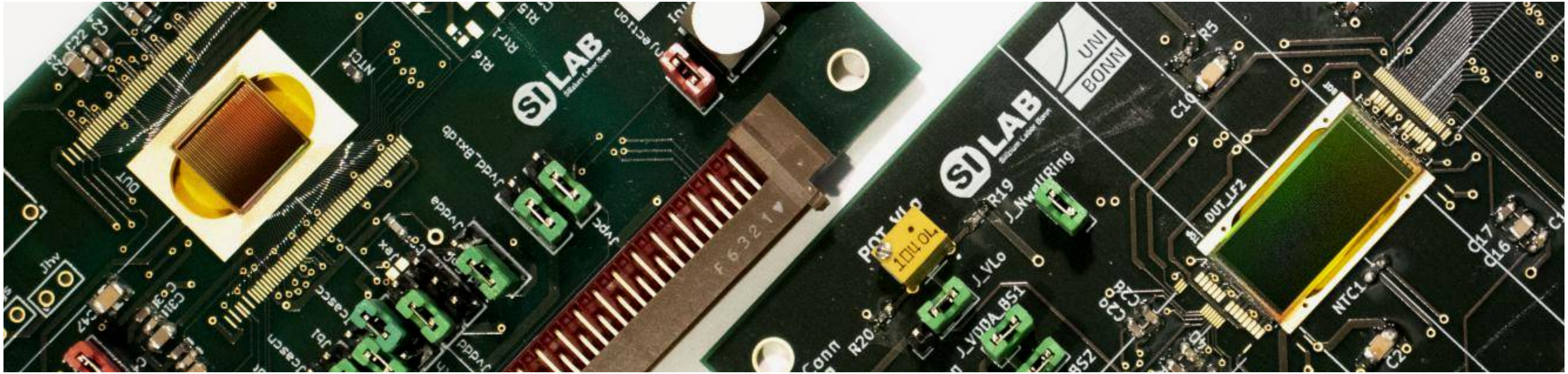
2ND AIDAINNOVA ANNUAL MEETING

RECENT RESULTS ON IRRADIATED LF-MONOPIX2

Lars Schall on behalf of the LF-Monopix testing team

Outline

- The LF-Monopix Chips
- Laboratory test of irradiated LF-Monopix2
- Testbeam results of irradiated LF-Monopix2
- Conclusion and upcoming plans



The LF-Monopix Chips

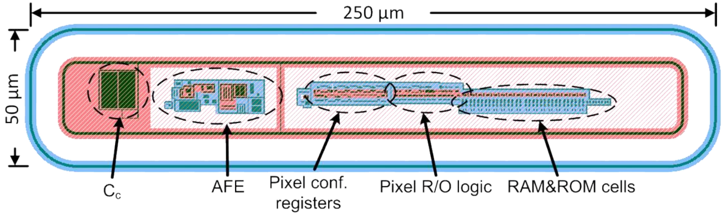
- 150nm LFoundry CMOS Technology
- **Large collection electrode** design
- Substrate resistivity > 2 kΩcm
- Fast **column drain readout** architecture (FE-I3 like)
- **Full in-pixel R/O electronics**

LF-Monopix1:

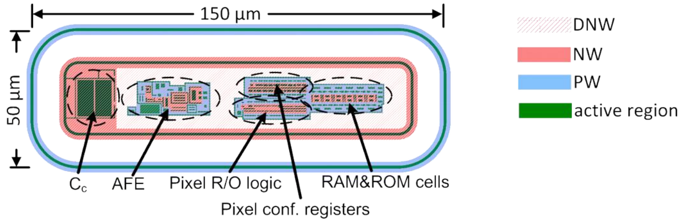
- ~1x1 cm² matrix
- 50x250 µm² pixel pitch

LF-Monopix2:

- ~2x1 cm² matrix
- 50x150 µm² pixel pitch



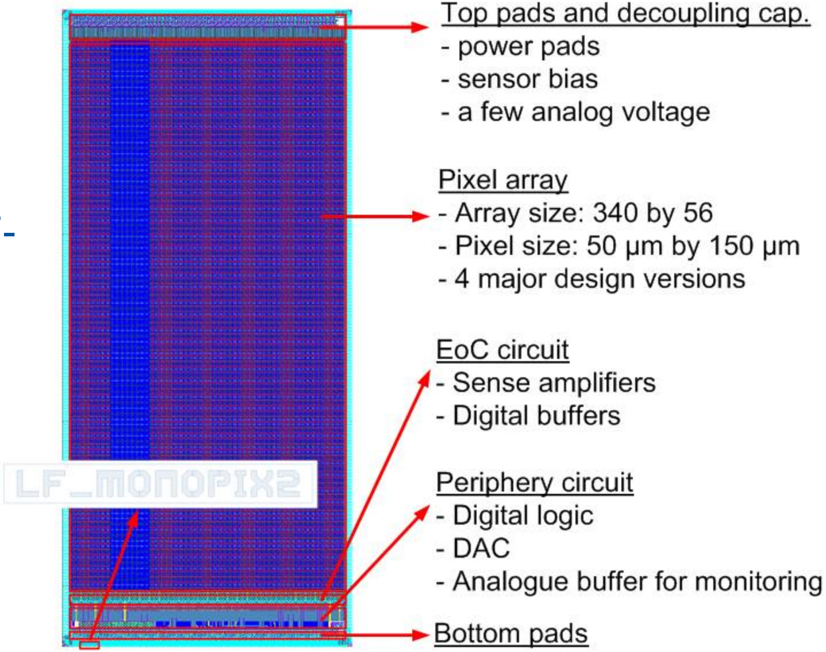
LF-Monopix1 (Mar 2017)



LF-Monopix2 (Feb 2021)

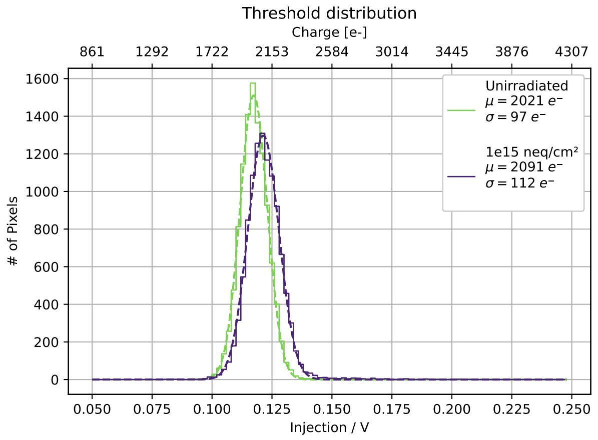
LF-Monopix2: Design

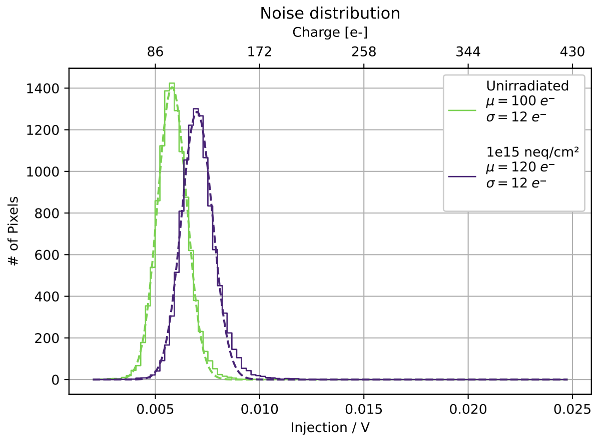
- Column drain readout architecture and **full column length**
  - Improved pixel layout to **mitigate cross-talk**
- Total of 6 matrices with 3 CSA types
  - Largest matrix with proven FE design from LF-Monopix1
- **6 bit ToT** information
- 4 bit **in-pixel threshold DAC**
  - Two different tuning circuit designs
- Wafers successfully **thinned** down **to 100 µm** and **backside processed**



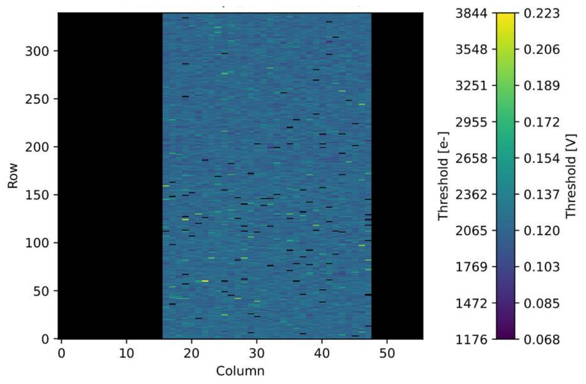
Laboratory Tests

- Available fluences – **unirr | 1e15** neq/cm² **| 2e15** neq/cm² (lab tests ongoing)
  - **Proton irradiation**: 1e15 at Bonn cyclotron, 2e15 at Birmingham MC40 cyclotron
- Operate irradiated chips at -20°C, unirr at room temperature
- Able to tune to approx. **2ke⁻ threshold** and **~100e⁻ dispersion** after irradiation
  - 20% **increase in ENC** after irradiation to 1e15 neq/cm²



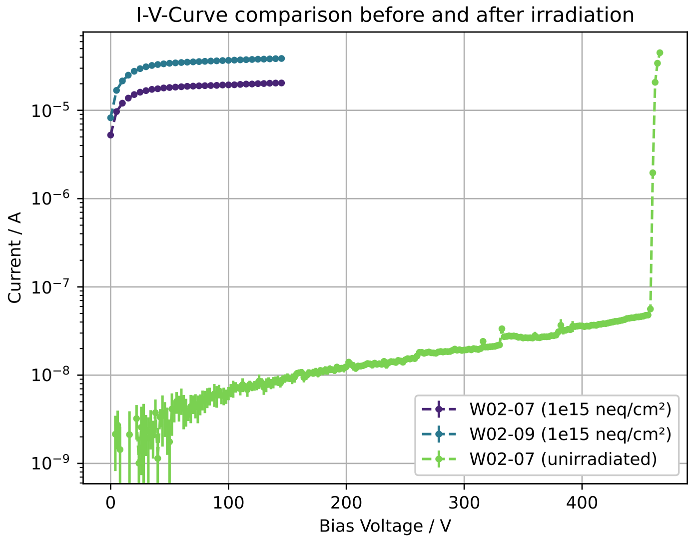


Threshold Map



I-V-Curves

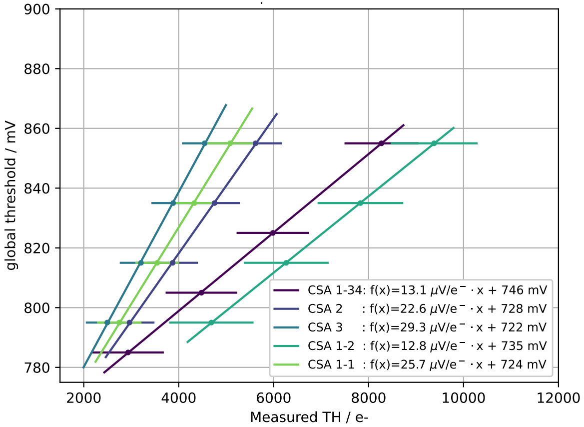
- **Breakdown** voltage between **450 - 500V** for unirradiated chips
- Expected increase in leakage current after irradiation
  - **Unirradiated @ room temperature**
  - **Irradiated 1e15 neq/cm² @ -15°C**
  - No temperature scaling done here
- Difference after irradiation still under investigation



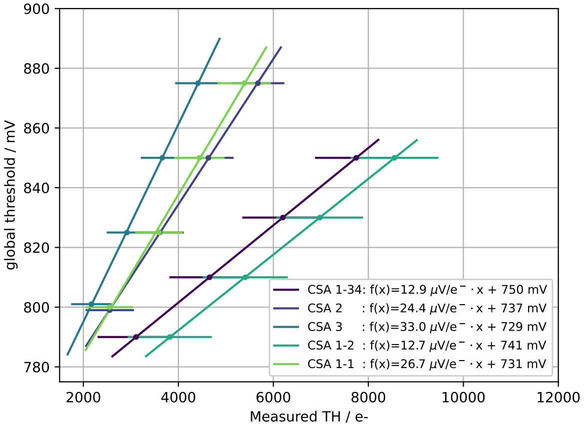
Gain Measurements

- Measure untuned threshold at different global threshold settings
  - Gain extracted from linear regression
  - Smaller $C_{feedback}$ → larger gain → faster LE rise time
- Gain slightly increased for *large gain matrices* after irradiation

Gain Unirradiated



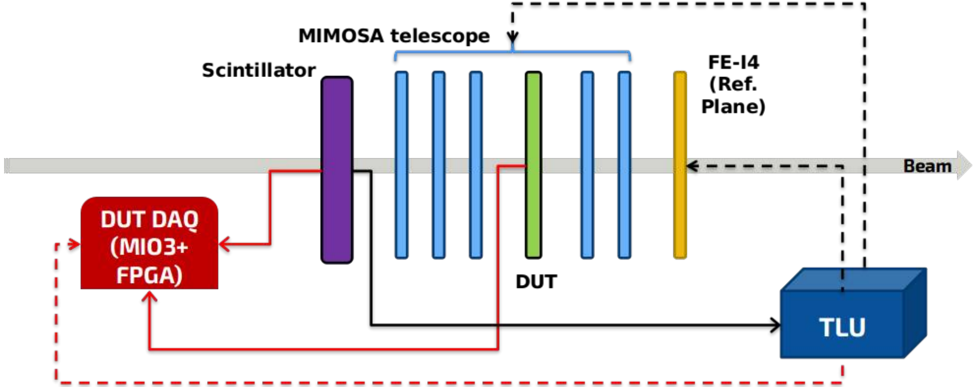
Gain Irradiated (1e15 neq/cm²)

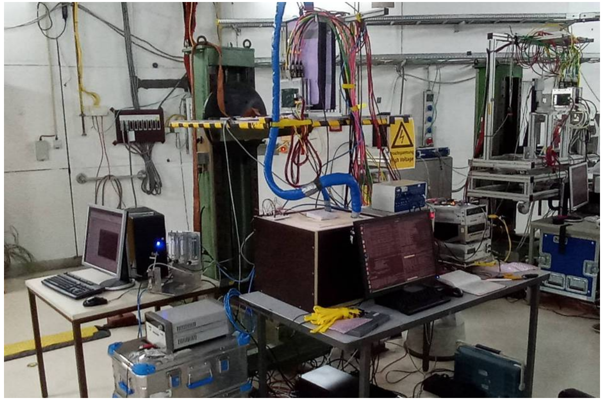


Testbeam Setup

- DESY: **5 GeV electron beam**
- Telescope setup:
  - Scintillator
  - EUDET type beam telescope
  - FE-I4
  - Trigger Logic Unit (TLU)
  - DUT (LF-Monopix2)
- **Irradiated DUT cooled to -20°C**
- Sample **Scintillator**, **DUT hit**, **TLU trigger** in DAQ for event building

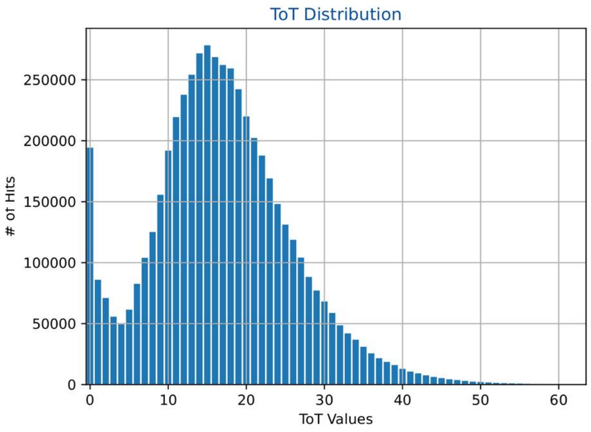
Following TB results measured with a 1e15 neq/cm² irradiated chip

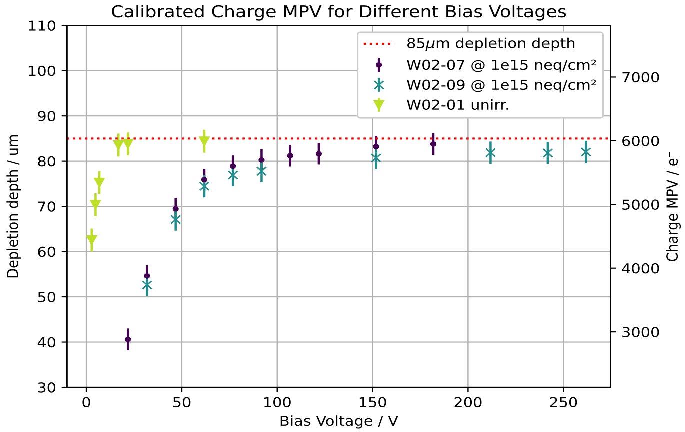




Depletion Depth

- All chips operated at roughly 2ke⁻ threshold
- Calculate calibrated charge MPVs from ToT distribution
- **Depletion depth profile of 1e15 irradiated chips in very good agreement**
  - Full depletion reached around 120V bias @ 1e15 neq/cm²
  - ~15V for unirradiated chips

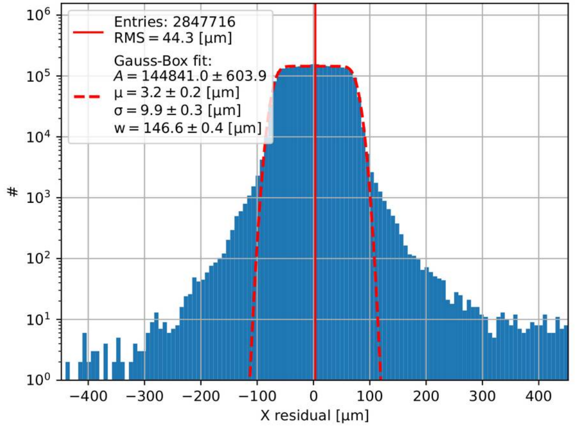




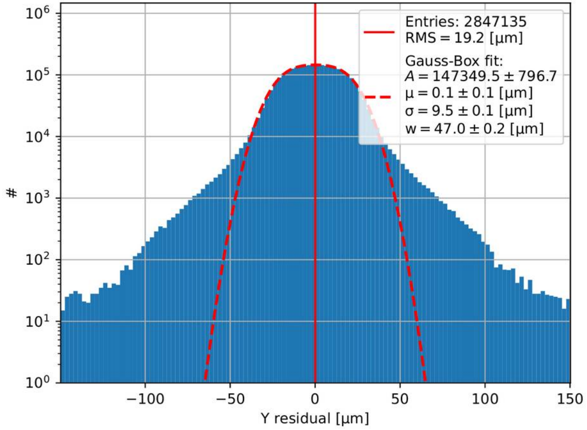
Residuals

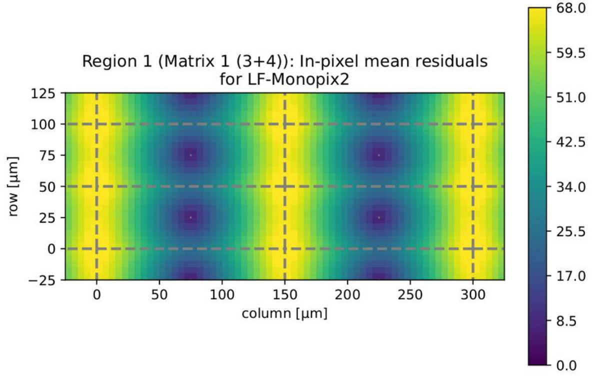
- Testbeam analysis done using *Beam Telescope Analysis*
- Residuals as expected
- Fitted Box-Gaussian to distribution
  - Box width in good agreement with pixel pitch (150 x 50 µm²)

Local X residuals



Local Y residuals

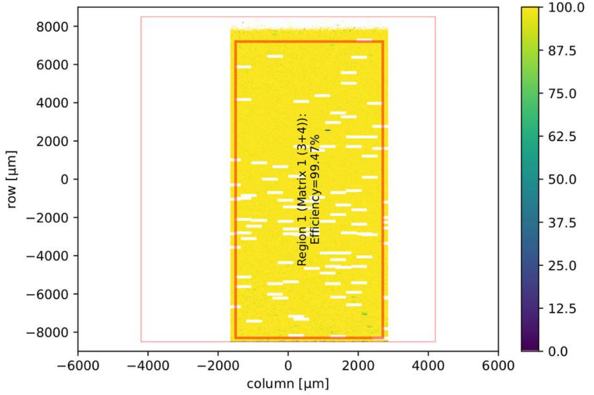




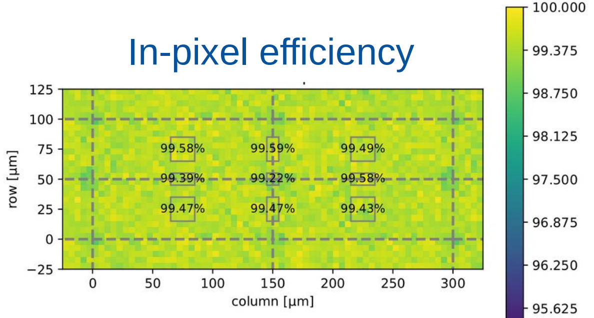
Efficiency Results

- **Uniform hit detection** and **in-time efficiency** across matrix (150V bias, 2ke⁻ threshold)
  - *Data run shown here (99.5 ± 0.1)% hit detection efficiency*
- Projected onto **2x2 in-pixel** plots for in-pixel studies
- Combine data runs to achieve higher statistics (if necessary)

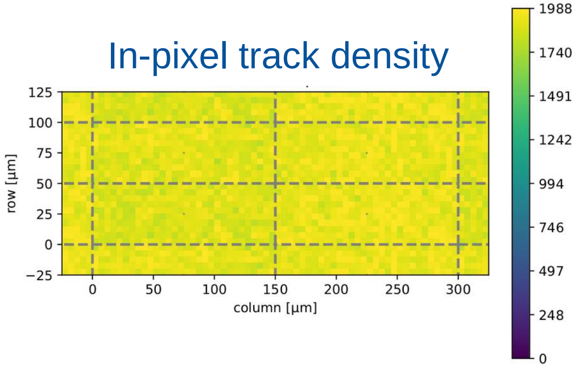
Efficiency Map



In-pixel efficiency



In-pixel track density



Efficiency Results

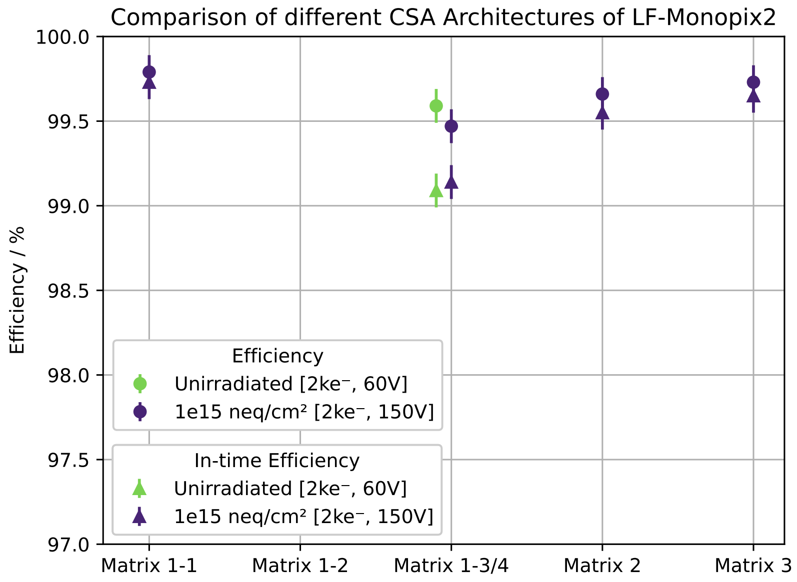
<u>1e15 neq/cm²:</u>

- **Hit detection** and **in-time efficiencies > 99%** at **2ke⁻ threshold** and **150V** bias voltage

<u>2e15 neq/cm²:</u>

- Problems with cooling setup
- Could not reach reasonable threshold
- Large increase in leakage current
- <u>But</u> could talk to chips continuously

Unirradiated result at **2ke⁻ threshold** and **60V** bias voltage as comparison



→ **No significant efficiency** loss after irradiation to **1e15 neq/cm²**

→ **No stable operation possible** at latest testbeam with **2e15 neq/cm²** irradiated chips

Efficiency Threshold and Bias Run

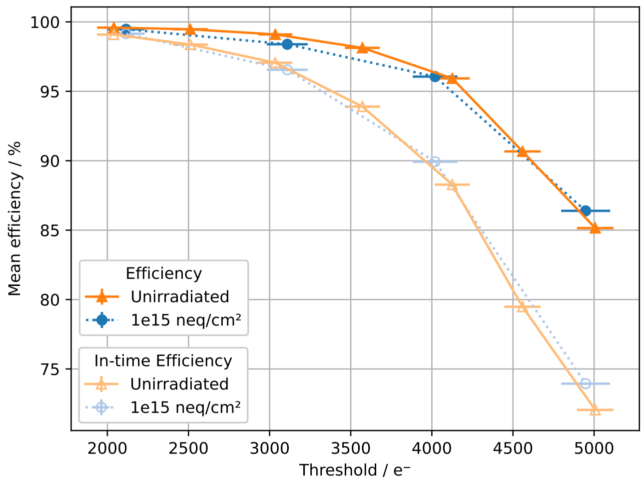
Efficiencies at different **thresholds**:

- **Decrease in efficiency for higher thresholds**

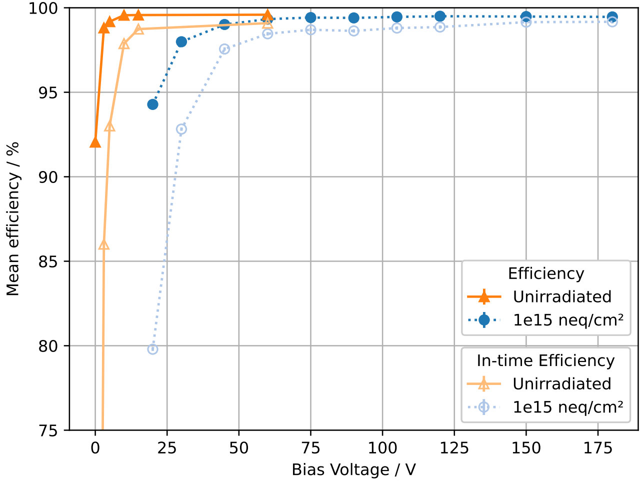
Efficiencies at different **bias voltages**:

- **Increase in efficiency for higher bias voltages** until full depletion of sensor

Efficiency vs Threshold



Efficiency vs Bias Voltage



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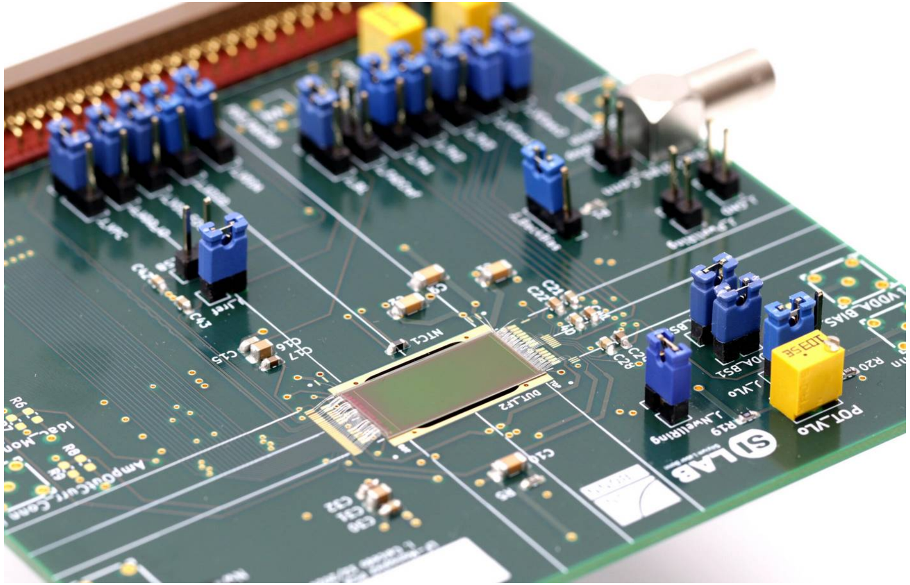
Conclusion and Outlook

- **LF-Monopix2** fully functional and efficient after **irradiation to $1x10^{15}$ neq/cm²**
  - Measured **hit detection efficiencies > 99%** for all FE designs
- **Cooling setup and leakage current problems** lead to difficulties at testbeam with **$2x10^{15}$ neq/cm² irradiated chips**



Upcoming:

- Detailed lab tests with 2e15 neq/cm² irradiated sensor
  - Check possible leakage current issues
- TID irradiation campaign

Thank you for your attention!

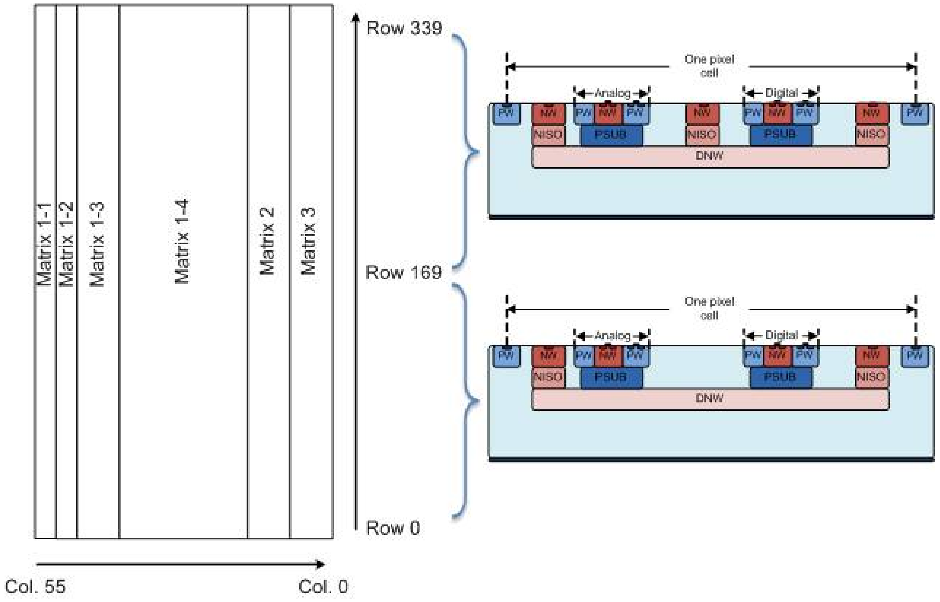
The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under GA No. 675587-STREAM, 654168 (AIDA-2020) and 101004761 (AIDA-Innova)

This project has received funding from the European Union's Horizon Europe Research and Innovation programme under Grant Agreement No 101057511.

Backup

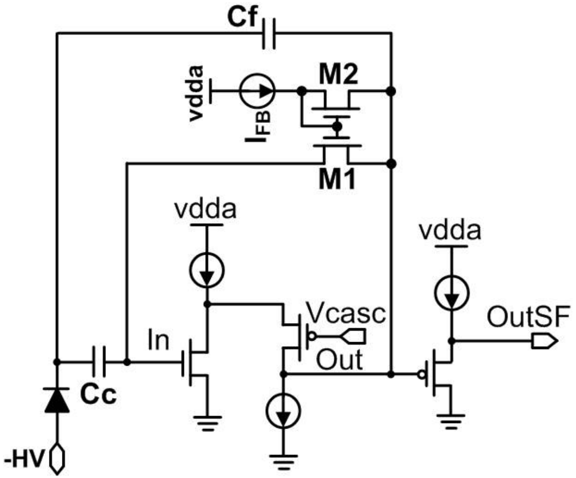
LF-Monopix2 In-Pixel Design



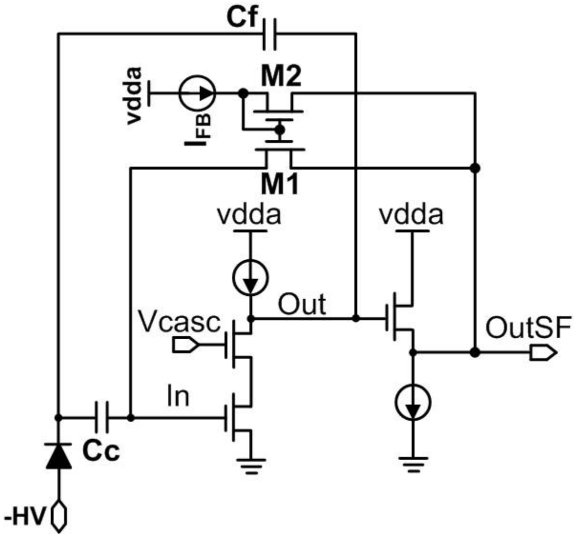
Matrix	Column	CSA	Feedback cap.	Discriminator	Logic
1-1	55 - 52	V1	1.5 fF	Bidirectional tuning	Falling
1-2	51 - 48	V1	5 fF	Bidirectional tuning	Falling
1-3	47 - 40	V1	5 fF	unidirectional tuning	Rising
1-4	39 - 16	V1	5 fF	unidirectional tuning	Falling
2	15 - 8	V2	1.5 fF	Bidirectional tuning	Falling
3	7 - 0	V3	1.5 fF	Bidirectional tuning	Falling

CSA Types of LF-Monopix2

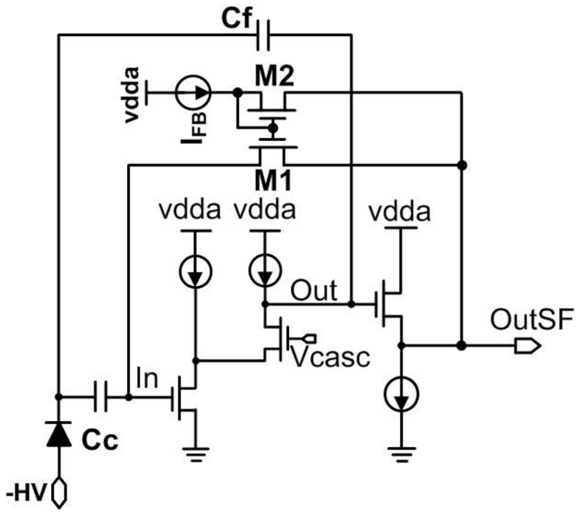
CSA 1
NMOS amplifier from LF-Monopix1



CSA 2
Telescopic cascaded structure

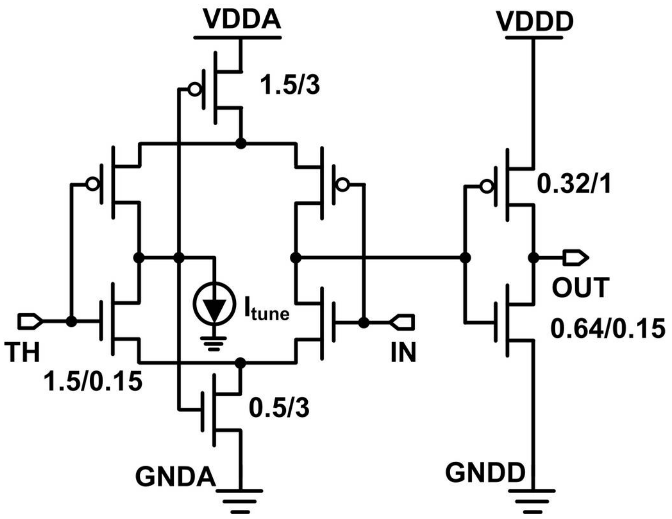


CSA 3
Current into input transistor from two separately adjustable branches

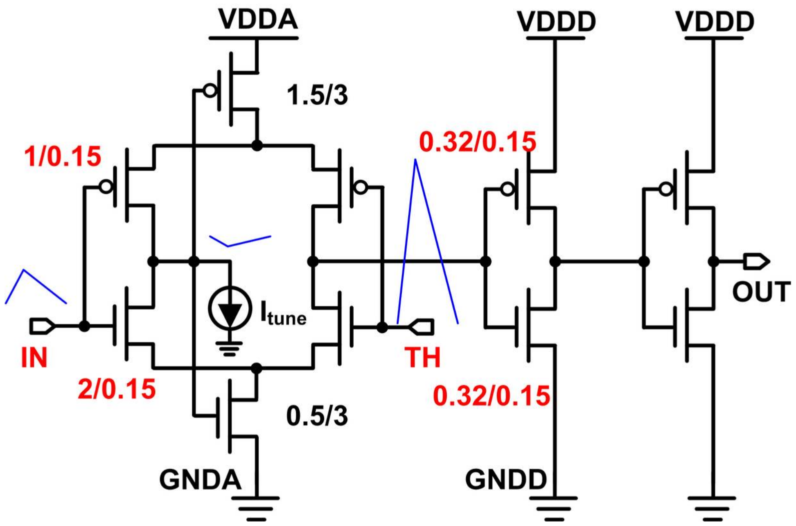


Discriminator Types of LF-Monopix2

Unidirectional
Self-biased differential amplifier followed by a CMOS inverter



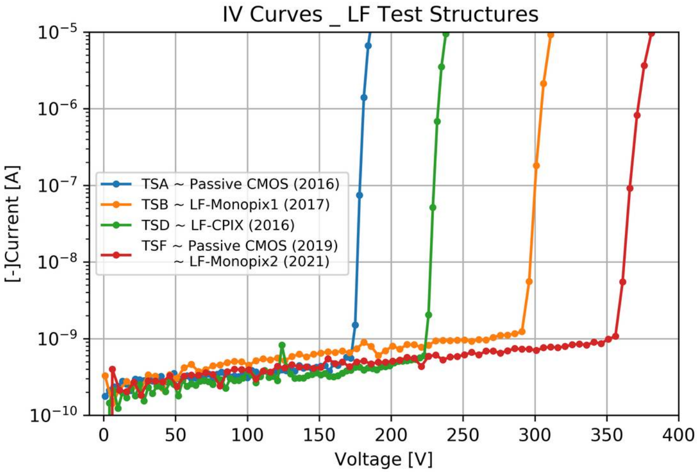
Bidirectional
Optimized transistor dimensions and swapped input ports for faster speed

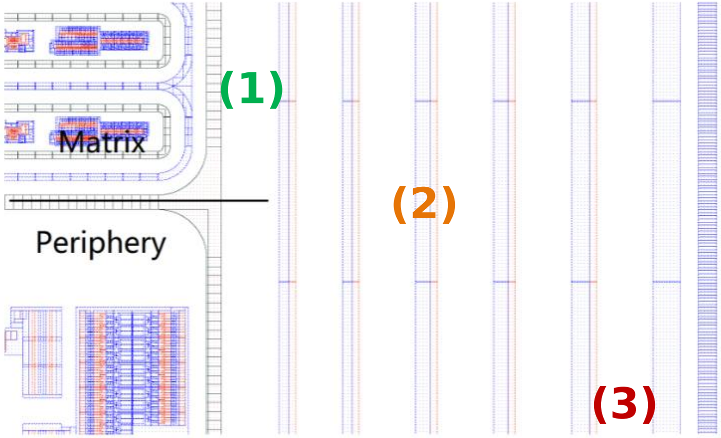


LF-Monopix: Guard Ring Design

Improvement of breakdown voltage achieved by:

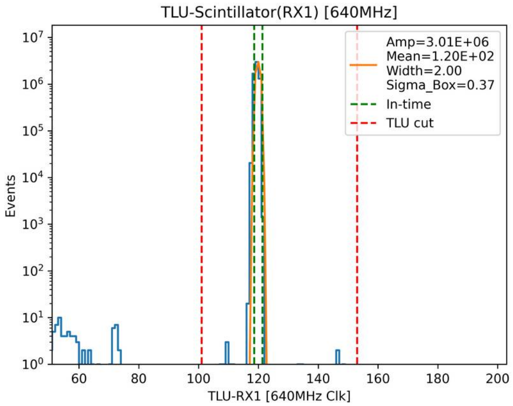
- Adding Deep N-well on innermost n-ring **(1)**
- P+N combination in guard-rings **(2)**
- Reduction of guard-ring number -> Increase in spacing **(3)**

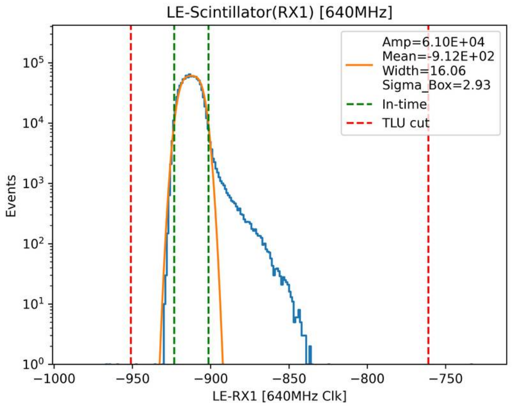




Event Building

1. Match TLU640 with closest Scintillator and TLU timestamp in raw data
2. Look for most frequent frequent value and cut on it (both LF-Monopix2 and FE-I4 data)
3. Match TLU640 with closest DUT hit (leading edge) timestamp
4. Assign corresponding Scintillator timestamp to DUT hit

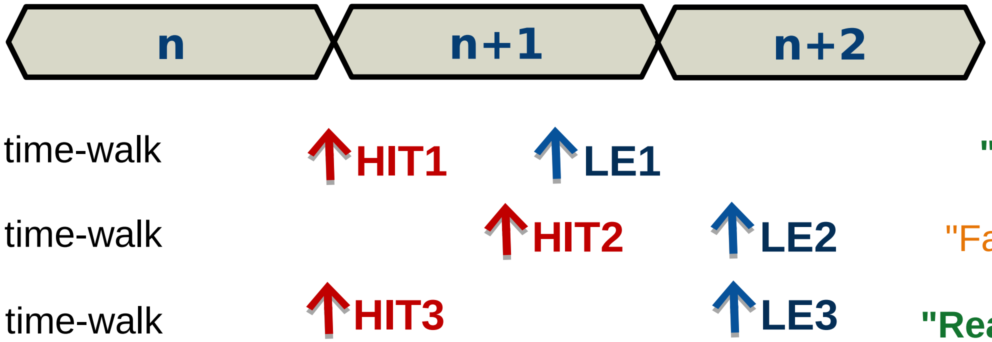




In-Time Events

- LF-Monopix2 is **triggerless**
- Leading edges (LE) sampled at 40MHz (25ns)
- Look at the matched scintillator signals (640 MHz), and find the **time frame where most hits have its leading edge in a single BCID.**

BCID clock (40 MHz)



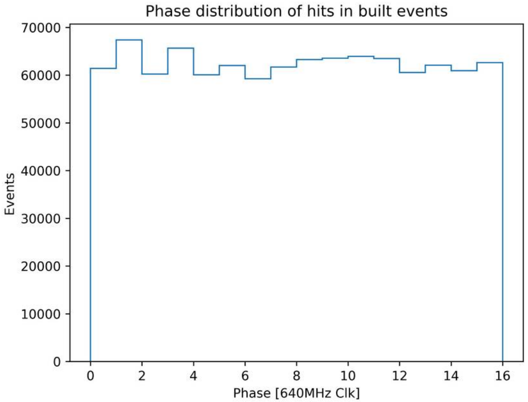
1: Hit at start of BCID + Short time-walk — **"Real"** In-time **efficient**

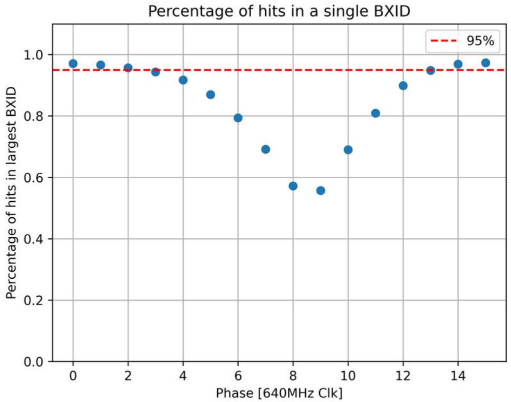
2: Hit late within BCID + Short time-walk — "Fake" in-time inefficiency

3: Hit at start of BCID + Long time-walk — **"Real"** in-time **inefficiency**

In-Time Events

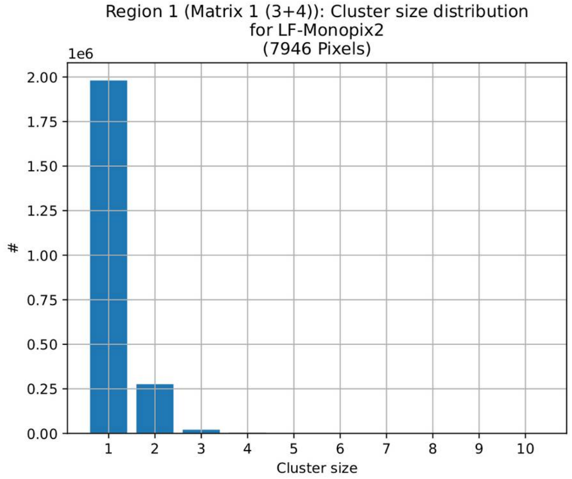
- Events are equally likely to come at any time within a single BCID
- Look at each 640MHz clock within 25ns and quantify percentage of hits in single BCID
- Take events of highest percentage hits in single BCID to analyze **in-time efficiency**
  - Due to jitter of TLU also take the phase before and after into account



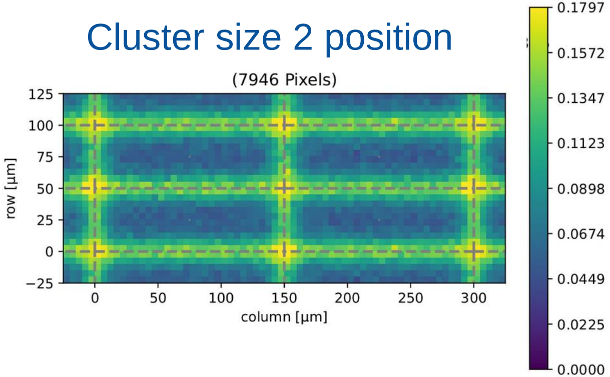


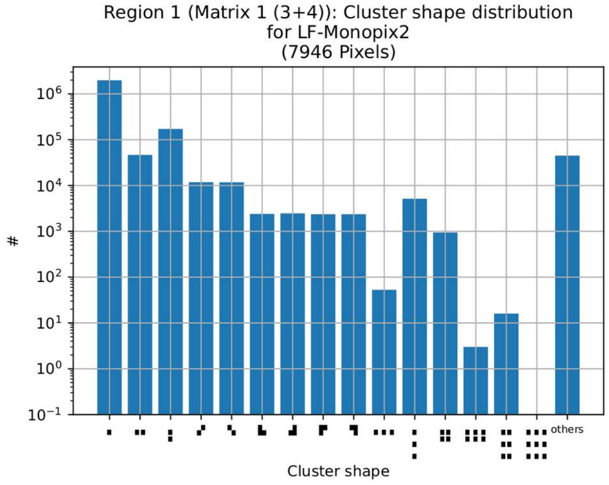
Cluster Size

- Mostly observe single pixel clusters
- Charge sharing likely at pixel edges
- Vertical clusters more likely than horizontal clusters (pixel shape)



Cluster size 2 position





In-Pixel Efficiency for Non-Optimal Operation

- Efficiency loss most prominent in pixel corners (expected)
  - Significant efficiency loss (<96%) already present at:

    → **3ke⁻ mean treshold** @ 150V bias voltage
    → **45V bias voltage** @ 2ke⁻ mean threshold