OBELIX for the Belle II Experiment

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on behalf of the Belle II VTX collaboration

AIDAinnova 2nd Annual meeting

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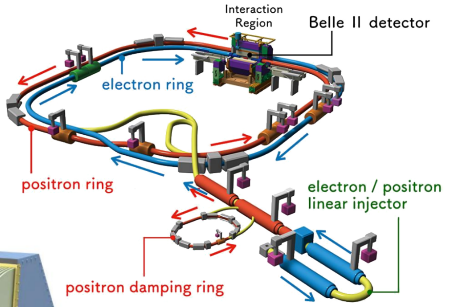
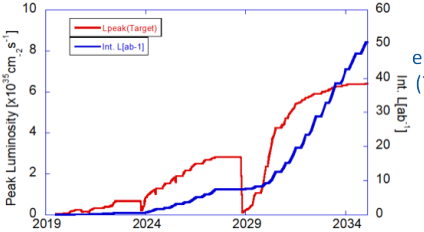
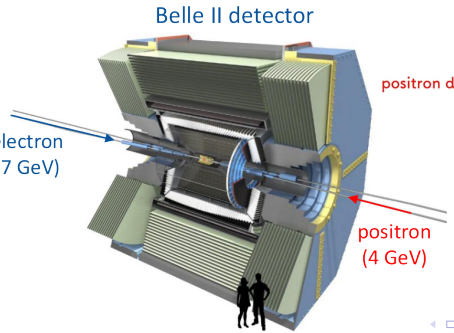
The Belle II Experiment

- Located at the SuperKEKB collider in Tsukuba/Japan
- Asymmetric $e^+ - e^-$ collisions at $\sqrt{s} = M_{\Upsilon(4S)} = 10.58\,\text{GeV}$
- Luminosity-frontier experiment, exploring new physics
- Target: $\mathcal{L}_{int} = 50\,\text{ab}^{-1}$, currently at $0.43\,\text{ab}^{-1}$
- Right now: long shutdown, restart early 2024
- $\mathcal{L}_{inst}$ will be increased stepwise
- Challenging hitrates expected

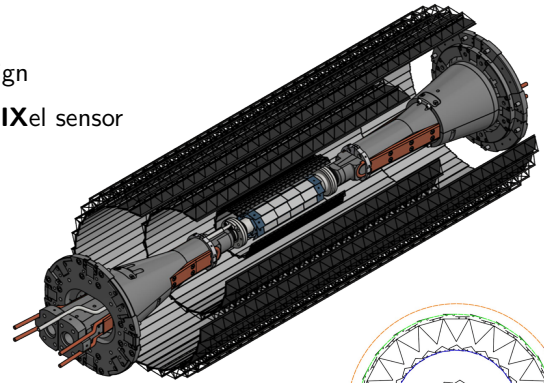


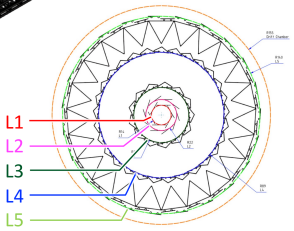




The VTX Upgrade Concept

- Scheduled for 2027/2028
- 5 straight layers with DMAPS in ladder/stave design
- Identical chips on all layers: **O**ptimized **BEL**le II p**IX**el sensor
- Different features enabled on different ladders
- **L1 & L2 (iVTX):**
  - All silicon ladders
  - Air cooling (constrains power)
- **L3 to L5 (oVTX):**
  - Carbon fiber support frame
  - Cold plate with water cooling



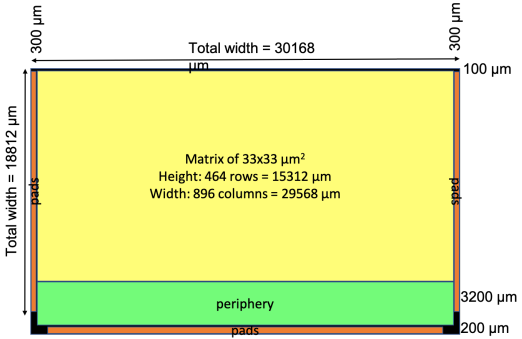


	L1	L2	L3	L4	L5	Unit
Radius	14.1	22.1	39.1	89.5	140.0	mm
# Ladders	6	10	8	18	26	
# Sensors	4	4	8	16	24	per ladder
Expected hitrate	18.0	6.7	1.7	0.45	0.22	MHz/cm^2
Material budget	0.1	0.1	0.3	0.5	0.8	% X_0

OBELIX Key Requirements

1. High hit efficiency at demanding hitrates and radiation levels
   - Matrix inherited from TJ-Monopix2
   - Evaluation still ongoing
2. Handling trigger latency of the Belle II experiment
   - New implementation of digital periphery
   - Simulation to validate performance
3. Power dissipation allowing air cooling of inner layers and water cooling of outer layers
   - Optimized digital logic
4. Low space for cables inside detector
   - 1 or 2 LVDS link(s) per chip (Tx)
   - 2 LVDS links for groups of chips (Clk, CMD)
   - On chip voltage regulators
5. Fast but coarse hit information as input for Belle II trigger
   - Independent data path
   - Low granularity/low latency transmission

The OBELIX chip

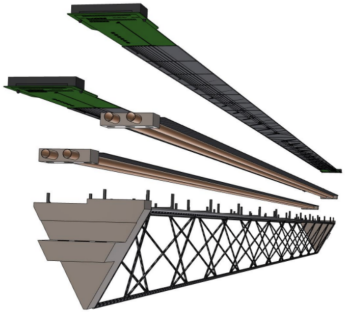


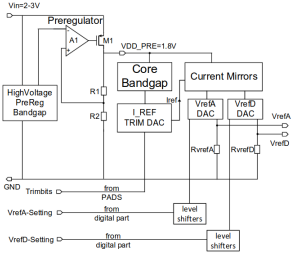
- Matrix from TJ-Monopix2, only size adjusted
- 464 rows and 896 columns
- Timestamp resolution: $\sim 50\,\text{ns}$
- Up to $10\,\mu\text{s}$ trigger latency
- Power: $< 1.5\,\text{W}$ per chip
- TID tolerance: $100\,\text{kGy/year}$
- NIEL tolerance: $5 \times 10^{13}\,\text{n}_{\text{eq}}/\text{cm}^2/\text{year}$
- Hitrates up to $120\,\text{MHz/cm}^2$ (continuous):
  - Safety factor of 5
  - Hitrate spikes due to injection expected

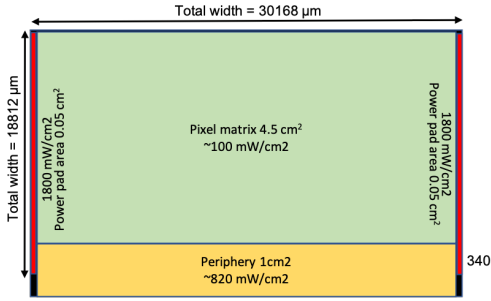
- Fast clock of TJ-Monopix2 is 160 MHz
- OBELIX clock 1/3 Belle II RF (509 MHz)
- Often round numbers stated

Clock signal	Rounded	Real value	Period
Fast clock	160 MHz	169.7 MHz	5.89 ns
Slow clock	20 MHz	21.2 MHz	47.1 ns
TXU clock	32 MHz	33.9 MHz	29.5 ns

OBELIX Power Management





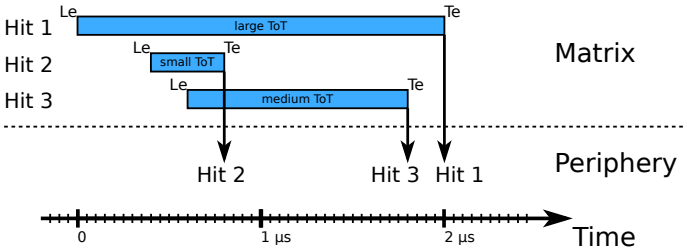


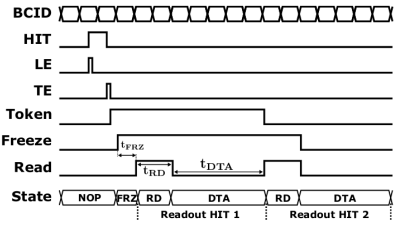
- Long linear ladders: voltage drop across ladder
- Narrow LDOs on both sides of the chip
- Input voltage 2 to 3 V
- LDOs cause some dead area, but TJ-Monopix2 matrix requires power from the sides
- Aspect ratio of regulators as high as possible to keep dead area small

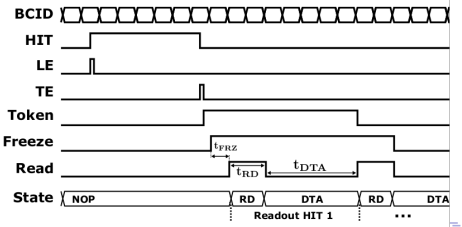
Matrix Readout

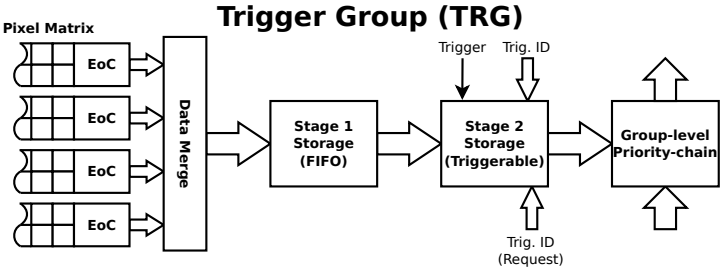
TJ-Monopix2 Readout Scheme:

- Also used in OBELIX
- Charge information over ToT measurement (up to 2 µs, tunable)
- Hit is released to periphery **after trailing edge**
- Leads to time disorder of received hits
- Max ToT defines how late data may come in datastream





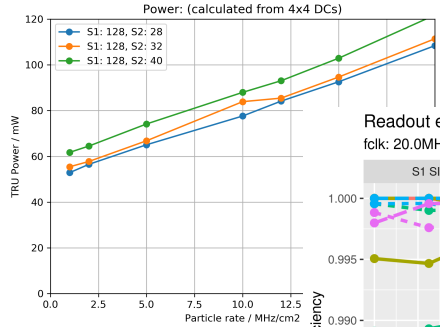




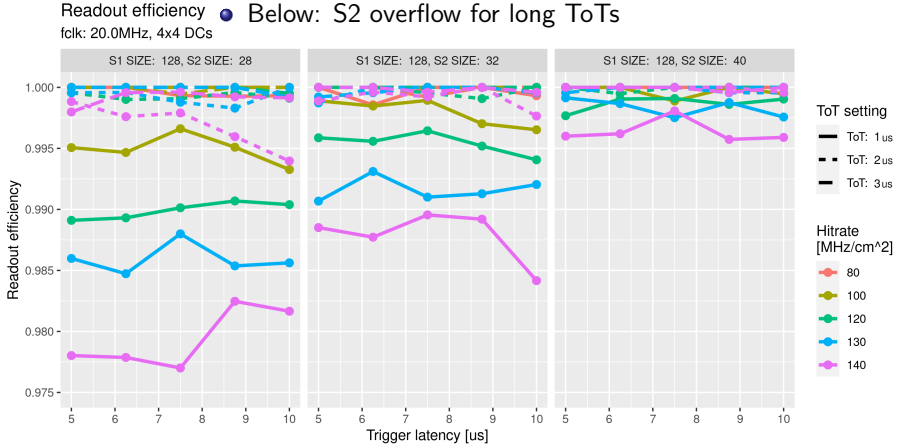
Sophisticated 2-Stage trigger logic:

- Trigger memory organized in 112 Tigger Groups (TRGs), each connected to 4 DCs
- Stage 1 (128 hits): Pre-trigger buffer **SRAM**, low power dissipation
- Stage 2 (32 hits): **Associative memory** to match trigger with hitdata, power hungy
- Time-disorder (2 µs) less than latency (10 µs): S2 can be smaller than S1
- Buffer sizing driven by power dissipation and hitrate, evaluated with extensive simulations

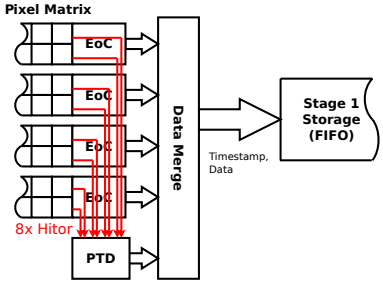
Trigger System: Simulations

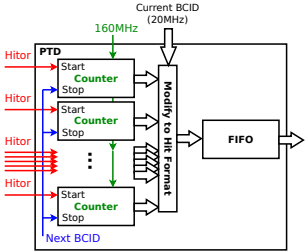


- Simulation includes: hit clustering, ToT vs charge
- Calibrated with TJ-Monopix2 results
- Below: S2 overflow for long ToTs



Peripheral Time to Digital converter (PTD)





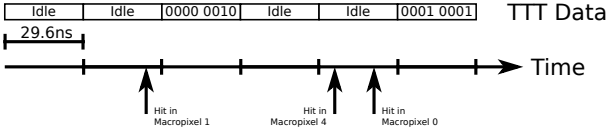
- HitOR: all comparator outputs of one column in an OR-chain (asynchronous)
- PTD: precision timing better than BCID (20 MHz)
- 160 MHz clock frequency
- Power hungry feature: disabled in iVTX
- PTD data stored in (fake-)hit data with nonexistent row addresses
- No extra storage needed for PTD, re-use of large trigger memory needed for higher hitrates
- Little overhead in terms of area/space when disbaled
- Resolution limited by timewalk and PVT of HitOR delay

Track Trigger Transmission (TTT)

- Provide coarse pixel information of all hits to trigger of Belle II (allows track trigger)
- Allows a Belle II trigger based on track information (track trigger)
- Low transmission latency is wanted (leaves more time for trigger algorithm)

Solution: Track Trigger Transmission (TTT)

- Separate transmission logic independent from normal OBELIX readout system (extra LVDS link))
- Power constrains this to the oVTX (outer 3 water cooled layers)
- 2 to 8 logical macropixels per whole chip (configurable)
- 160 MHz DDR transmission (320 Mb/s, 8b/10b encoded)
- No framing, no sync necessary, bit is set when HitOR of macropixel rises



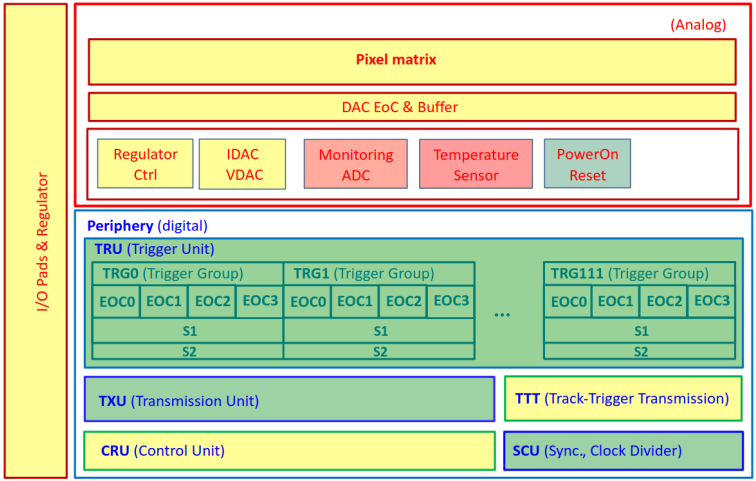
* Additional pipelining steps delaying transmission by 2 other clock cycles not shown here for clearer illustration

Summary and Outlook

- The OBELIX chip is based on the analog part of TJ-Monopix2
- The digital periphery will have several additional features
- Versatile chip for large dynamic range of hitrates
- Still under development, but significent progress recently
- Feature completeness planned for July 2023
- Verification ongoing

Backup slides

OBELIX Block Diagram



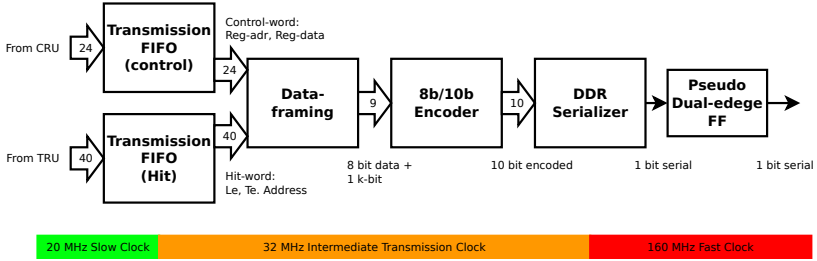
- On chip LDOs (1.8V)
- On chip trigger logic (TRU)
- Fast triggerless output for Belle II Track Trigger (TTT)
- Precision timing counter improve timing for outer layers
- On chip ADC for temperature measurement and calibration

Conceptual phase

Design ongoing

Finished

Transmission Unit (TXU)



- Most TXU components run at 32 MHz (160 MHz/5) intermediate clock
- Serializer needs one byte (10 bit encoded, DDR) per 32 MHz clock cycle
- This allows simple state machines
- Clock boundary to 20 MHz clock is done via FIFO
- Hits are sent in frames sharing the same leading edge BCID

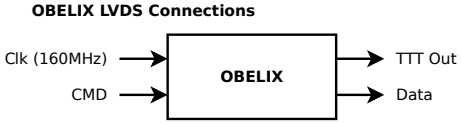
Track Trigger Transmission (TTT)

Goal:

- Provide coarse pixel information of all hits to trigger of Belle II
- Allows a Belle II trigger based on track information (track trigger)
- Power constrains this to the oVTX (outer 3 water cooled layers)
- Low transmission latency is wanted (leaves more time for trigger algorithm)

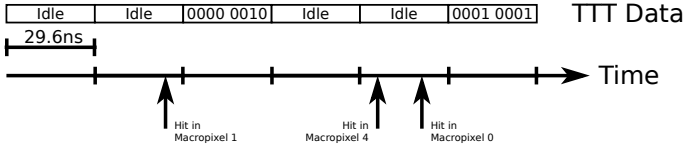
Solution: Track Trigger Transmission (TTT)

- Independent from normal OBELIX readout system
- Separate transmission logic (and extra LVDS link)
- 2, 4 or 8 logical macropixels per whole chip (configurable)
- Whole columns grouped via HitOR (56 to 224 DCs create one macropixel)



TTT: Implementation

- Continous data stream is sent out, 8b/10b encoded
- Bit corresponding to macropixel is set once when rising edge on HitOR
- No data frames, each byte sent stands for its own and defines timing
- No sync needed
- 160 MHz DDR transmission (320 Mb/s)
- Resolution from clock: 29.6 ns (boxlike, $\sigma = 8.5$ ns)
- Uncertainty from HitOR: 35 ns (boxlike, $\sigma = 10.1$ ns)
- Total time resolution: $\sigma \sim 13$ ns



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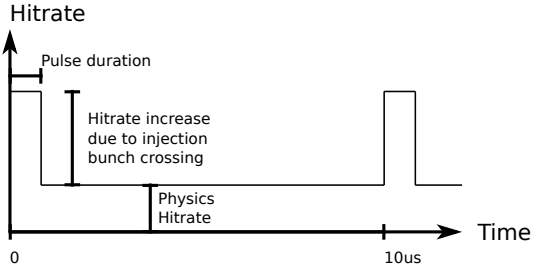
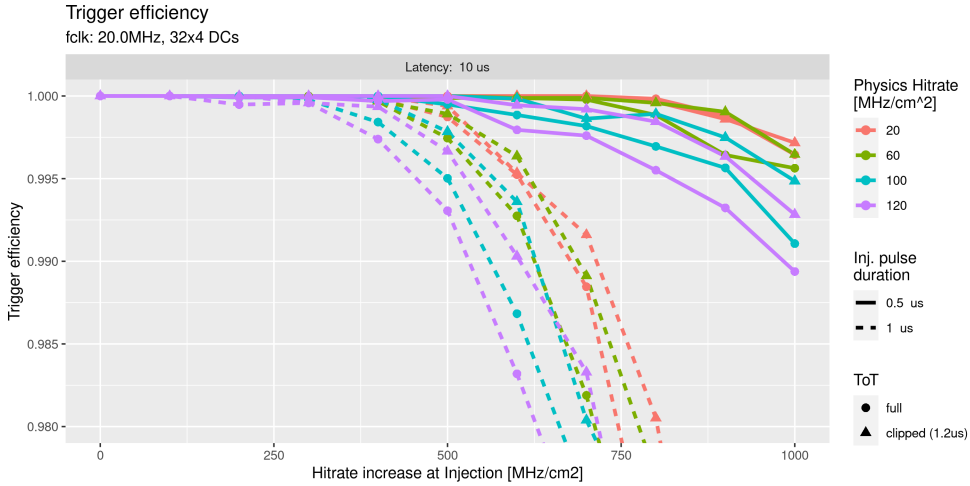
Time dependent Simulation



- Hitrate is time modulated
- To the physics hitrate, an increased pulse is added
- Trigger is NOT vetoed - some triggers will happen during injection bunch
- Two different pulse durations tested: 0.5 µs (expected) and 1 µs (much more demanding)

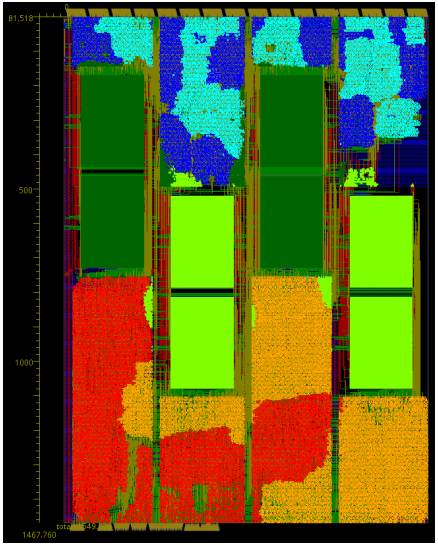
Simulation results TRU (32DCs)



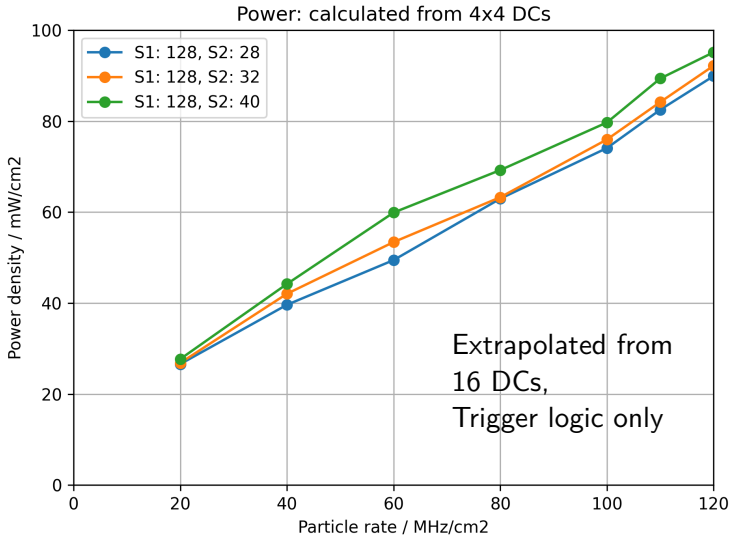
Interpretation

- Short pulses of high hitrate do not degrade performance
- Longer spikes create performance degradation
- For 0.5 µs, up to 800 MHz/cm^2 of BG have low impact (20 MHz/cm^2 physics)
- An additional veto mechanism is probably not necessary
- Trigger probability was constant over time (no veto)
- We might have triggers inside the veto in the future

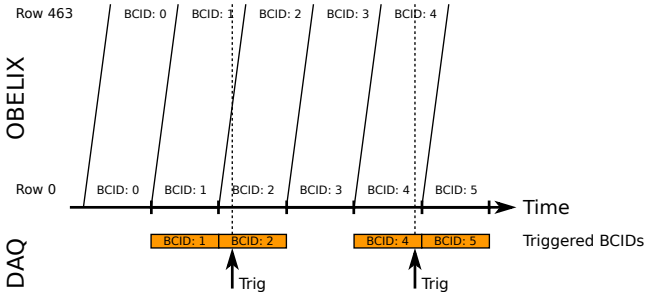
Floorplan (4x4 Version)



Power simulation



Timewalk and BCID Delay



- The plan is: no further precautions for the chipdesign
- OBELIX can handle triggers on multiple subsequent BCIDs
- The DAQ system automaically can create e.g two triggers for BCID, BCID+1 for the same event
- Easily reconfigurable if e.g. three BCID frames are necessary
- At 30 kHz trigger rate, link speed is not limiting