Development and evaluation of the RD50-MPW chips in the LFoundry 150 nm HV-CMOS process

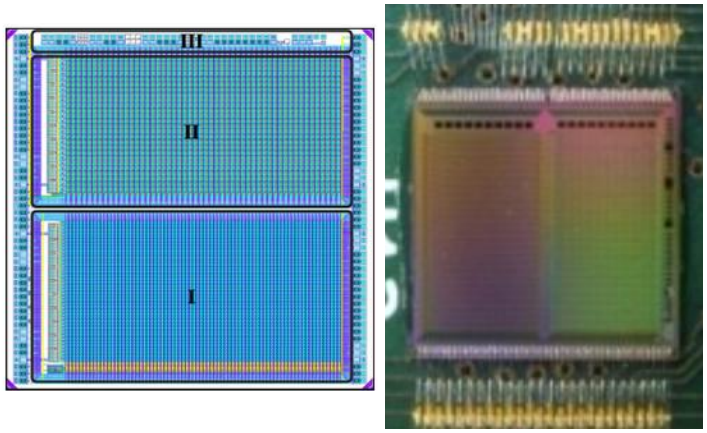
Ricardo Marco Hernández IFIC (CSIC-UV), on behalf of the CERN RD50 CMOS collaboration.

CERN RD50 depleted CMOS activities

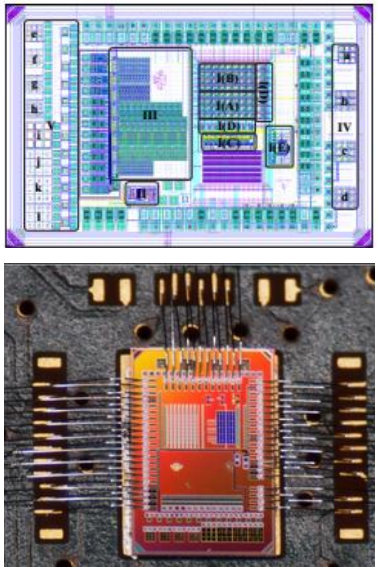
- **CERN RD50 collaboration.**
  - International collaboration with more than 400 members.
  - Aimed at developing and characterising radiation-hard semiconductor devices for high luminosity colliders.
  - R&D carried out in new structures (3D, LGAD, Depleted CMOS, etc.).
- **Depleted CMOS sensors** have a huge potential for future experiments in physics: **high priority in RD50.**
- **RD50 has working group** to develop and study these sensors.
- **CERN-RD50 CMOS working group make efforts in:**
  - TCAD simulations;
  - ASIC design;
  - DAQ development;
  - Chip performance evaluation.
- **Currently involves 17 institutes.**
- **A series of HV-CMOS prototypes have been developed using LFoundry 150 nm HV-CMOS process with large collection electrode.**

RD50 HV-CMOS prototypes

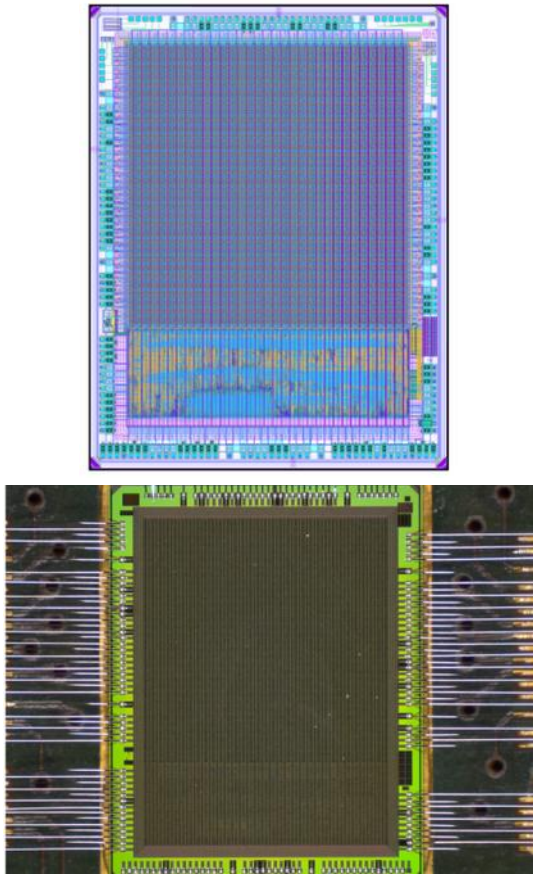
RD50-MPW1
Received in Apr. 2018
5 x 5 mm²



RD50-MPW2
Received in Feb. 2020
3.2 x 2.1 mm²



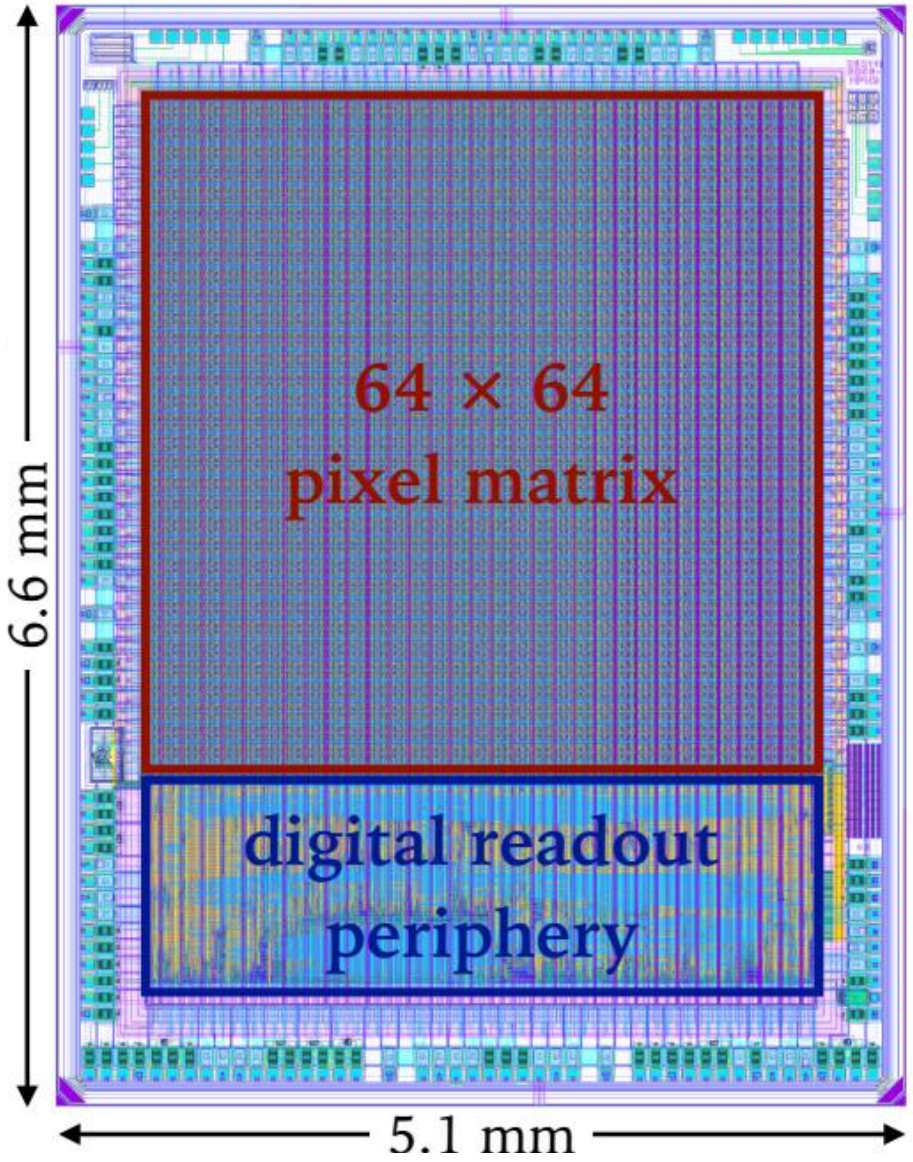
RD50-MPW3
Received in Aug. 2022
6.6 x 5.1 mm²



- **RD50-MPW1:** test the LF150 process.
  - Low V_{BD} (55 V) and high I_{Leak} (~ µA).
  - Crosstalk in some digital readout lines from pixels.
- **RD50-MPW2**: focus on the pixel and analog readout design.
  - Small pixel matrix (8 x 8) without in-pixel digital readout and no digital readout periphery.
  - High V_{BD} (130 V), low I_{Leak} (~ nA) and fast analog front-end.
- **RD50-MPW3**: increase size and include digital readout.
  - Larger pixel matrix (64 x 64) with in-pixel digital readout and advanced peripheral readout.

General details of RD50-MPW3

- **RD50-MPW3** design based on lessons learnt from previous chips.
  - Same chip ring structure for high V_{BD} and low I_{Leak}.
  - Fast analog front-end.
- Mainly composed of a **pixel matrix**, a **digital readout periphery** and **test structures**.
- Wafers with **different resistivity** (1.9 kΩ·cm, 3 kΩ·cm and 10 Ω·cm).
- Several new features in **RD50-MPW3**.
  - **Double-column** architecture.
  - **FE-I3 style digital readout** circuits.
  - **Optimised digital periphery** for **effective chip configuration** and **fast data transmission**.
- **RD50-MPW3** was submitted for fabrication in Dec. 2021 and received in Aug. 2022.



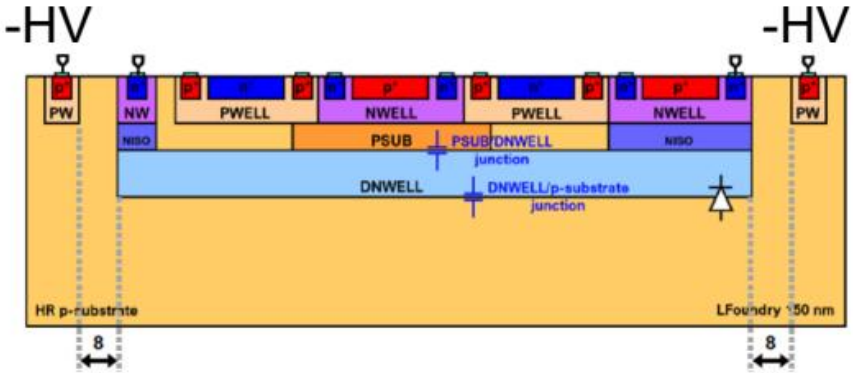
RD50-MPW3 floorplan

RD50-MPW3 pixel

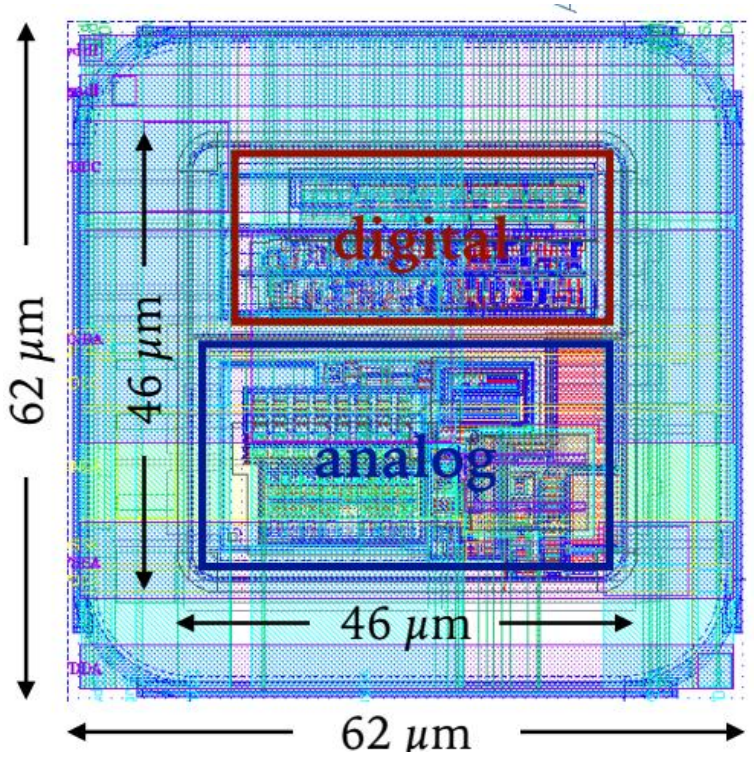
- **Large collection electrode** pixel.
- **High voltage** applied **from top side**.
- **Analog and digital electronics** included **inside each pixel** (55% pixel area).
- **Analog and digital circuits** placed into **separate deep p-wells** and have **different power lines** to **minimise crosstalk noise**.
- **Analog front-end** from **RD50-MPW2** (CSA + comparator).
- **Digital readout** with **double column drain readout** and **rolling shutter**.
  - **Time of arrival** and **time over threshold** are recorded (8-bit time stamps) + **pixel address** (8-bit).

Pixel size	62 μm × 62 μm
Cd	~ 250 fF
Power	22 μW/pixel (VDD = 1.8 V)
Gain	230 mV (for 5 ke$^-$)
ToT	55 ns (for 5 ke$^-$)
ENC	120 e$^-$
Time walk	9 ns

RD50-MPW3 pixel parameters from simulation



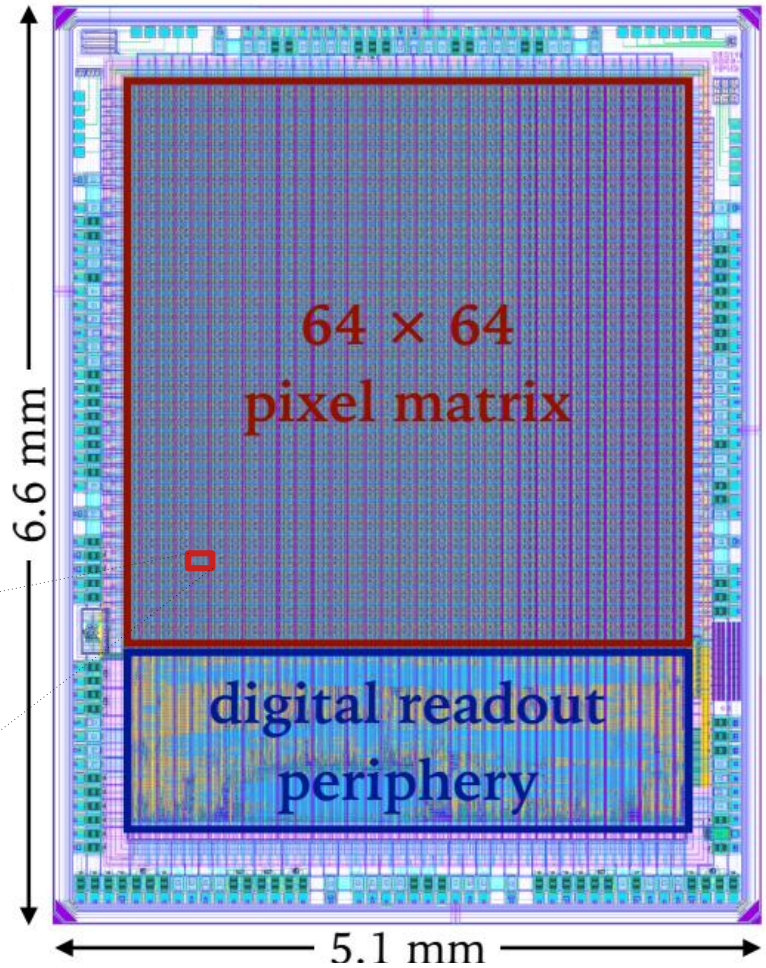
RD50-MPW3 pixel cross section

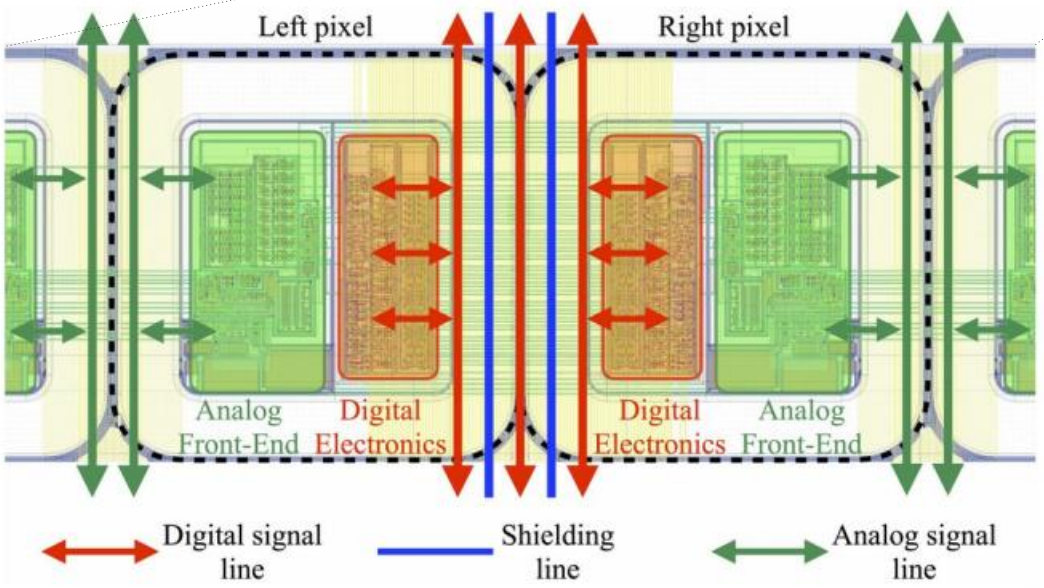


RD50-MPW3 pixel floorplan

RD50-MPW3 pixel matrix

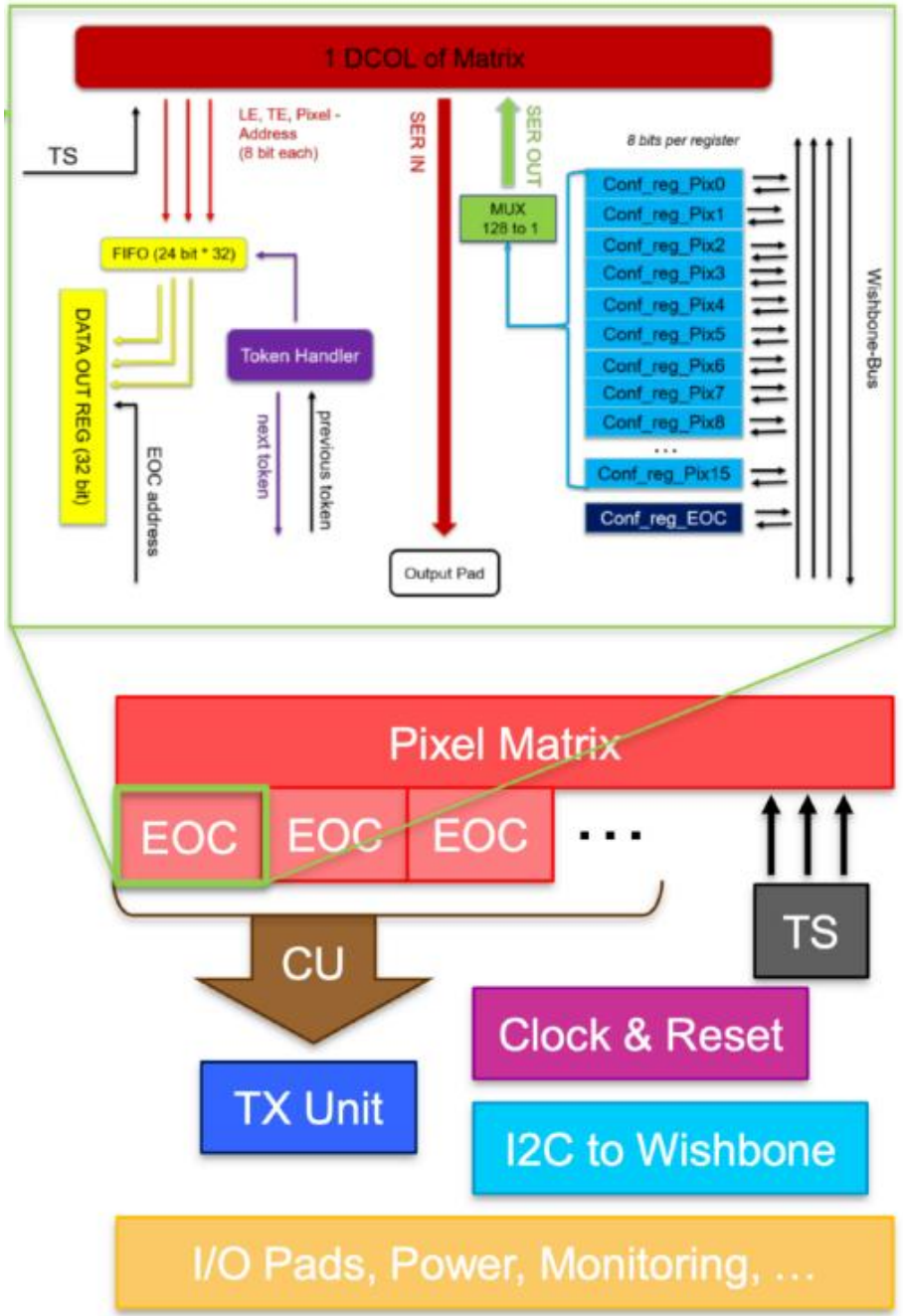
- **64 columns** organised into **32 double columns**.
- **Digital signal lines** placed in the **middle of each column**.
- **Analog lines** placed **between double columns**.
- **Shielding lines (grounded)** inserted **between digital lines** to **minimise coupling**.
- **Power grid** used to **minimise IR voltage drop**.





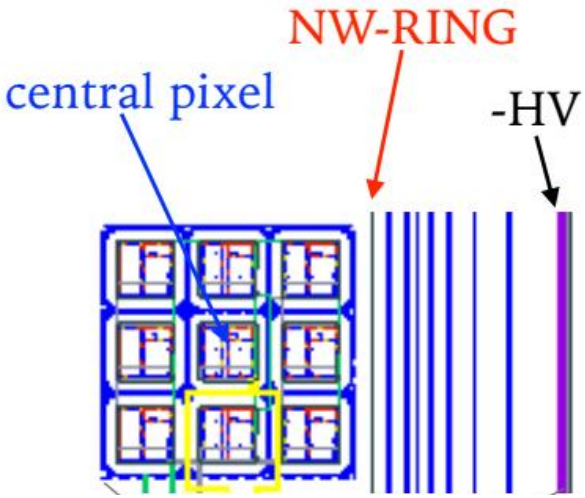
RD50-MPW3 readout periphery

- **One End-Of-Column (EOC)** per **double coulmn (DCOL)**.
  - Configuration of pixels.
  - Pixel data readout + 32 word deep buffer.
- **Transmission unit (TX unit)** for **data transmission**.
  - 128 words deep buffer (FIFO).
  - Framing and encoding (Aurora 8b-10b).
  - Serialisation at 640 MHz.
- **Control unit (CU)** for **reading out EOC buffers**.
  - Controls data propagation from EOCs to TX Unit.
- **Global timestamp (TS) generator.**
  - 8-bit, running at 40 MHz.
  - Gray-encoded to minimise activity on bus.
- **Clock and reset generator.**
  - Dividing 640 MHz clock into a 40 MHz clock.
  - Clock multiplexer for optional external 40 MHz clock.
  - External reset synchronisation with clock.
- **I2C to Wishbone module.**
  - Converts external I2C signals to internal wishbone control signals.

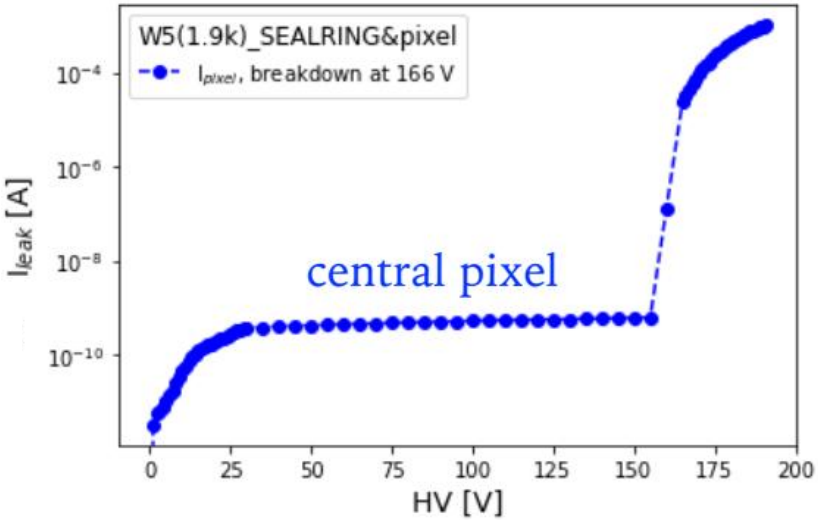


RD50-MPW3 initial IV measurements

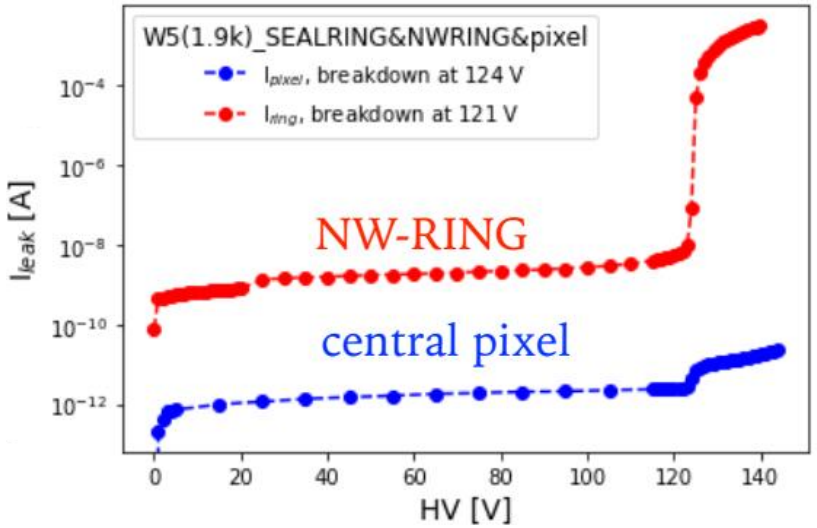
- **Dedicated test structures** to **measure leakage currents** of **central pixel** and **ring**.
- **Only central pixel biased**: leakage current **~ nA** and breakdown voltage **~ 160 V**.
- **NW-Ring also biased**:
  - **Most leakage current collected** by the **NW-Ring**.
  - **NW-Ring** leakage current **~ nA** and breakdown voltage **~ 120 V**.
  - **Pixel** leakage current **~ pA** and breakdown voltage **> 120 V**.



Dedicated test structures



I-V curve (central pixel biased)

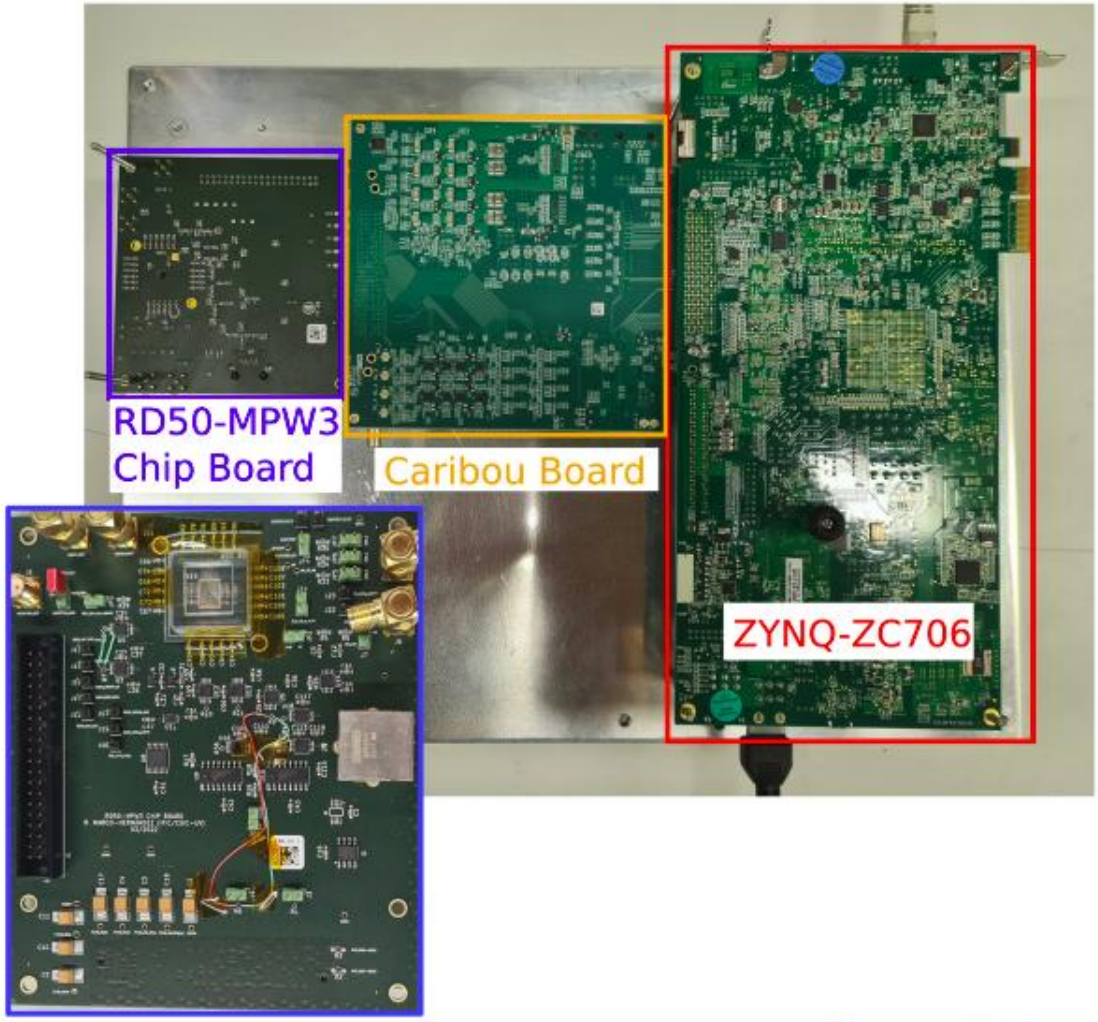


I-V curve (central pixel and NW-ring biased)

From Zhang, 41st RD50 Workshop, 2022.

DAQ system for RD50-MPW3

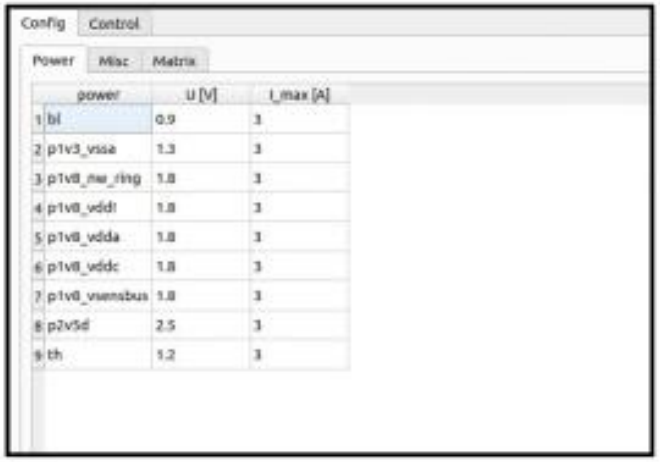
- **Based on Caribou DAQ** system.
- **Xilinx Zynq-ZC706 board** with **Yocto based linux**.
- **CaR board**.
- **Custom chip board**.
  - Allows chaining of second chip board for test beam.
  - SMA connectors to probe analog outputs from RD50-MPW3.



DAQ software for RD50-MPW3

- **Caribou firmware customised** for **RD50-MPW3**.
- **Software based on Peary** from **Caribou**. **Custom GUI.**
- **Control tab.**
  - DAQ configuration.
  - Chip configuration.
  - Execute commands to run the chip.
- **Matrix configuration tab.**
  - Select pixels for configuration.
- **Power tab.**
  - Set bias and supply voltages.

Control tab

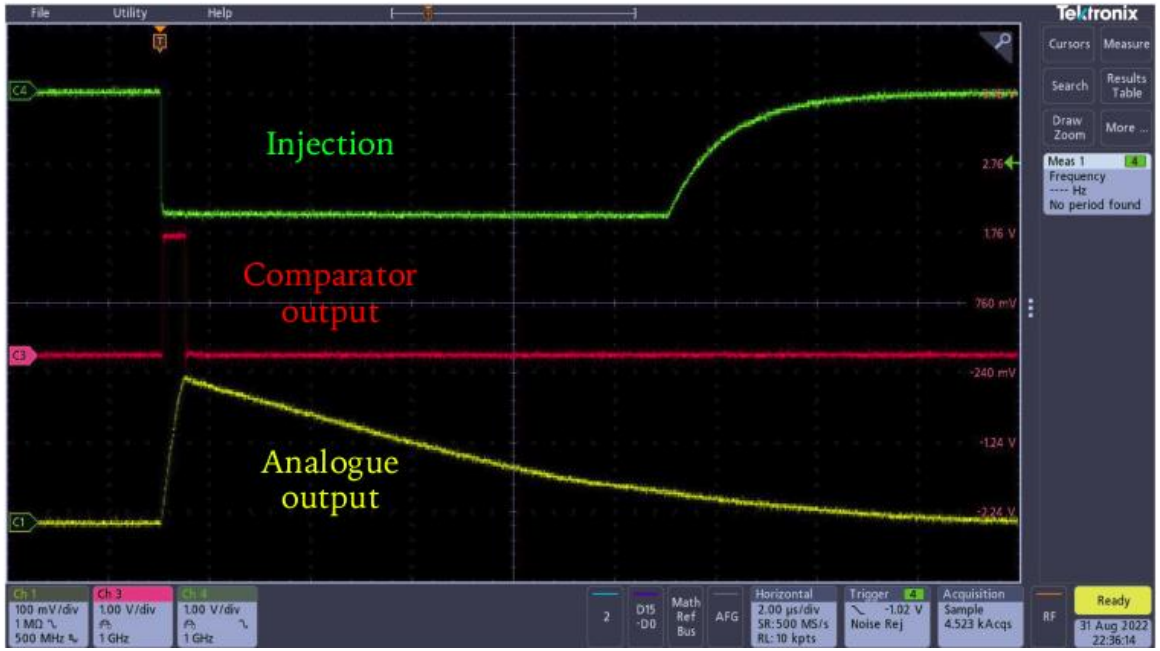


Power tab

Matrix configuration tab

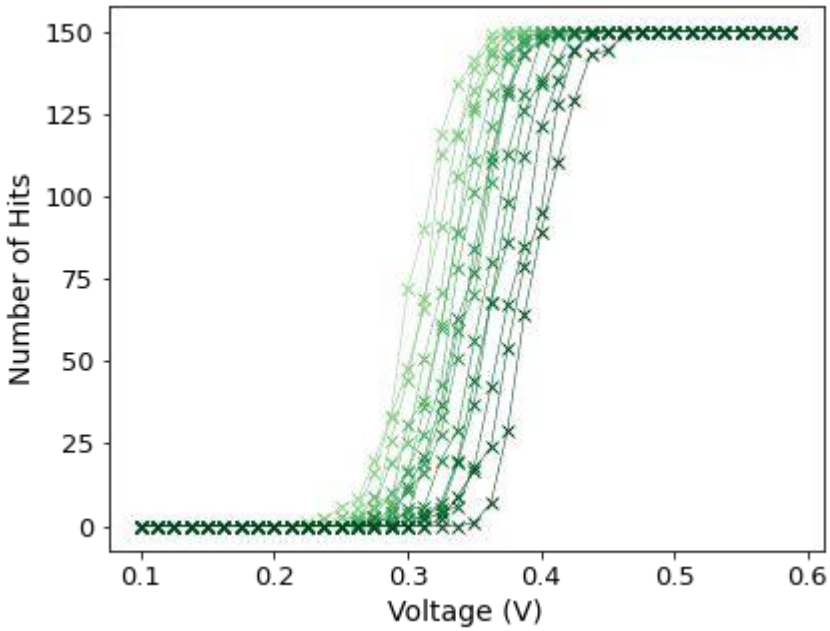
RD50-MPW3 first response

- Send **injection signal** into **pixels**.
- **Chip, DAQ** and **GUI** are **functioning**.
- **S-curve** for **different pixels as expected**.



Pixel amplifier and comparator output signals when a pulse is injected to the pixel.

From Zhang, 41st RD50 Workshop, 2022.

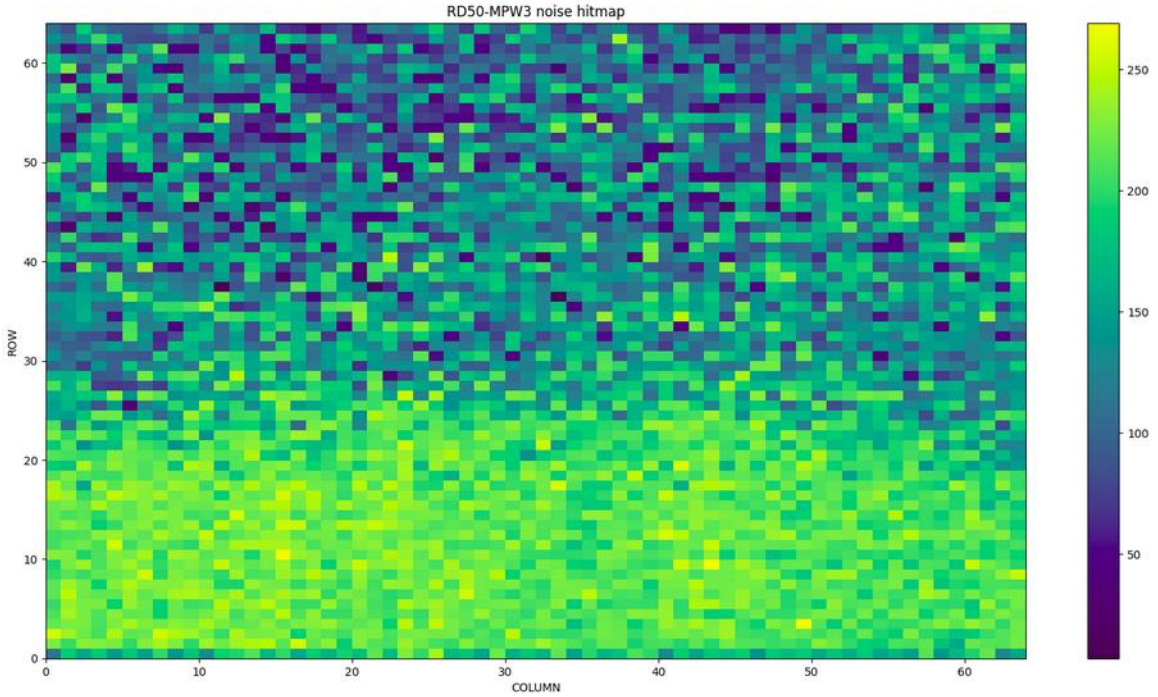


S-curve for one pixel (150 hits per point). Threshold varied with trimdac (darker curve corresponds to higher threshold).

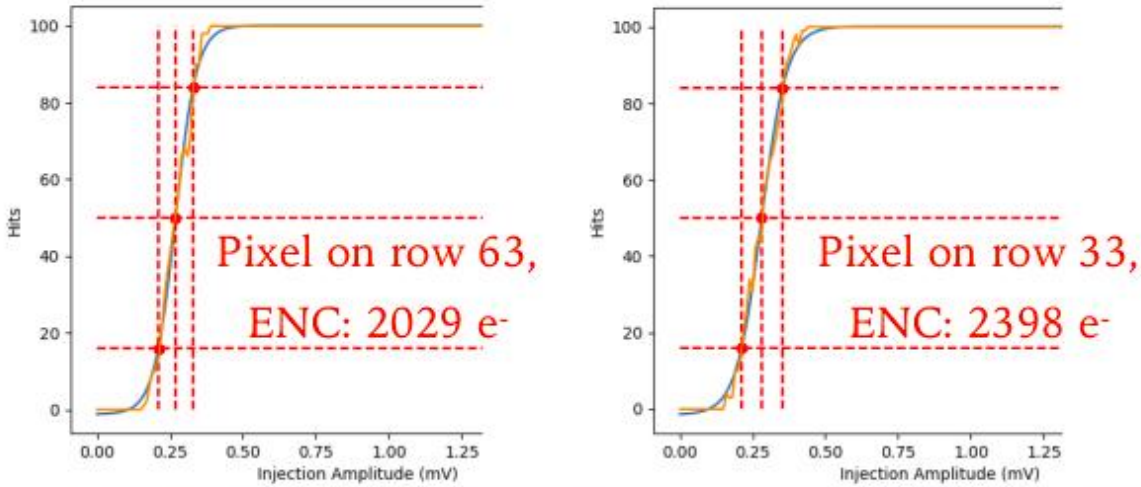
From Sieberer, Zhang, TWEPP, 2022.

RD50-MPW3 noise hitmap

- **Pixel matrix hitmap**.
  - No injected signal (**only noise**).
  - Chip default configuration.
  - Threshold 300 mV above baseline (900 mV).
  - Shutter window of 2s.
- **Bottom part of the matrix is noisier**.
  - **Confirmed by S-curves** of **pixels** corresponding to **different rows**.
- **Noise coupling** from **digital periphery**.
  - **Digital ground shared** by **digital periphery** and **digital part of pixels**.
  - **Simulation confirms** that **noise** is **minimised** by **separating digital periphery** and **digital pixel grounds**.



Pixel matrix noise hitmap

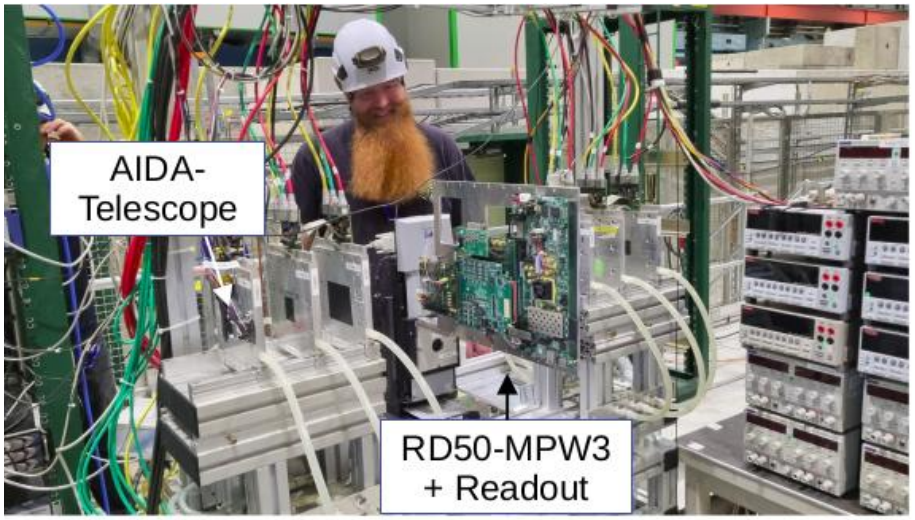


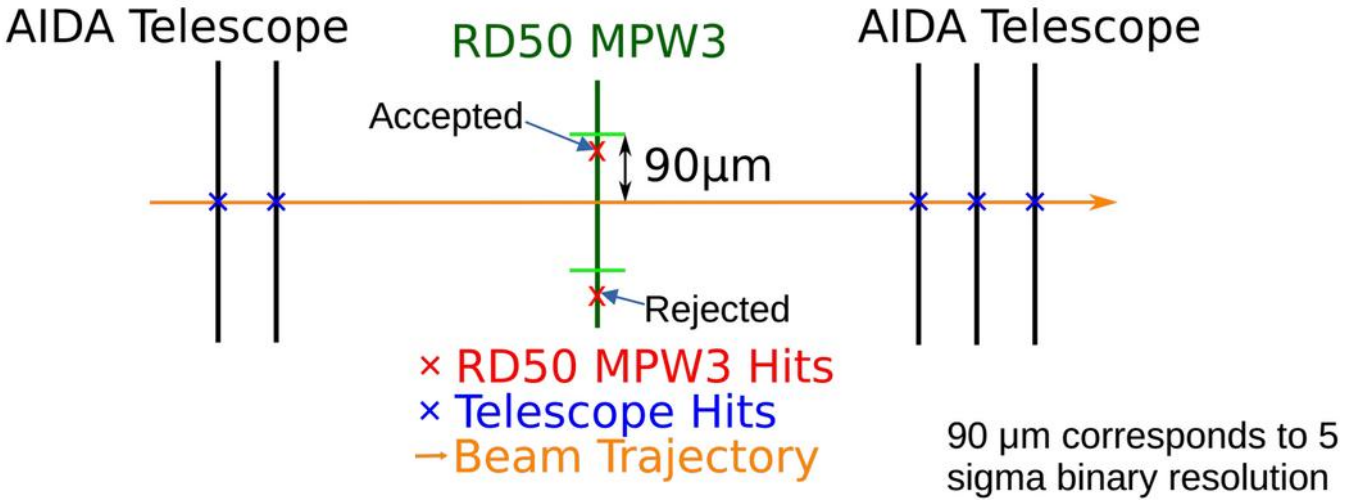
S-curves for pixels on row 63 and 33 for the same column.

From Zhang, 41st RD50 Workshop, 2022.

RD50-MPW3 CERN SPS test beam

- **SPS test beam** week in October 2022.
- Placed within **SPS proton beam line** (H6B-PPE 156, 120 GeV beam).
- **EUDET-type telescope** with 5 **MIMOSA26-planes** used.
- **Synchronised data taking** via **AIDA TLU** using **EUDAQ2**.
- **Analysis** using **Corryvreckan**.



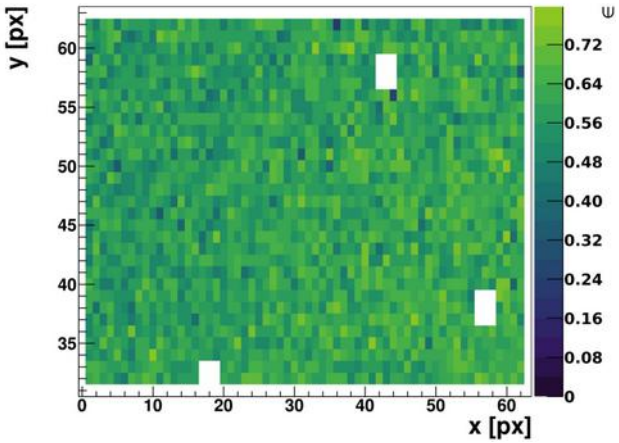


- **Spatial matching**.
  - **AIDA telescope** provides **reference tracks**.
  - **Only accepted hits matched** to **tracks** are **shown**.
  - **Interpolated track position** used for **in-pixel measurements**.

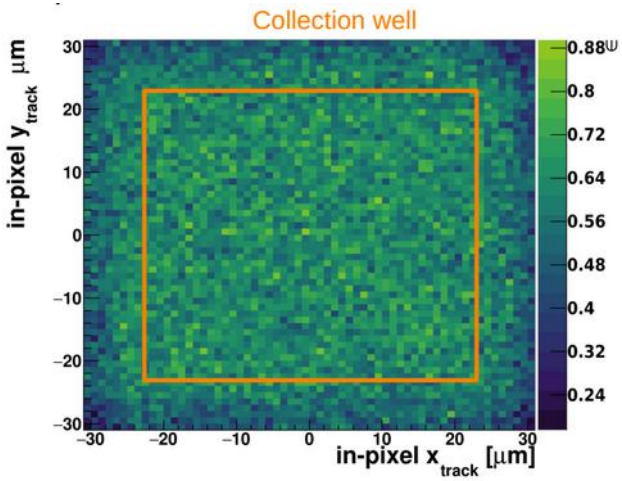
From Kraemer, TREDI 2023.

- **Chip and in pixel efficiency.**
  - **Efficiency** based on **ratio of matched to total tracks**.
  - **Average efficiency** of **active sensor of 60%**.
  - **Efficiency reduced** by **high threshold set** (1/3 MIP MPV for 190 µm depletion depth).
- **Spatial resolution.**
  - **Residual** between i**nterpolated track position** and **measured pixel hit location**.
  - **Almost binary distribution** due to **low double hit clusters**.

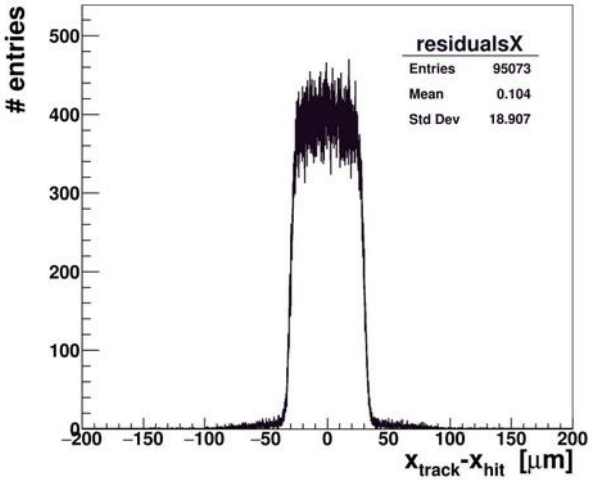
$$\sigma_{\text{meas}} = 18\mu\text{m} \approx \frac{62\mu\text{m}}{\sqrt{12}} = \sigma_{\text{binary}}$$



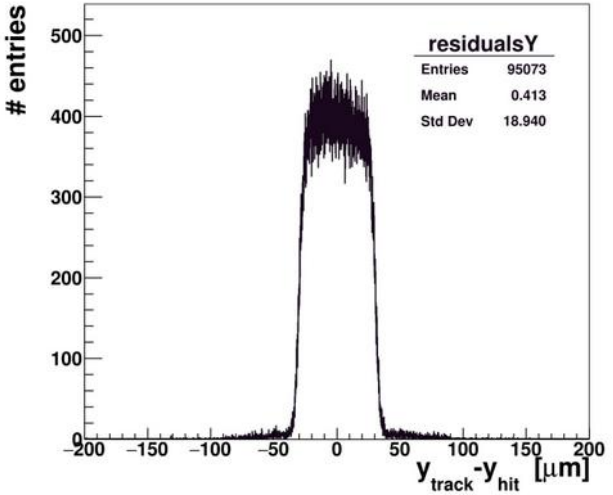
Chip efficiency



In-pixel efficiency



Spatial resolution (residuals in X).



Spatial resolution (residuals in Y).

From Kraemer, TREDI 2023.

RD50-MPW4 submission plans

- **New RD50-MPW4 chip submission** planned for **May 2023**.
- **Fix issues** observed in **RD50-MPW3**.
  - Interface between matrix and periphery: longer pull-down time to run time-stamp without discharging effects.
  - Easy generation of global time-stamp: 64-bit counter in the chip.
  - High noise in lower half of matrix: separate digital pixel matrix and digital periphery power/ground domains.
- **Improve breakdown voltage** and **radiation tolerance**.
  - Optimised multi-ring guard structure around chip: as in current test structures.
  - Better HV distribution to pixels: backside biasing (backside processing).
- **Same pixel matrix size** and **similar chip size** (5.4 mm x 6.4 mm).
- **Three wafers** with **substrate resitivity** of **3 kΩ·cm** (also standard resistivity of 10 Ω·cm).

Summary and outlook

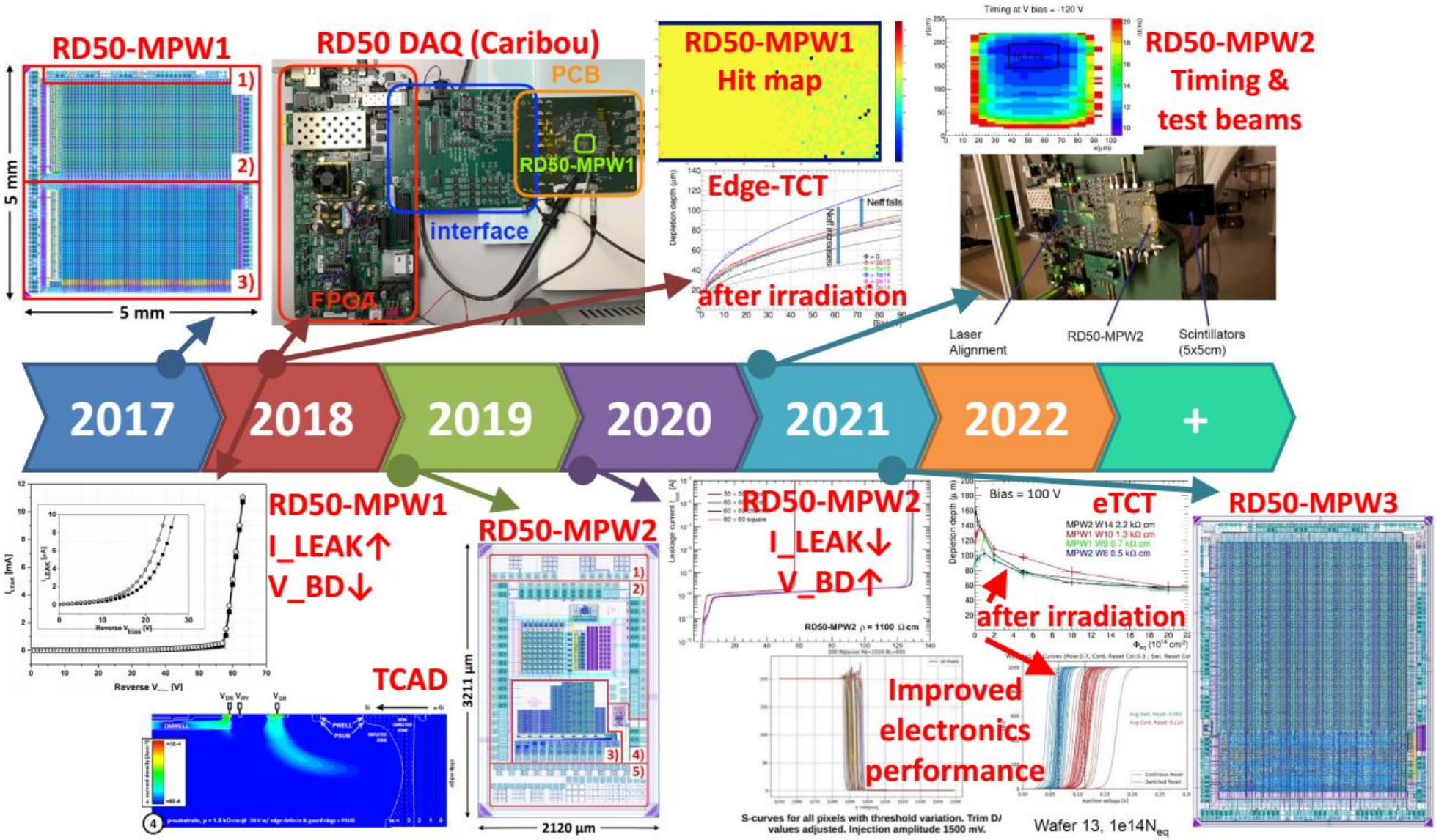
- **Summary.**
  - **RD50 CMOS activities** on **monolithic CMOS devices** for **very high luminosity colliders progressing** at **good pace**.
  - **Three RD50 HV-CMOS prototypes developed** so far.
  - **RD50-MPW3 operation tested successfully** for **non-irradiated devices**.
  - **Test beam** with **RD50-MPW3** carried out at **CERN SPS** showed **promising results**.
  - **Several RD50-MPW3 issues identified** and **well understood**.
- **Outlook.**
  - **New RD50-MPW4 submission** in **May 2023.**
  - **Continue RD50-MPW3 characterisation** with **non-irradiated** and **irradiated devices.**
  - **New RD50-MPW3 test beam** campaign at **DESY** in **July 2023.**

Development and evaluation of the RD50-MPW chips in the LFoundry 150 nm HV-CMOS process

Ricardo Marco Hernández IFIC (CSIC-UV), on behalf of the CERN RD50 CMOS collaboration.

Backup slides

RD50 CMOS timeline

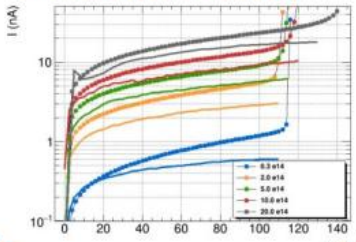


From Vilella, 1st AIDAinnova meeting, 2022.

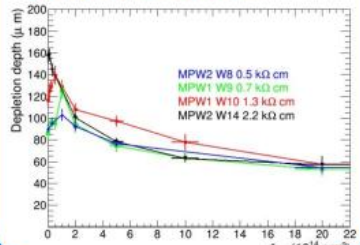
RD50-MPW2 measurements summary

- Prototype HV-CMOS sensor with test structures and a small active pixel matrix, fabricated in high resistivity substrates in a Multi-Project Wafer submission with LFoundry.
  - Aim to study and improve time resolution and radiation tolerance with 60 µm x 60 µm pixels
  - Evaluated in the lab before and after neutron irradiation up to 2e15 n_{eq}/cm^2

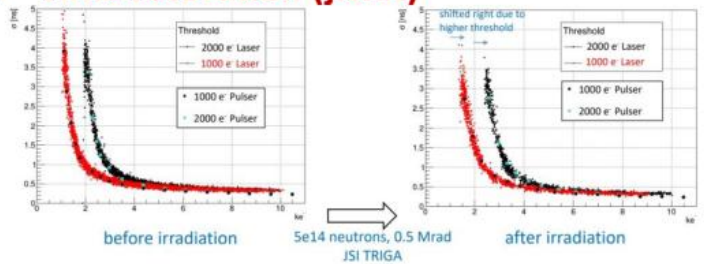
I-V (after 80 mins annealing)



eTCT @ V_HV = 100 V, 2 kΩcm

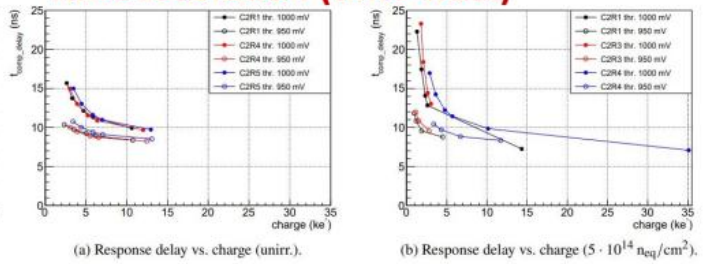


Time resolution (jitter)



Jitter < 160 ps before and after irradiation to 5e14

Time resolution (time-walk)



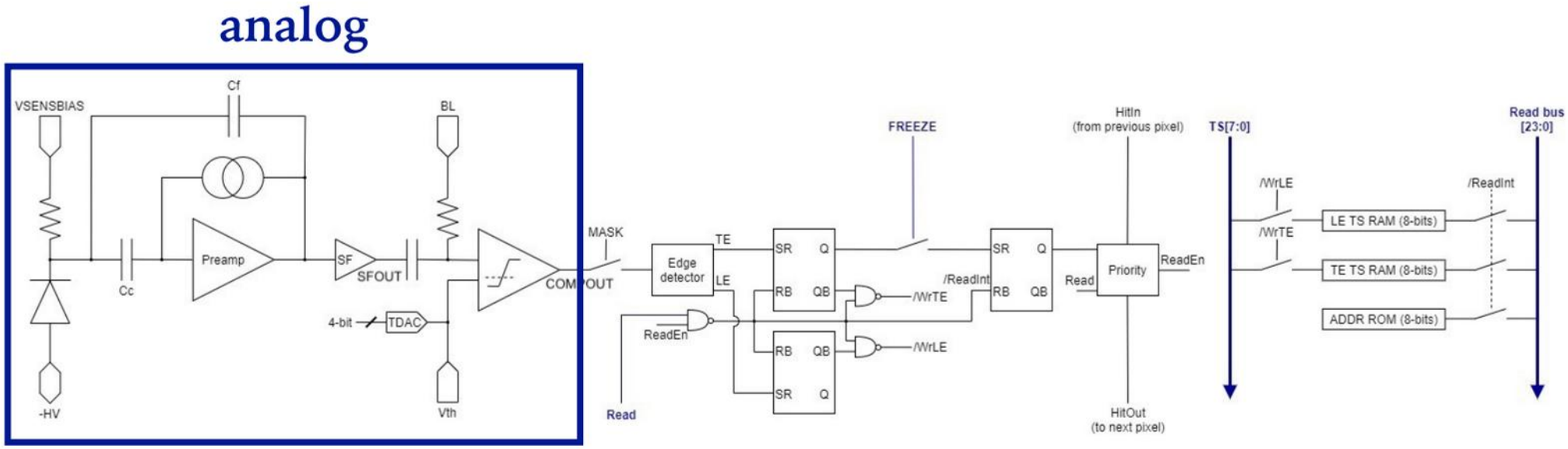
(a) Response delay vs. charge (unirr.). (b) Response delay vs. charge ($5 \cdot 10^{14}$ n_{eq}/cm^2).

Time-walk < 10 ns before and after irradiation to 5e14 @ > 2ke⁻ collected

From Vilella, 41st RD50 Workshop 2023.

RD50-MPW3 pixel: analog front-end

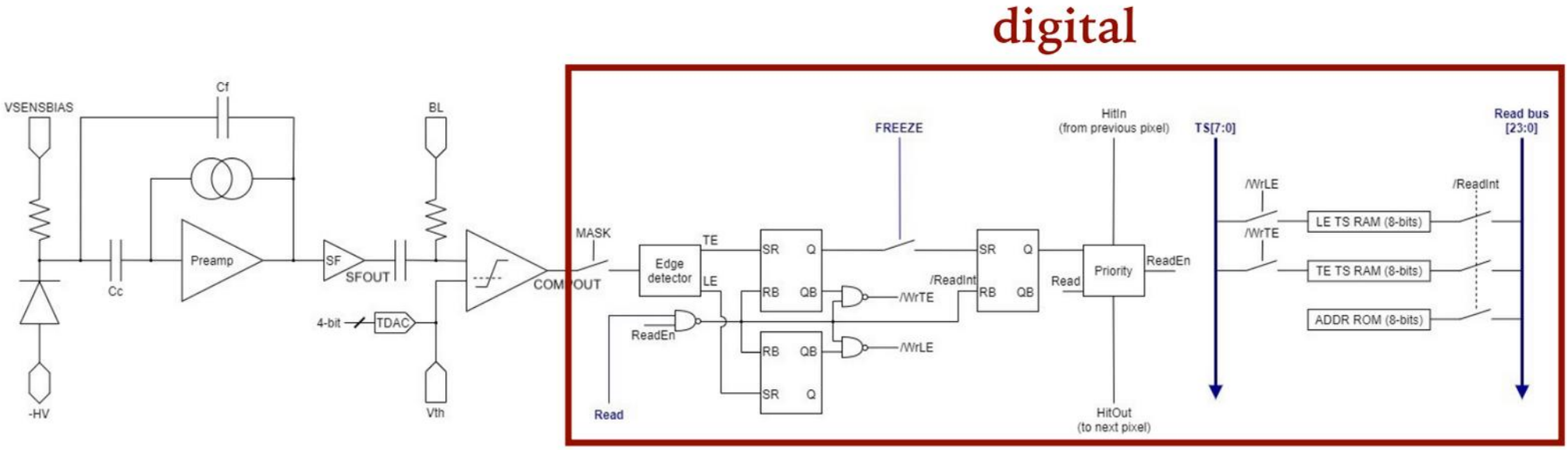
- **Analog front-end** from **RD50-MPW2 pixels**: **tested design** with **good performance**.
  - **Continuous-reset charge sensitive amplifier** with **high processing speed**.
  - Each pixel has a **comparator to digitise** its **analog signal**.
  - A **4-bit trim-DAC** inside each pixel **tunes comparator threshold**.
  - **Injection circuit** included to characterise pixel performance.
  - **Analog pixel outputs routed** to **external pads** (SFOUT and COMPOUT).



From Zhang, 40th RD50 Workshop, 2022.

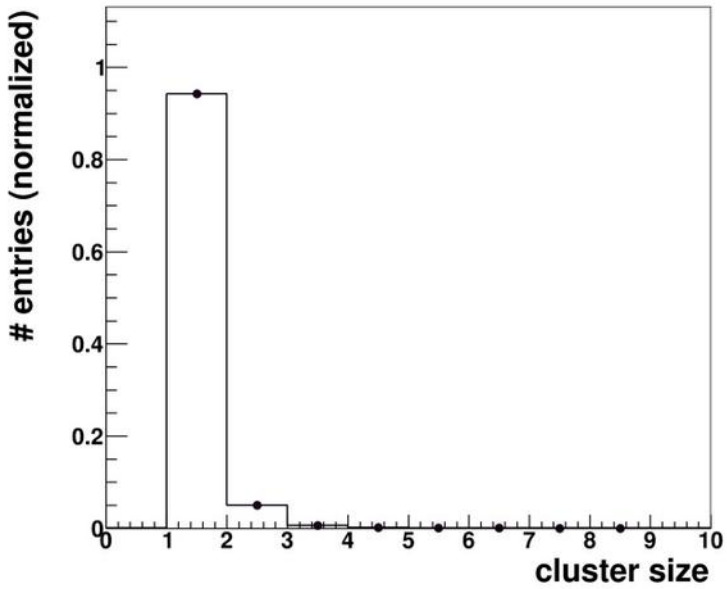
RD50-MPW3 pixel: digital front-end

- **Digitial readout** based on **coulmn drain architecture** from RD50-MPW1 (highly improved).
  - **8-bit time stamp (40 MHz)** sent to all pixels.
  - **Time stamps** of the **rising and trailing edges** of the **comparator output** recorded to measure **Time of Arrival (ToA)** and **Time over Threshold (ToT)**.
  - **Time stamps stored** in two **8-bit RAMs**, which are **sent out** together with an **8-bit pixel address** via a **shared readout bus**.
  - **Full custom design** to **minimise area**.

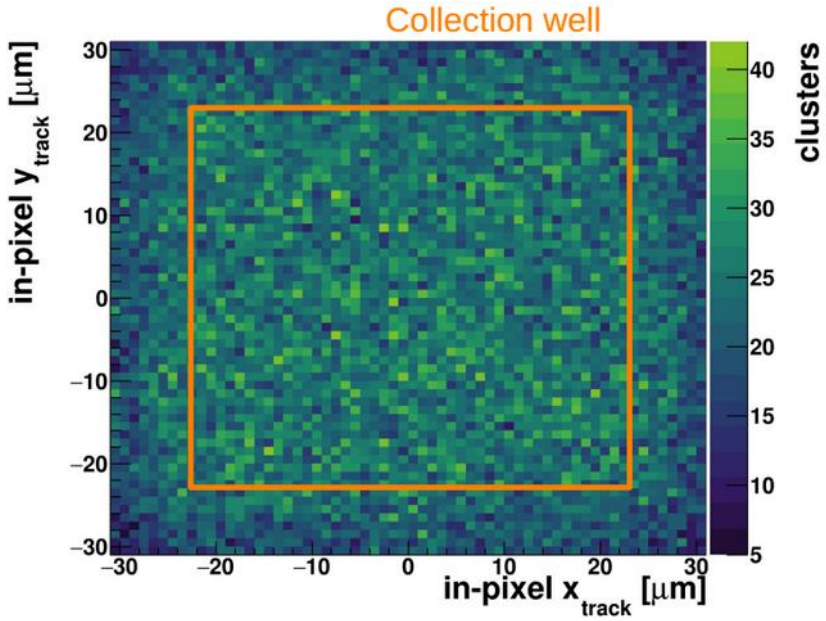


From Zhang, 40th RD50 Workshop, 2022.

- **Cluster size distribution.**
  - **Majority** of **1-hit clusters** (94%).
  - **Homogeneous distribution** of **1-hit clusters within pixel**.
  - **Reduction** towards **the edges** due to **charge sharing.**



Chip cluster size



In-pixel cluster size

From Kraemer, TREDI 2023.