ETH zürich

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DMAPS activities of the PSI High Energy Physics Group

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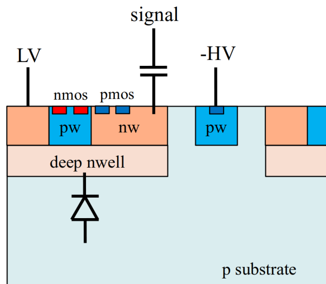
Motivation

- The PSI High Energy Physics group in collaboration with ETHZ has a generic R&D program for DMAPS since 2019
- Several technologies are being evaluated for potential use in in-house experiments (μSR, μEDM)
- Goal: radiation hard detectors featuring timing
- Aiming for
  - Spatial resolution of O(10 µm)
  - Sub-nanosecond timing resolution

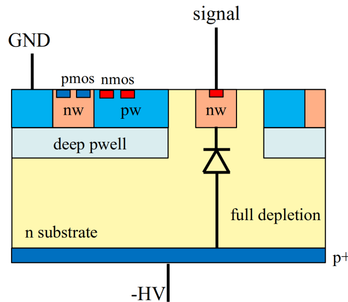
DMAPS Types (1)



- **Large Fill Factor (area of collection electrode)**
- Large sensor capacitance: higher noise, needs more power
- slower signals: ⊖ for timing
- shorter drift paths: ⊕ for timing, ⊕ for radiation hardness
- Crosstalk issues from electronics into collection node

TSI, AMS, LFoundry 150

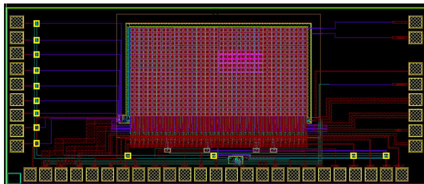
DMAPS Types (2)



- **Small Fill Factor (area of collection electrode)**
- Small sensor capacitance: higher noise, needs less power
- faster and larger signals: ⊕ ⊕ for timing
- longer drift paths: ⊖ for timing, ⊖ for radiation hardness
- Need to find new ways to shape fields

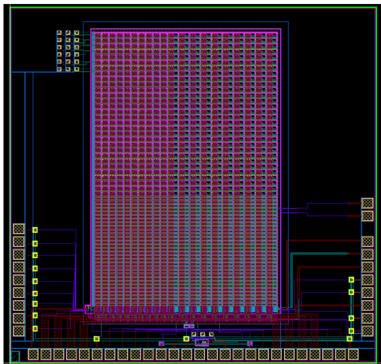
LFoundry 110 nm, ESPROS, TowerJazz

First PSI TSI MAPS Chip



- Standard low resistivity wafers → Only very thin depleted region
- 20 by 40 pixels of 50 by 50 μm^2
- Different preamplifier designs
- Different biasing schemes (resistor / forward biased diode)
- Readout similar to ROC4Sens (serial readout with shift registers, no zero suppression)
- Works well, registered Strontium hits, choosing diode bias.

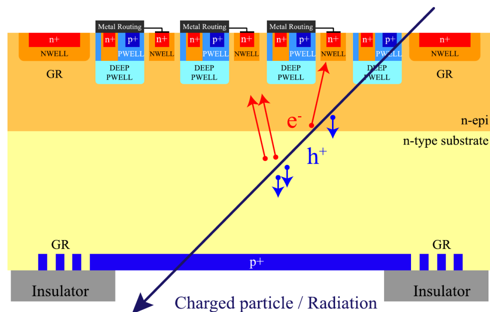
Second PSI TSI MAPS Chip



- 200 Ωcm and 5 kΩcm Wafers
- 20 by 20 pixels of 50 by 150 μm^2 and 75 by 150 μm^2
- Now including a trimmable comparator and sample and hold circuit
- Received in April 2023, test beam planned for June 2023
- Submissions in collaboration with KIT / Heidelberg University

Process Overview: Modified LFoundry 110 nm Process

N-type substrate wafers



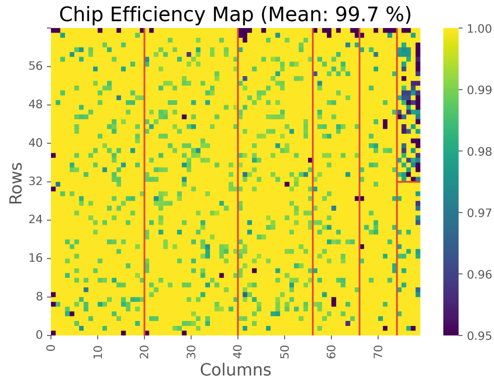
- All sensing structures designed by ARCADIA
- Small electrodes with small capacitance
- The wafers are backside processed to have guard rings and backside metal contact
- Depletion from the backside
- Active thicknesses of 50, 100, 200 µm

The development of the process modification and sensor nodes has been performed in the framework of the INFN CSN5 Call ARCADIA

LFoundry 110 nm: Monolithic Timing Chip (MoTiC)

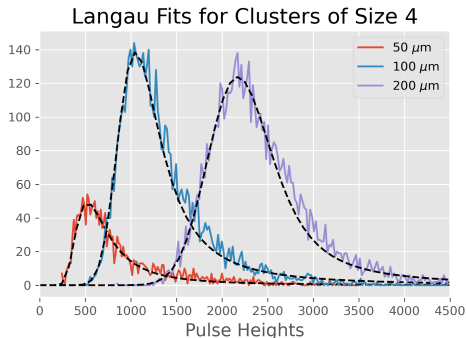
- Manufactured in a modified 110 nm CMOS process
- Pixel pitch: 50 x 50 μm^2
- 80 columns by 64 rows (5120 pixels)
- Full frame readout
- In-pixel discriminators and TDC shared by 4 pixels
- 7 pixel flavours with different preamplifier designs
- Sister chip with varying sensor geometries and test structures (MoTiC B)
- Test beam in Nov 2022

Efficiency Map



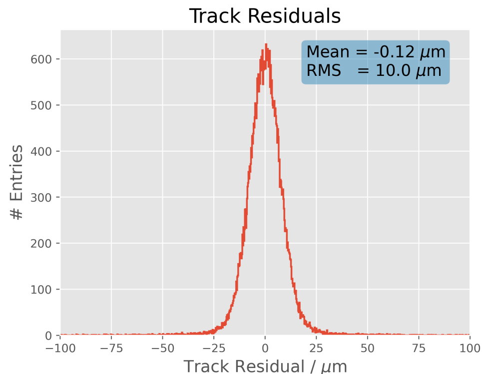
- Efficiency across full matrix.
- Red borders show different preamplifier designs.
- Top right flavour has a larger feedback capacitance leading to a lower gain.

Charge Distribution of Associated Clusters



- Charge distribution of associated clusters.
- Samples of 50, 100, 200 μm active thickness.
- MPV of roughly 500, 1000, 200 ADC counts.
- MPV proportional to active thickness.

Spatial Resolution at Vertical Incidence



- Better than binary resolution ($\sim$ 14.4 µm)
- This is due to significant charge sharing even at vertical incidence.

Conclusion and Outlook

- First prototypes in TSI and LFoundry 110 nm CMOS processes have been designed and manufactured.
- First TSI chip main functionality proven in lab.
- First LFoundry 110 nm chip functionality verified in test beam.
- High efficiency (99.7 %) and good spatial resolution (10 µm) measured in test beam
- TDC verified standalone, but not in the matrix.
- Second versions of both chips delivered in April 2023 to be investigated in test beams.