AIDA innova

2nd annual meeting
24-26 April 2023
Valencia

WP5: Activities on TPSCo 65 nm process

Report by Jerome Baudot
for a large community

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- → Interest for sensors in a 65 nm process
- → 1st submission MLR1 findings
- → Contents of ER1
- → Plan for ER2

65 nm & requirements from WP 5

Slightly modified introductory slide from kick-off meeting (April 2021)

- **Sensor spatial resolution**
  - Key requirement for Higgs factories: $\sigma_{sp} \lesssim 3$ µm
  - ALICE-ITS3 ~5 µm, Belle II <15 µm, trackers >10µm

⇐ critical benefit of small feature size in 65nm for task 5.2

- **Detection layer with material budget: 0.05 to 0.15 % X_0**
  - Achieved through large stitched & curved sensors
    - Key requirement for ALICE-ITS3, strong interest for Higgs factories
  - Low power <<100 mW/cm^2, compatible with air-cooling
    - Important for Higgs factories & ALICE-ITS3

⇐ possible with other techno BUT attractive in 65nm due to 12" wafer size

⇐ benefit of low supply voltage in 65nm, critical for task 5.2

- **Hit rate and time resolution (highly dependent on experiment)**
  - Few 10 MHz/cm^2/s for Higgs-factories
  - > 100 MHz/cm^2/s for Belle II and some trackers
  - Time resolution ~ns for CLIC and some trackers
  - Specific for PID or 4D tracking: time resolution in ~10 or ~100ps range

⇖

⇐ requires new readout architectures, critical for both tasks 5.2+5.3

⇐ benefit of thin sensitive layer in 65nm, critical for task 5.3

- **Radiation tolerance to NIEL fluence**
  - Up to 10^{12} $n_{eq(1MeV)}$/cm^2 for task 5.2
  - Mimimum 10^{15} $n_{eq(1MeV)}$/cm^2 and beyond for task 5.3

⇐ 65nm tolerance to be checked, critical for task 5.3

A large effort, including AIDAinnova partners

Many contributors

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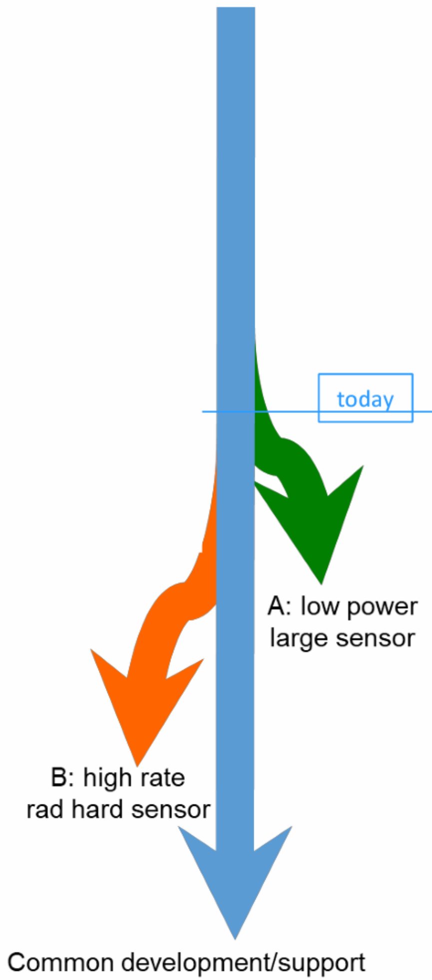
Timeline



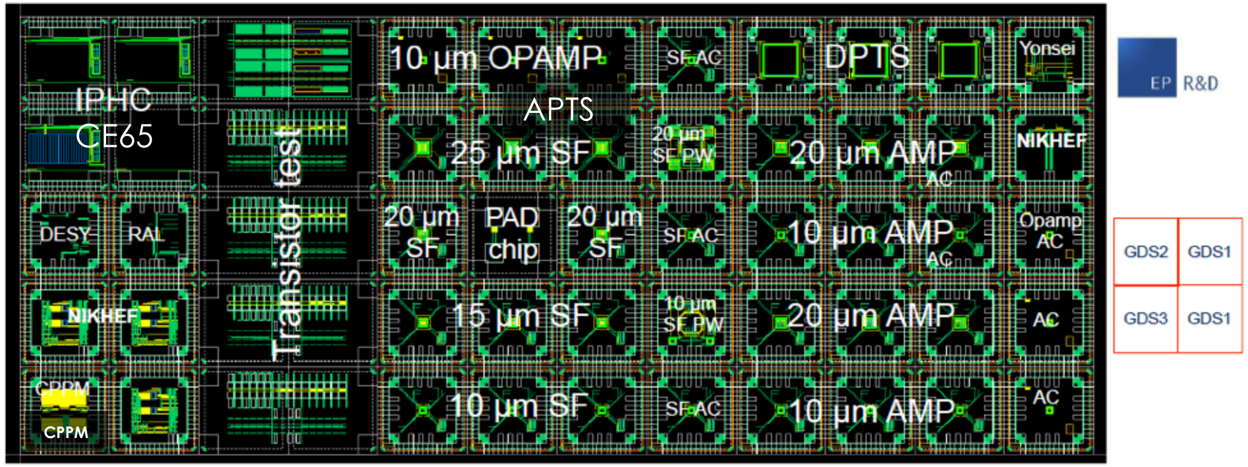
Time	*Scope*	*Submissions TPSCo ISC 65nm*
Phase I 2020-21	Technology Test structures Collaboration Framework	**MLR1** Dec20
Phase II 2021-22	Technology iterations Test demonstrators Dissemination	**ER1** Nov22
Phase III 2023-24	Technology iterations Full chips	**ER2** Exp. 2024
		MLR2

⇒Well within AIDAinnova
ALICE-ITS3 centered

⇒Preparation within AIDAinnova
Open for new R&D tracks

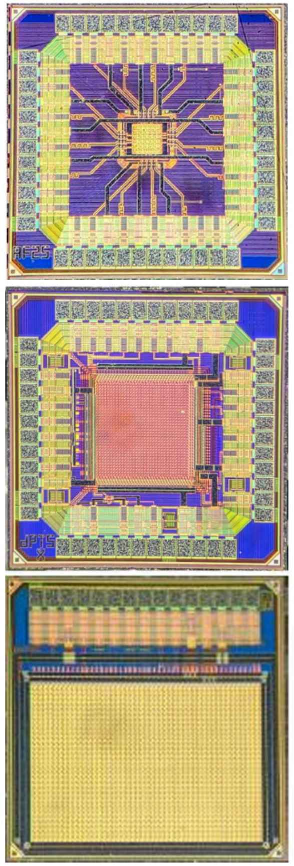
Reminder on 1st submission

- Multi-Layer Reticule (MLR1)
  - 5 metal layers, HR thin (~10µm) epi layer



- IPHC: rolling shutter larger matrices, DESY: pixel test structure (using charge amplifier with Krummenacher feedback, RAL: LVDS/CML receiver/driver, NIKHEF: bandgap, T-sensor, VCO, CPPM: ring-oscillators, Yonsei: amplifier structures
- CERN { Transistor test structures, analog pixel (4x4 matrix) test matrices in several versions (in collaboration with IPHC with special amplifier), digital pixel test matrix (DPTS) (32x32), pad structure for assembly testing.
- After final GDS placement, GDS1 is instantiated twice.
- Converged with 4 splits of 3 wafers

⇒ Sensors
- 10-25 µm pitch
- APTS = analogue outputs with OpAmp
- DPTS = digital outputs
- CE65 = analogue outputs with DC/AC and no-Amp/Amp



APTS

DPTS

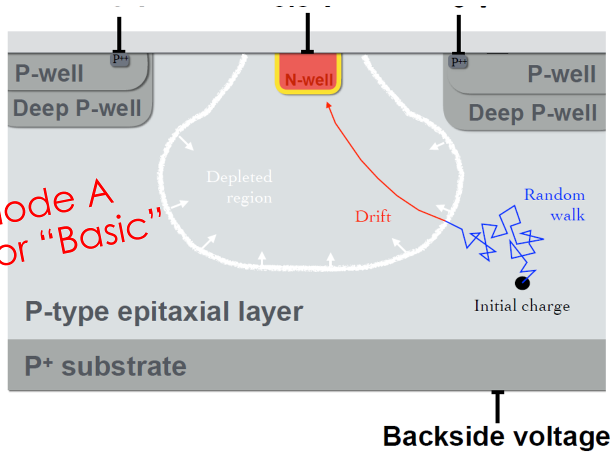
CE65

- Test & Building blocs
  - Transistors: no show stoppers (still some measurements to be done)
  - Ring oscillators: ready for irradiation study
  - DAC, Bandgap, Temp-sensors, VCO: functional, TID/NIEL irradiations & SEE under-study

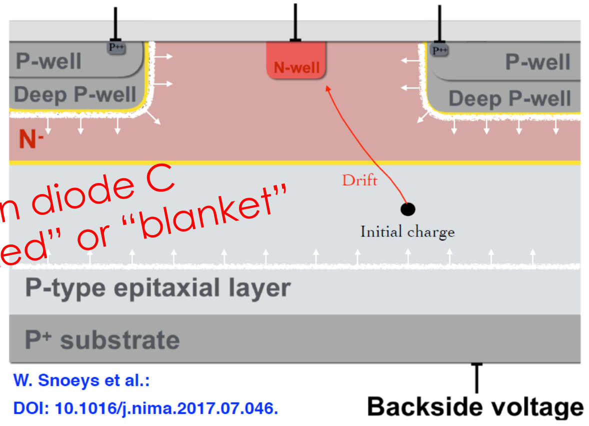
TPSCo 65nm process modification

- <u>4 process splits</u>
  - Doping modifications:
    1. Default process
    2. First intermediate process
    3. Second intermediate process
    4. Optimized process

Collection diode A
"standard" or "Basic"

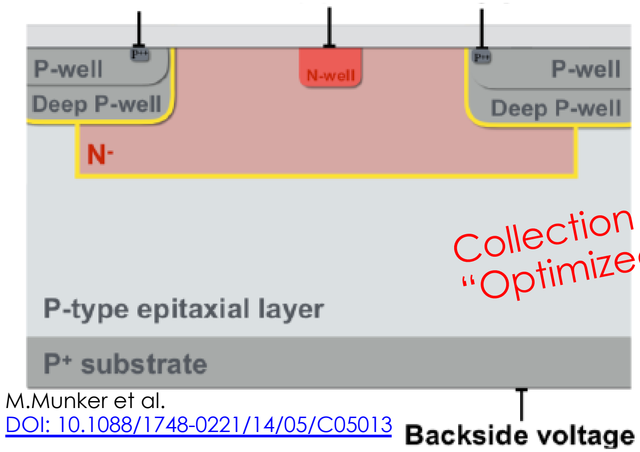


Collection diode C
"Optimized" or "blanket"



W. Snoeys et al.:
DOI: 10.1016/j.nima.2017.07.046.

- <u>3 collection diode structures</u>
  - Following successful modifications in Tower 180 nm
  - Standard => Optimized(gap) structures



Collection diode B
"Optimized-gap" or "gap"

M.Munker et al.
DOI: 10.1088/1748-0221/14/05/C05013

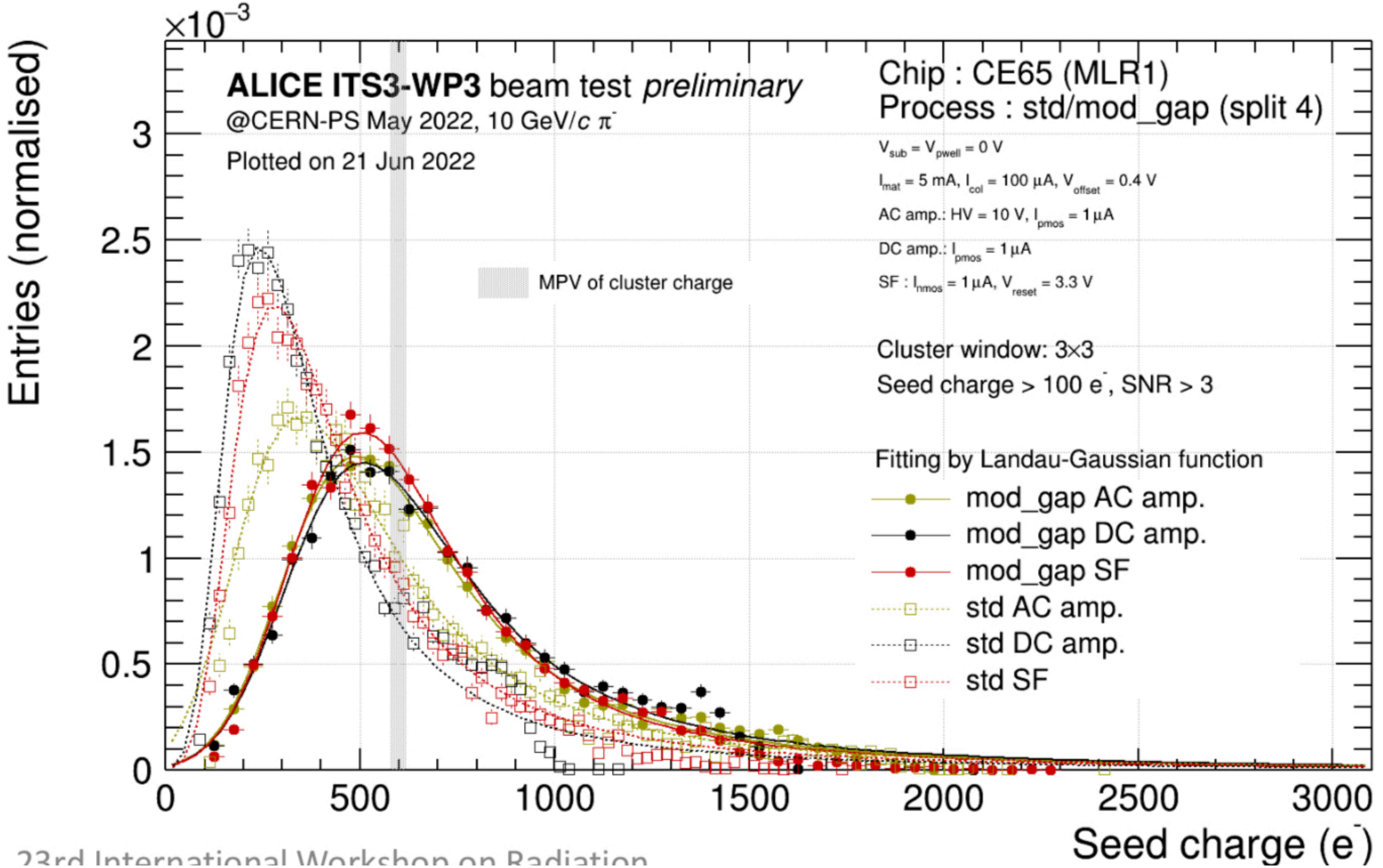
⇒ Both modifications based on TCAD studies
Stll on-going for subsequent submissions

MLR1 findings so far 1/3

- Process modifications successfull / basic detection

S.Senyukov @ IWoRiD2022

- CE-65 (analog) with 15 µm pitch
- Beam test at DESY



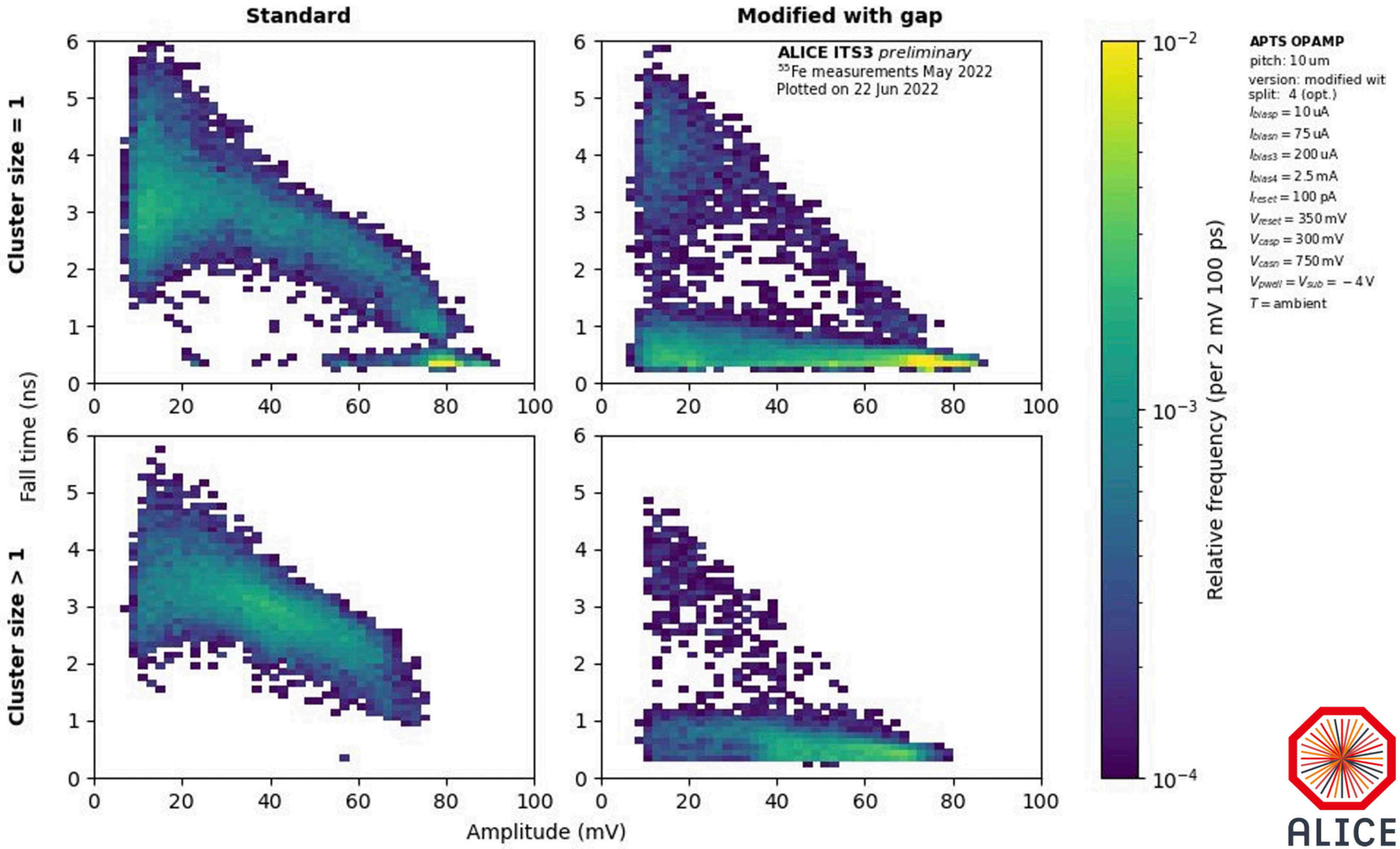
23rd International Workshop on Radiation

MLR1 findings so far 1/3

- Promising timing performance

S.Perciballi @ TREDI2023 https://indi.to/yD2ZF

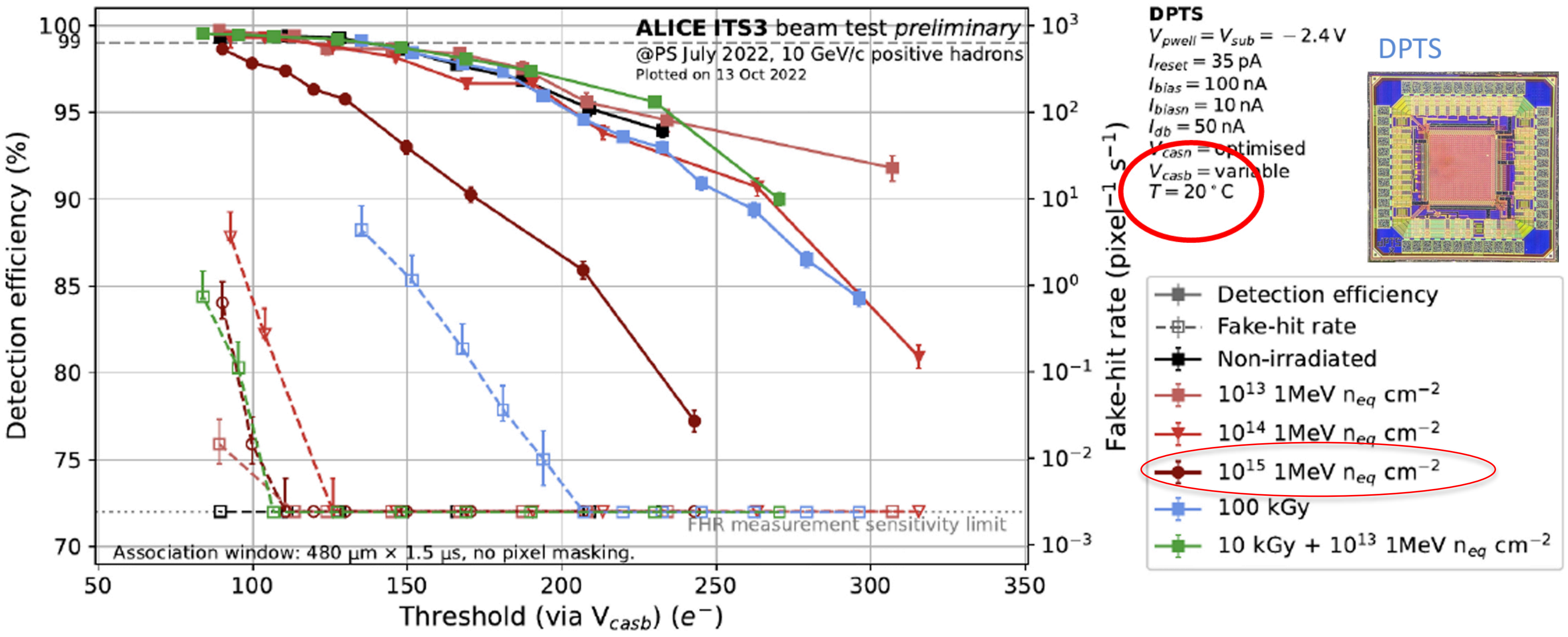
- APTS with OpAmp, 10 µm pitch
- ^{55}Fe illumination
- Note fall time = rising timing since negative signal



MLR1 findings so far 3/3

- Promising radiation tolerance
  - DPTS (digital) with 15 µm pitch
  - Beam test results

S.Perciballi @ TREDI2023 https://indi.to/yD2ZF



DPTS

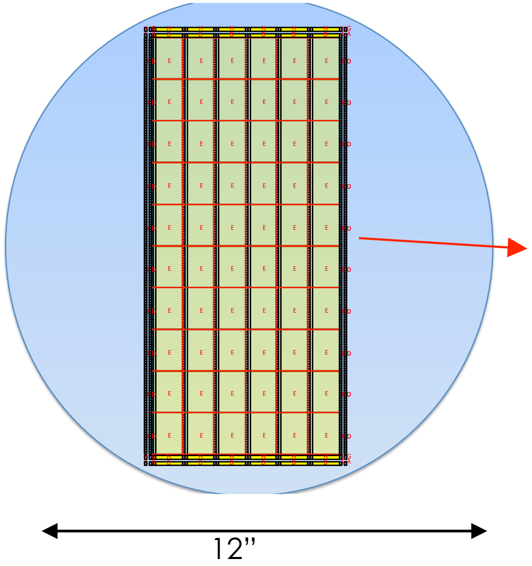
2nd submission: Engineer Run 1 (ER1)

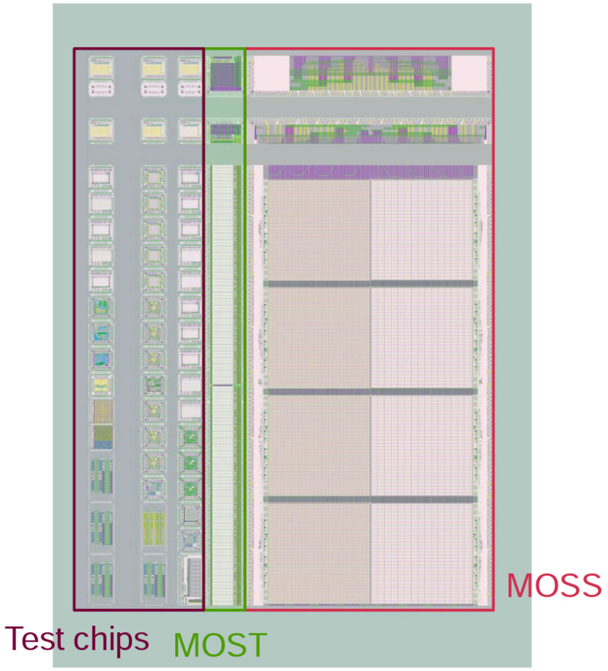
- Main goal = exercise stitching (in 1D) to assess yield
- Submission November 2022
- Back from fab April 2023

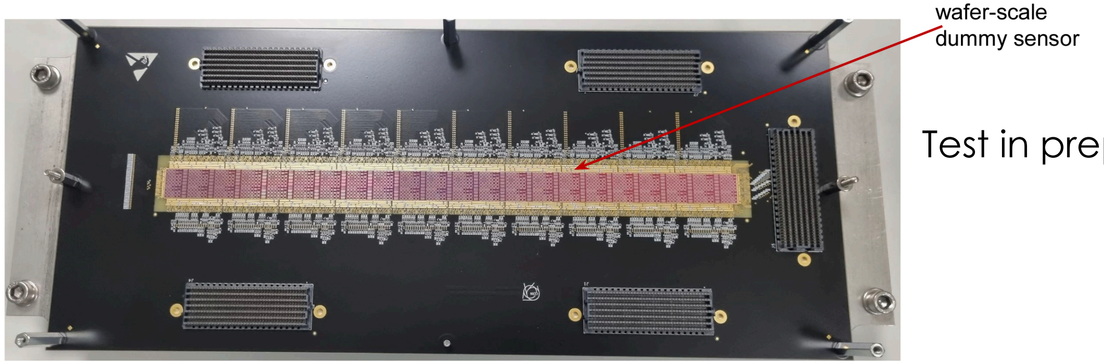
- 2 long (~26 cm) sensors
  - **MOSS:** priority-encoder readout (ALPIDE-like)
    - 1.4 cm wide
    - 18 & 22.5 µm pitch
  - **MOST:** low power asynchronous readout
    - 0.25 cm wide

- Many (51) **chiplets**
  - Pixel prototypes
  - SEU test chips
  - Functional blocks (PLL, serial links)

- New metal staks
- New methodology for submission
  - Digital-on-top







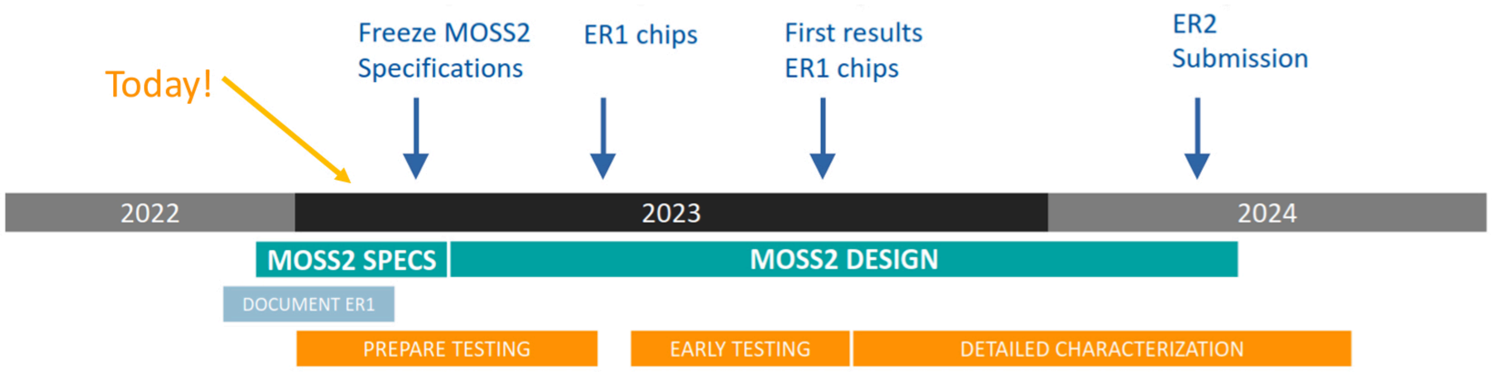
Test in preparation

3rd submission: ER2

Towards ER2 submission

EP R&D

- ER2 submission will focus on a large area stitch sensor that targets the ALICE ITS3 requirements
  - Build on ER1 learned lessons
  - Increased dimensions (1.8 x 26 cm)
  - Decreased dead area (between 6.7% - 9.5%)
  - Increased readout speed (between 25.6 Gbps – 51.2 Gbps)
  - On chip power regulation for power segmentation and IRdrop compensation (~0.6% active area granularity)
- Design specifications are ongoing



20 Feb 2023 EP R&D Day | WP1.2 | Pedro Leitao 13

Conclusion

- 1st submission: **MLR1** **Pre-AIDAinnova**
  - Test structures + Functional blocs
  - Various pixel structures

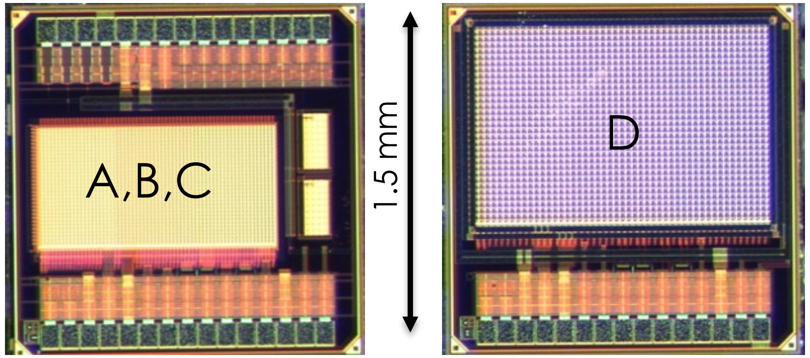
Activities in 2021-23 mostly driven by CERN EP R&D-roadmap & ALICE-ITS3 } Still targeting GENERAL GOALS in excellent synergy with WP5

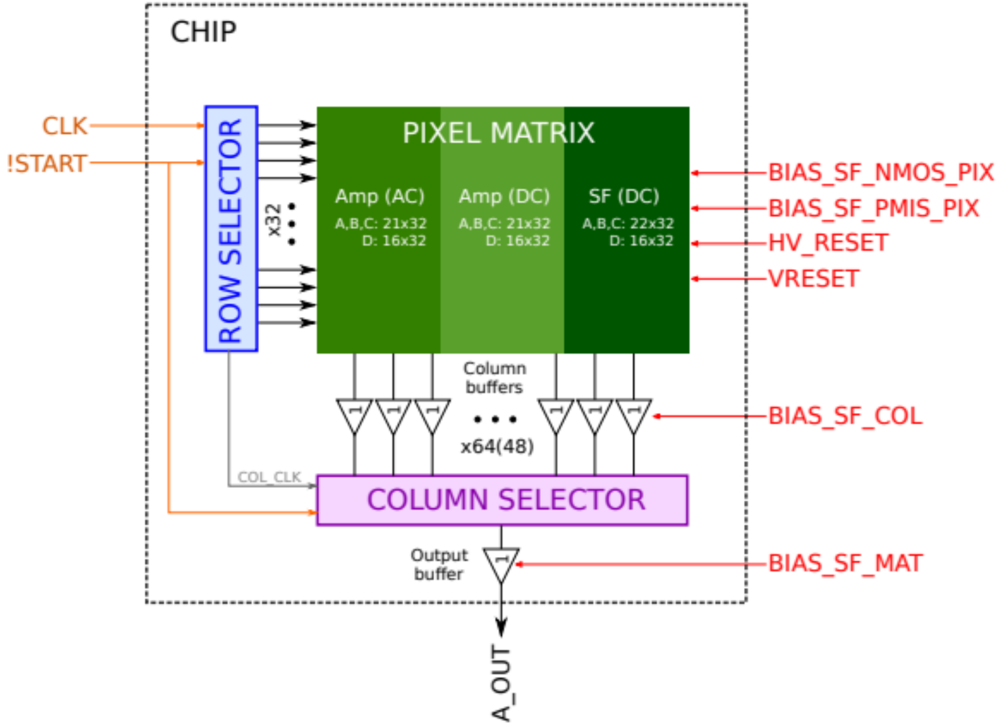
	Design work	Testing work	Question addressed
			⇨ Techno validation
2023	• Preparation for **ER2** - ALICE-ITS3 stitched sensors - Still some chiplets	• Finalise tests on **MLR1** • **Start ER1 tests** - 1st test on stitched sensors - Tests on chiplets	• Yield with stitching • Handling/bending of thin & large (<100cm²) area • Performance optimisation (space & time resolution
2024	• **3nd submission: ER2** • Preparation for **4th submission** - MLR2 with new R&D tracks	• Continued tests on **ER1** • Preparartion of **ER2** tests	⇨ Techno exploration
2025	• 4th submission ?	• Tests of **ER2**	• Readiness for ALICE-ITS3

Supplementary slides

CE-65 sensors

- Contribution from IPHC





4 different flavours

- Square pixels
- Analogue output
- Rolling-shutter readout 10 to 40 MHz

Variant	pitch	Matrix size	Front-ends	Collection diode structure	Split
A	15 µm	64x32	DC-SF, DC-Amp, AC-Amp	Basic	1-4
B				Blanket w gaps	
C				Blanket	
D	25 µm	48x32		basic	

Note:

- AC-coupled front-end allows sensitive volume biasing without backside voltage