

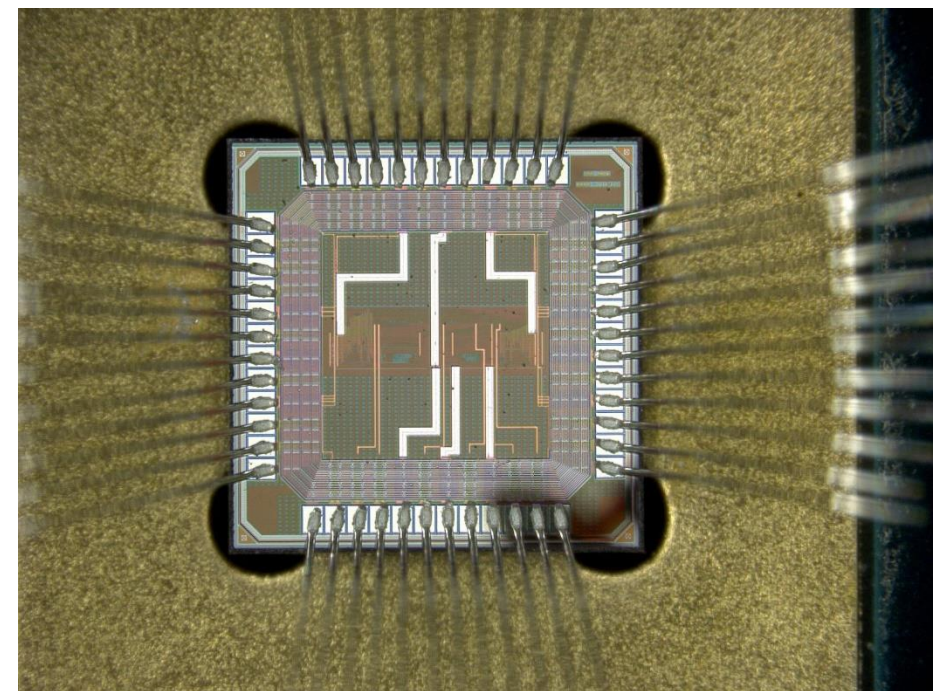
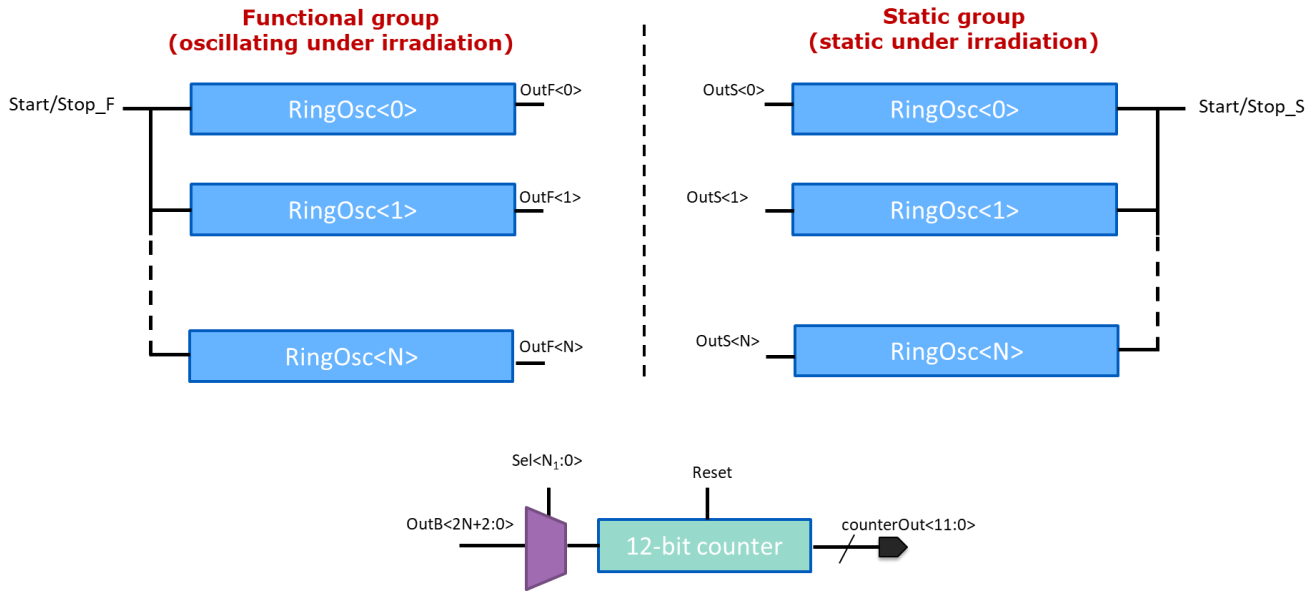
# TPSCo 65nm CIS Ring Oscillators Temperature, Irradiation and Annealing tests

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Patrick Pangaud

April 25<sup>th</sup> 2023

AIDA – Innova meeting

# The ring oscillators



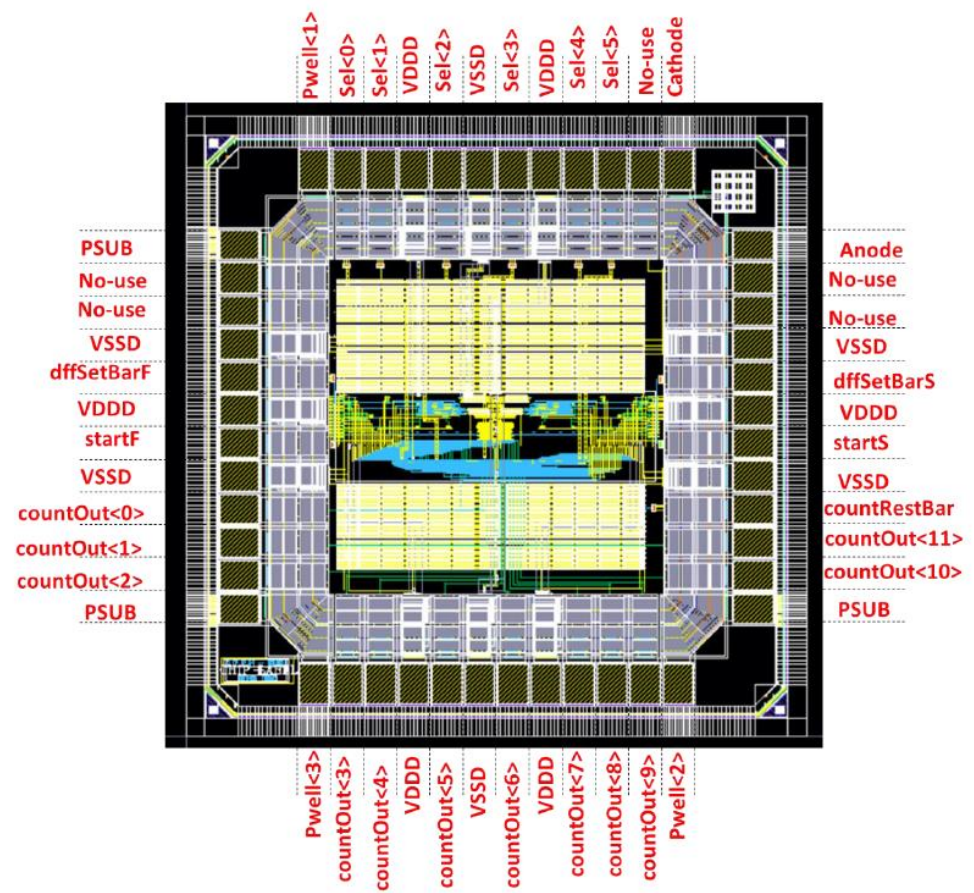
- In 2020, participation to the MLR1 run in TowerJazz 65 nm through CERN's EP-R&D WP1.2, by designing a **Ring Oscillator test chip** to characterize the standard cells of this technology.
- The chip contains 48 ring oscillators made of a chain of 101 standard cells.
- 2 banks of 24 Rows each with the purpose of testing two approaches while irradiating:
  - Functional: the oscillation is enabled
  - Static: the oscillation is disabled

| Low $V_T$   |             | Super Low $V_T$ |              |
|-------------|-------------|-----------------|--------------|
| Size Min    | Size+       | Size Min        | Size+        |
| INV0_LVT    | INV4_LVT    | INV4_SLVT       | INV8_SLVT    |
| NOR1_LVT_A  | NOR4_LVT_A  | NOR4_SLVT_A     | NOR8_SLVT_A  |
| NOR1_LVT_B  | NOR4_LVT_B  | NOR4_SLVT_B     | NOR8_SLVT_B  |
| NAND0_LVT_A | NAND4_LVT_A | NAND4_SLVT_A    | NAND4_SLVT_A |
| NAND0_LVT_B | NAND4_LVT_B | NAND4_SLVT_B    | NAND4_SLVT_B |
| DFF1_LVT    | DFF4_LVT    | DFF1_SLVT       | DFF4_SLVT    |

# The ring oscillators

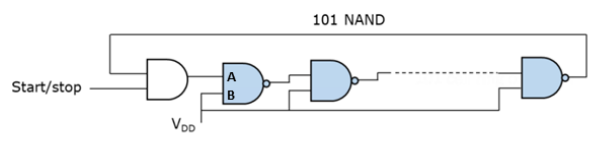
Table 3: Typical oscillation frequencies

| Channel number | Cell Name    | Schematic [MHz] | Post-layout (F) [MHz] | Post-layout (S) [MHz] |
|----------------|--------------|-----------------|-----------------------|-----------------------|
| ch<0>, ch<24>  | Inv0_LVT     | 298,9           | 195,5                 | 196,8                 |
| ch<1>, ch<25>  | Inv4_SLVT    | 392,9           | 286,6                 | 288,8                 |
| ch<2>, ch<26>  | Inv4_LVT     | 304,1           | 241,6                 | 244,4                 |
| ch<3>, ch<27>  | Inv8_SLVT    | 392,9           | 292                   | 294,5                 |
| ch<4>, ch<28>  | NOR1_A_LVT   | 147,7           | 128                   | 129,1                 |
| ch<5>, ch<29>  | NOR4_A_SLVT  | 184,7           | 148                   | 148,8                 |
| ch<6>, ch<30>  | NOR1_B_LVT   | 185,1           | 139                   | 140,7                 |
| ch<7>, ch<31>  | NOR_4_B_SLVT | 229,5           | 183,1                 | 185,9                 |
| ch<8>, ch<32>  | NOR4_A_LVT   | 152,1           | 122,3                 | 123,6                 |
| ch<9>, ch<33>  | NOR8_A_SLVT  | 182,6           | 149,2                 | 150,3                 |
| ch<10>, ch<34> | NOR4_B_LVT   | 190,1           | 152,6                 | 153,9                 |
| ch<11>, ch<35> | NOR8_B_SLVT  | 226,1           | 169,5                 | 170,7                 |
| ch<12>, ch<36> | NAND0_A_LVT  | 174,3           | 136,2                 | 137,2                 |
| ch<13>, ch<37> | NAND4_A_SLVT | 217,2           | 174,2                 | 176,2                 |
| ch<14>, ch<38> | NAND0_B_LVT  | 200,2           | 134,2                 | 135,1                 |
| ch<15>, ch<39> | NAND4_B_SLVT | 246,6           | 198,7                 | 200,5                 |
| ch<16>, ch<40> | NAND4_A_LVT  | 180,9           | 146,3                 | 145,6                 |
| ch<17>, ch<41> | NAND8_A_SLVT | 213,9           | 173,8                 | 175                   |
| ch<18>, ch<42> | NAND4_B_LVT  | 206,6           | 167,7                 | 169,4                 |
| ch<19>, ch<43> | NAND8_B_SLVT | 242,1           | 182,4                 | 183,8                 |
| ch<20>, ch<44> | DFF1_LVT     | 344,1           | 168,1                 | 170,1                 |
| ch<21>, ch<45> | DFF1_SLVT    | 372,5           | 182,6                 | 184,2                 |
| ch<22>, ch<46> | DFF4_LVT     | 352,3           | 187,4                 | 188,8                 |
| ch<23>, ch<47> | DFF4_SLVT    | 383,1           | 200,8                 | 194,9                 |

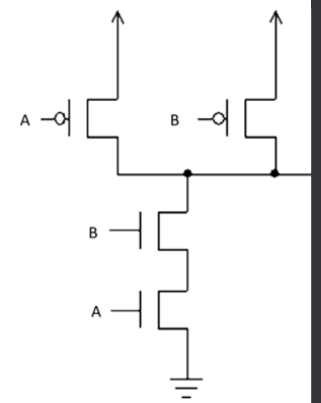
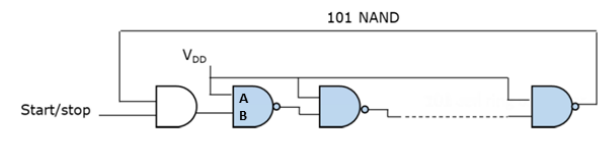


The 24 ring oscillators, of each bank, differ from each other by the **type of cells** they were made of (Inverter, NAND, NOR and DFF), with variations in the **transistor width** (e.g: Inv0, Inv4 and Inv8, the width being larger with increased number) and **threshold** (Low VT and Super Low VT). **A and B** correspond to 2 flavors to observe the effect of the proximity of the power supply rail.

Multi-input cells: e.g. NAND2 Input A

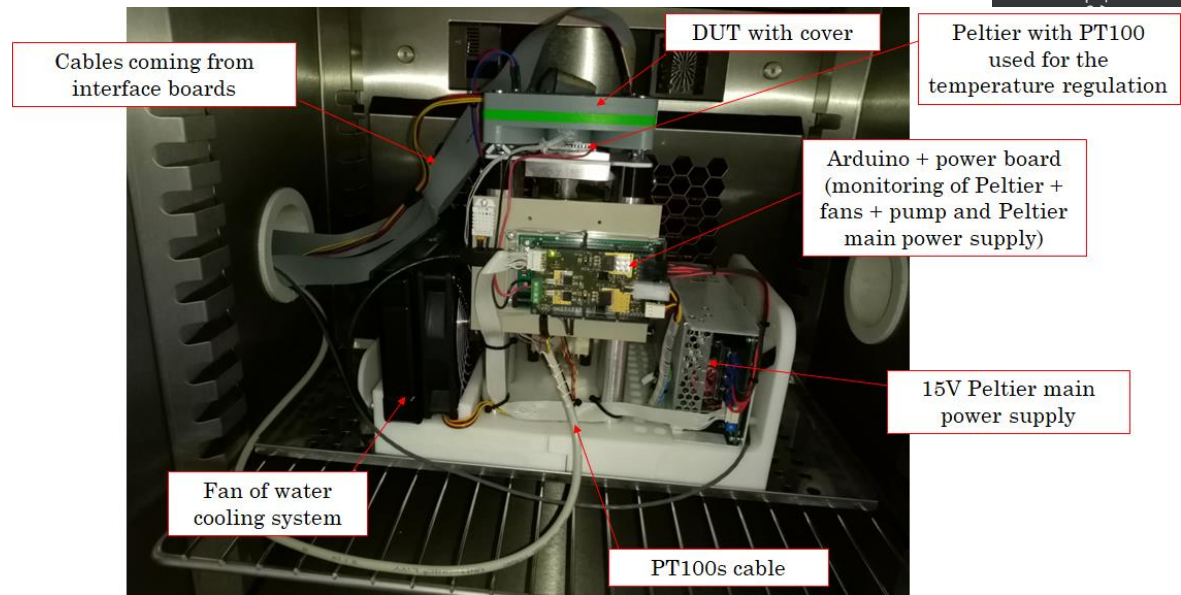
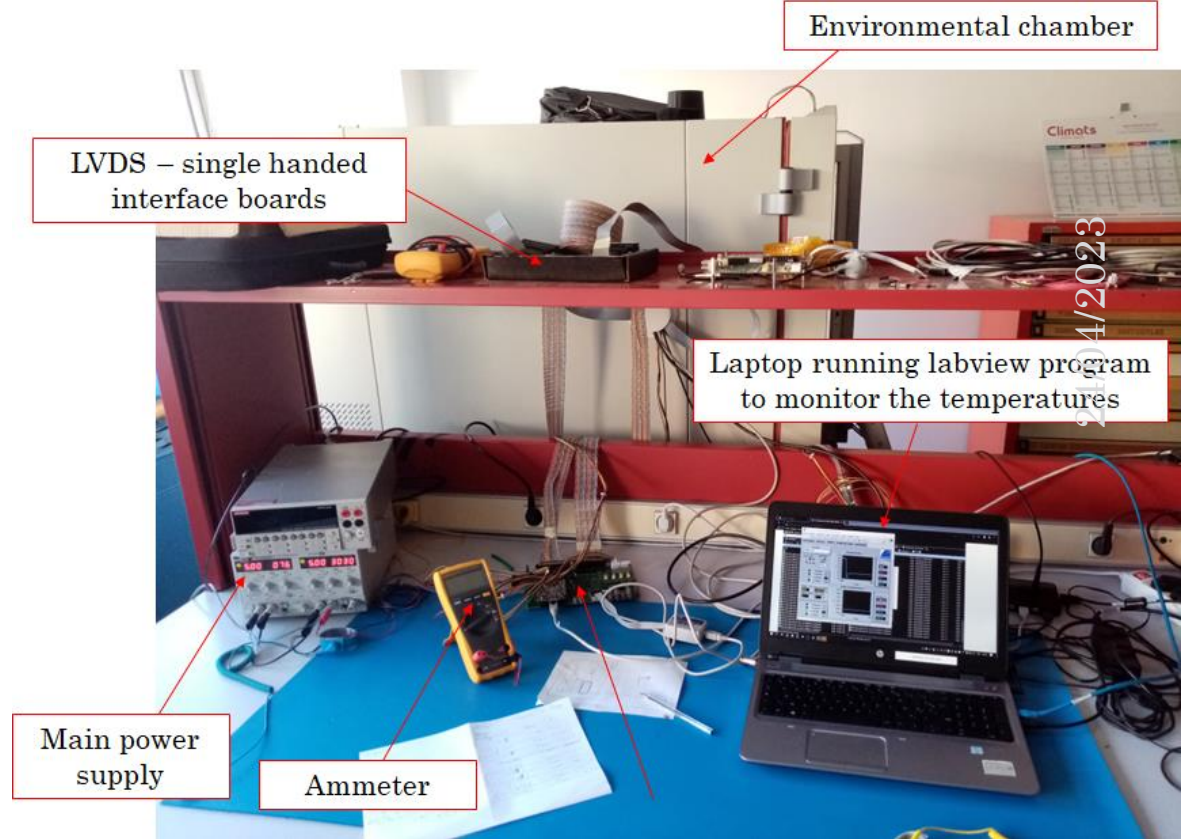


Multi-input cells: e.g. NAND2 Input B



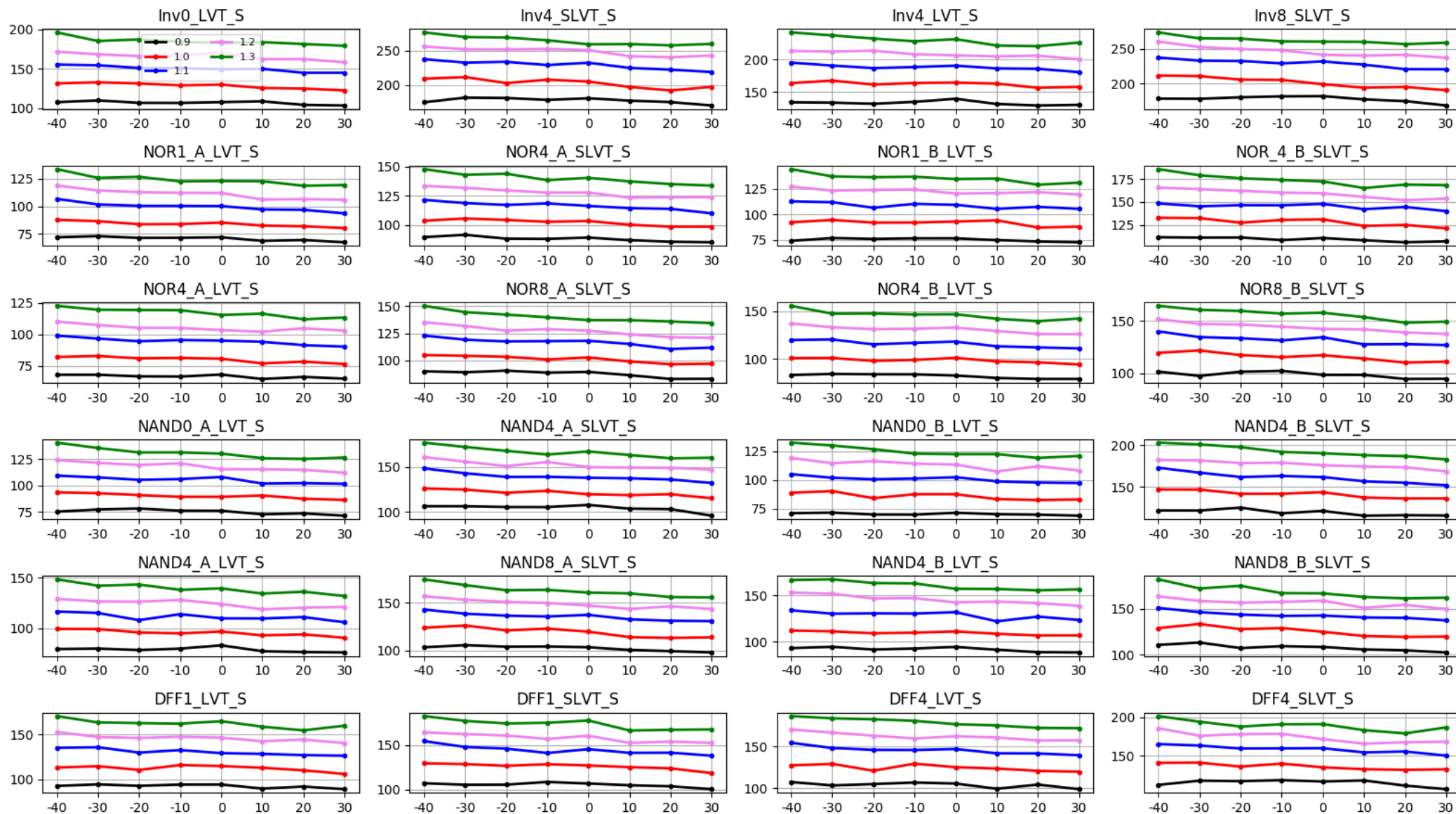
# Temperature tests

- The temperature tests were carried out with the characterization set-up (DUT board, beaglebone + mezzanine, interface boards) and an environmental chamber to regulate the temperature.
- In addition, inside the chamber a **Peltier system** was used to accurately set the temperature at the level of the circuit.
- Temperature regulated at 8 values: -40, -30, -20, -10, 0, 10, 20 and 30 °C
- At each temperature: 5 different values of the V<sub>dd</sub>: 0.9, 1.0, 1.1, 1.2 (nominal) and 1.3V
- For each couple (Temperature, V<sub>dd</sub>), 20 measurements were taken for each ring oscillator.
- Offline, the data were analyzed by computing the mean count for each RO and then calculating the mean frequency.
- Each RO exhibits a decrease of the frequency while the temperature increases (5-10 % over 70°C) whatever the V<sub>dd</sub> or the bank.



# Separating RO: temperature effect

BANK S

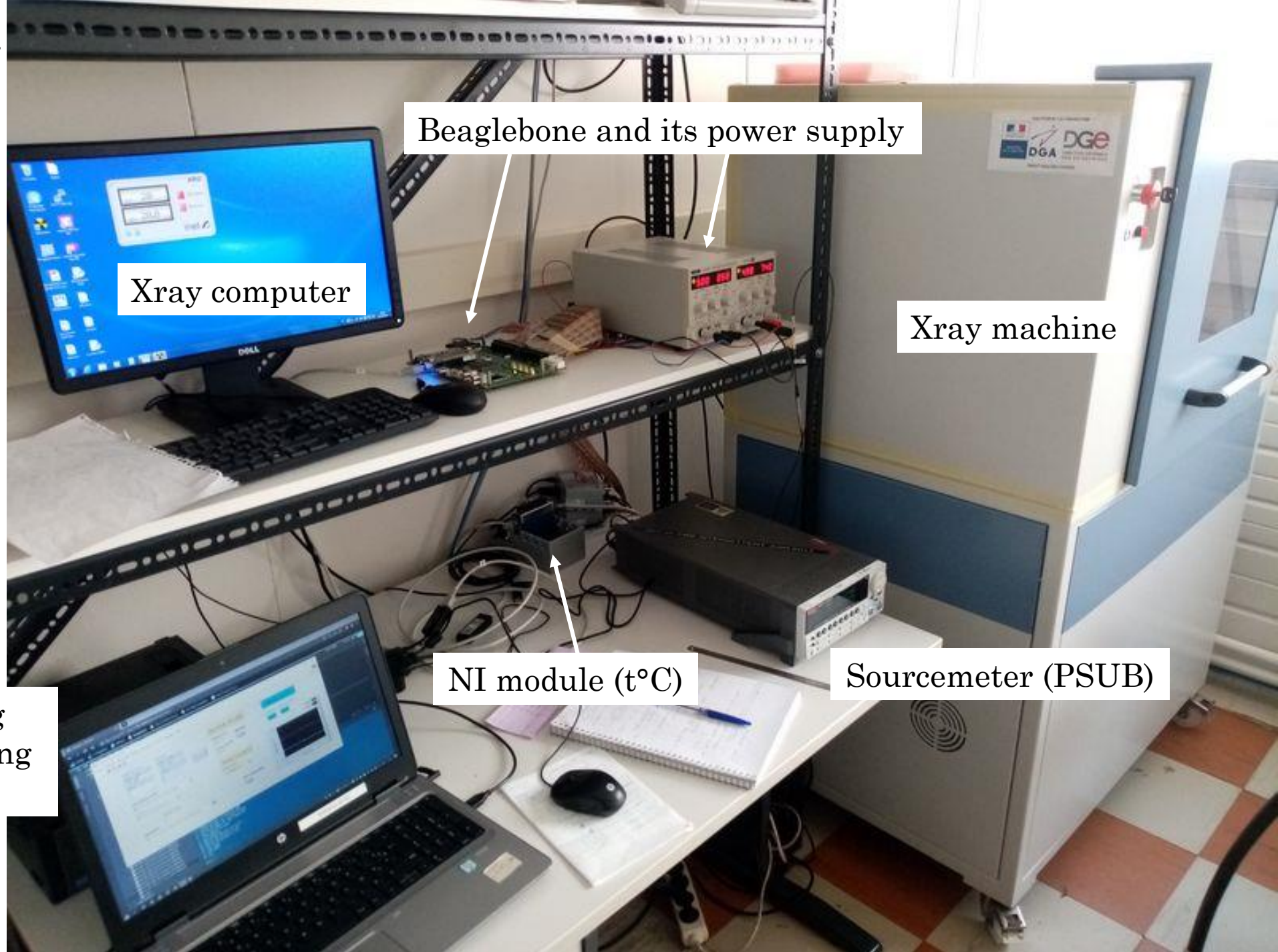


24/04/2023

# Tests: irradiation & annealing

- Irradiation performed at ambient temperature with no regulation.
- Xray tube at 1 cm above the DUT (dose rate:  $\sim 20$  krad/mn).  
Temperatures (pcb and ambient) monitored every minute.
- During irradiation bank F oscillating and bank S no oscillating.
- Paused at specific TID  
both banks oscillating and measurement of the 24 RO of each bank.
- 2 chips tested:
  - **Chip1**: 4 weeks irradiation (**830MRad**) followed by annealing at  $-18^{\circ}\text{C}$  (21 days),  $25^{\circ}\text{C}$  (25 days) and  $80^{\circ}\text{C}$  (9 days). It is **important to that the functional bank of the chip1 was incorrectly configured during the irradiation and therefore was also kept static.**
  - **Chip2**: started irradiation 13/06/22. Chaotic because of Xray tube cooling system. Several technical stops correlated to the outside temperature. 20/06/22 : a mobile clim is installed and running ( $25^{\circ}\text{C}$  regulation) in the room. Still we had interruptions (for some  $> 1$  day). We stopped at **521 Mrad**.
- Both chips responded similarly to the irradiation and exhibited a decrease (up to 25%) of the frequencies. We observed differences between ring oscillators, depending on the type, length, and threshold of the transistors of the base cells.
- **Annealing**: For all the ring oscillators, we observed no recovery at cold temperature ( $-20^{\circ}\text{C}$ ), a small recovery at room ( $25^{\circ}\text{C}$ ) and what looks to be a reverse annealing at warm temperature ( $80^{\circ}\text{C}$ ).

# The Xray Set-up



Xray computer

Beaglebone and its power supply

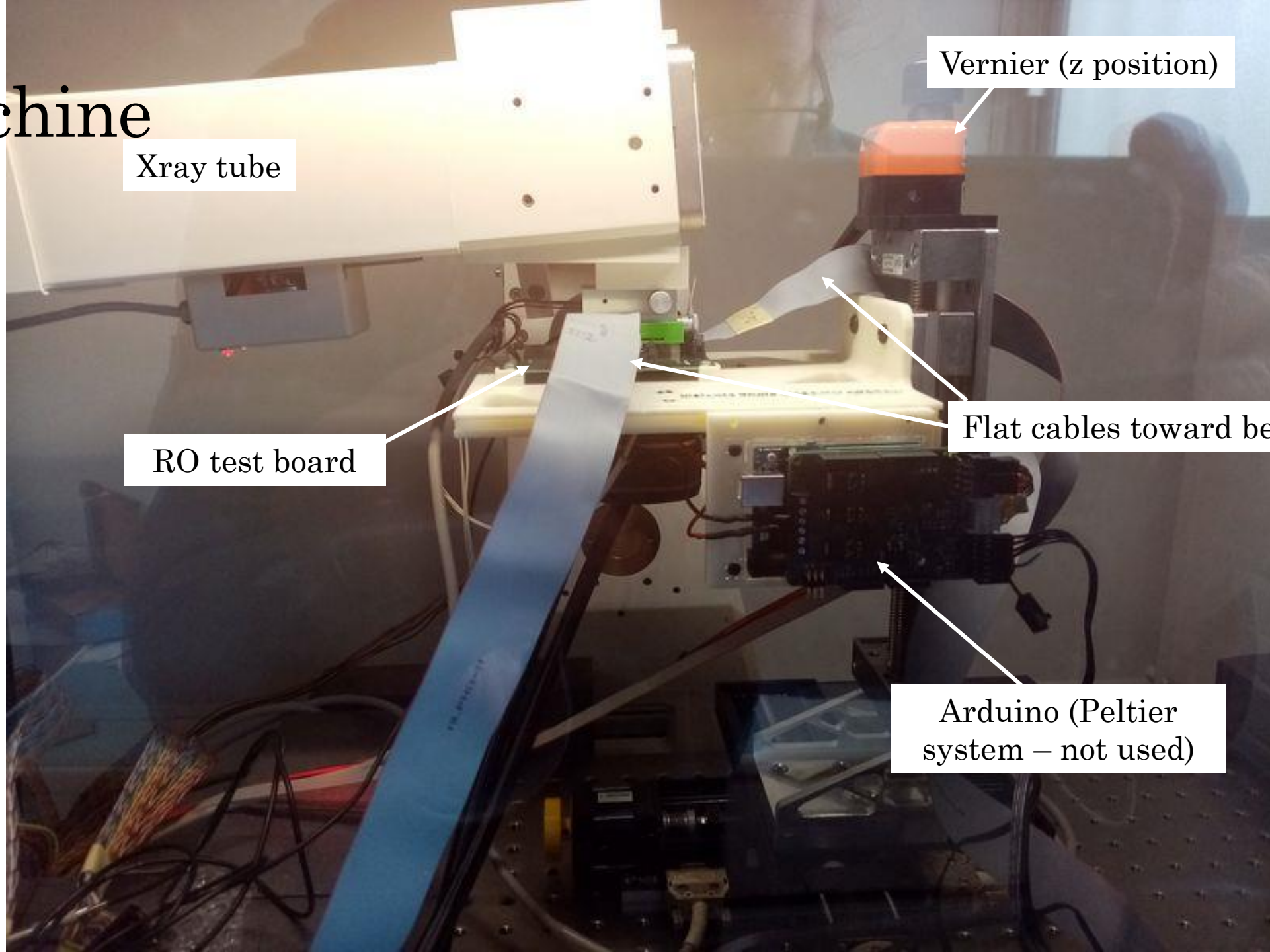
Xray machine

NI module (t°C)

Sourcemeter (PSUB)

Laptop running labview monitoring and c++ script

# Inside the machine



Xray tube

Vernier (z position)

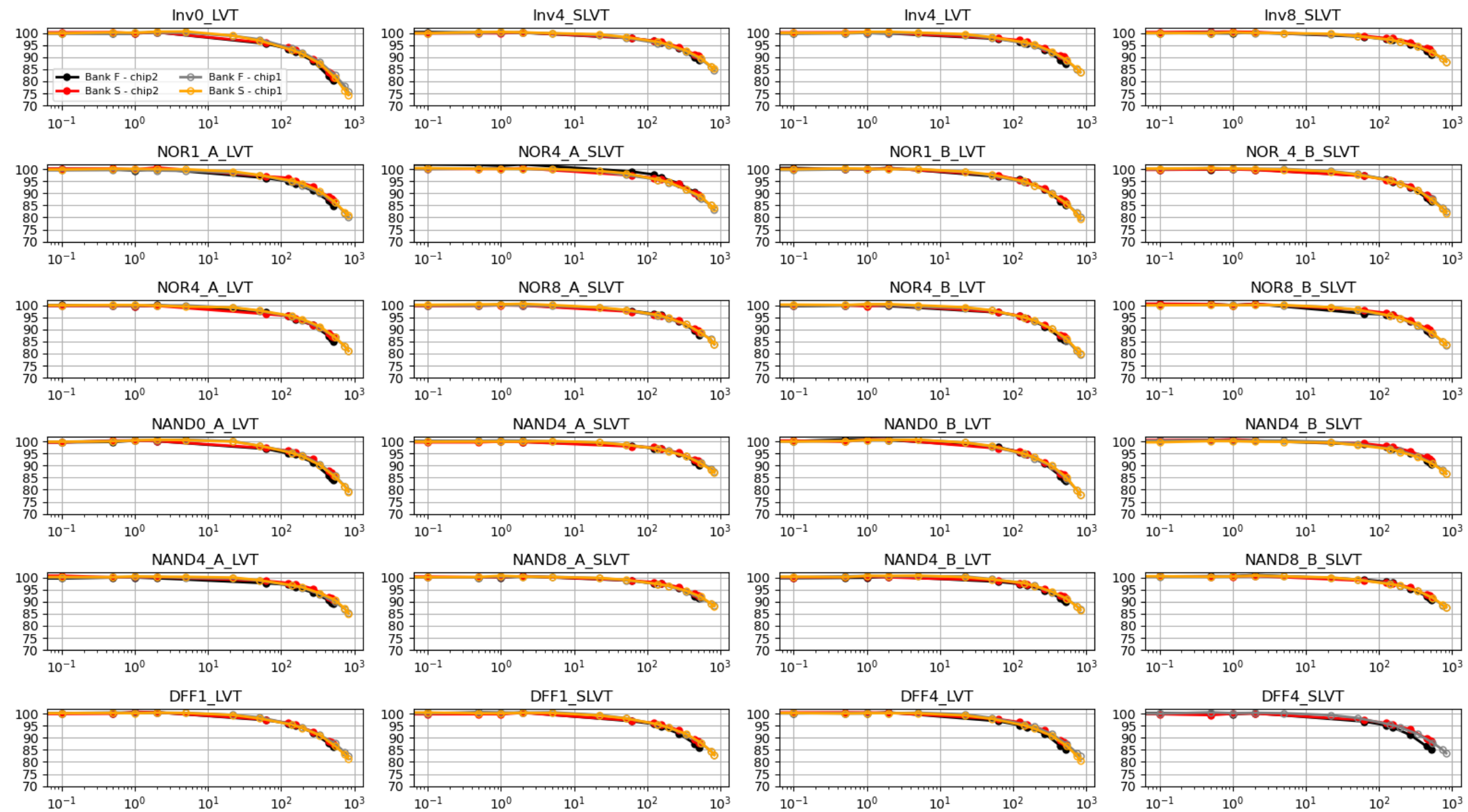
RO test board

Flat cables toward beaglebone

Arduino (Peltier system – not used)

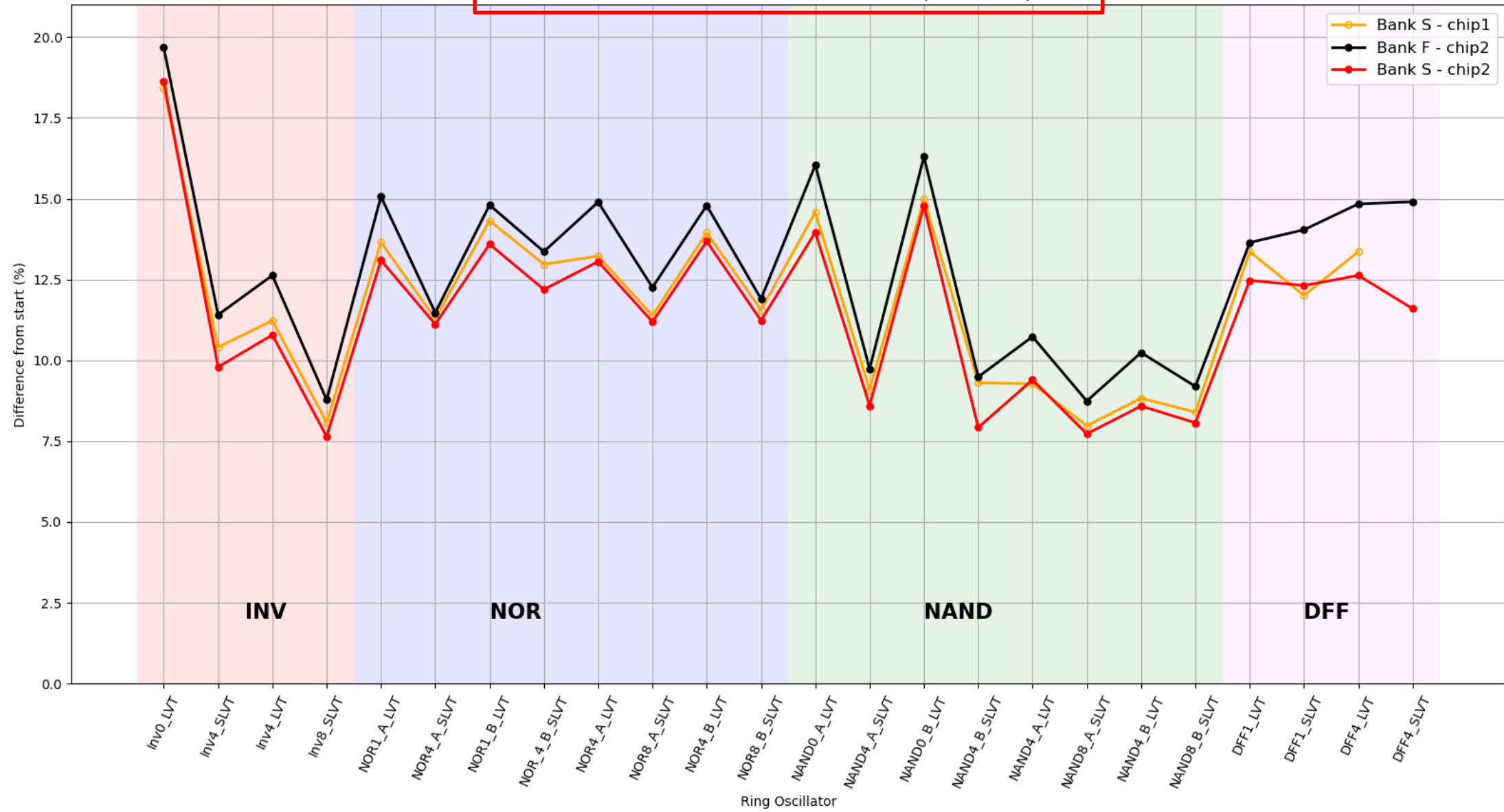


# Chip1 and chip2 relative frequency vs dose

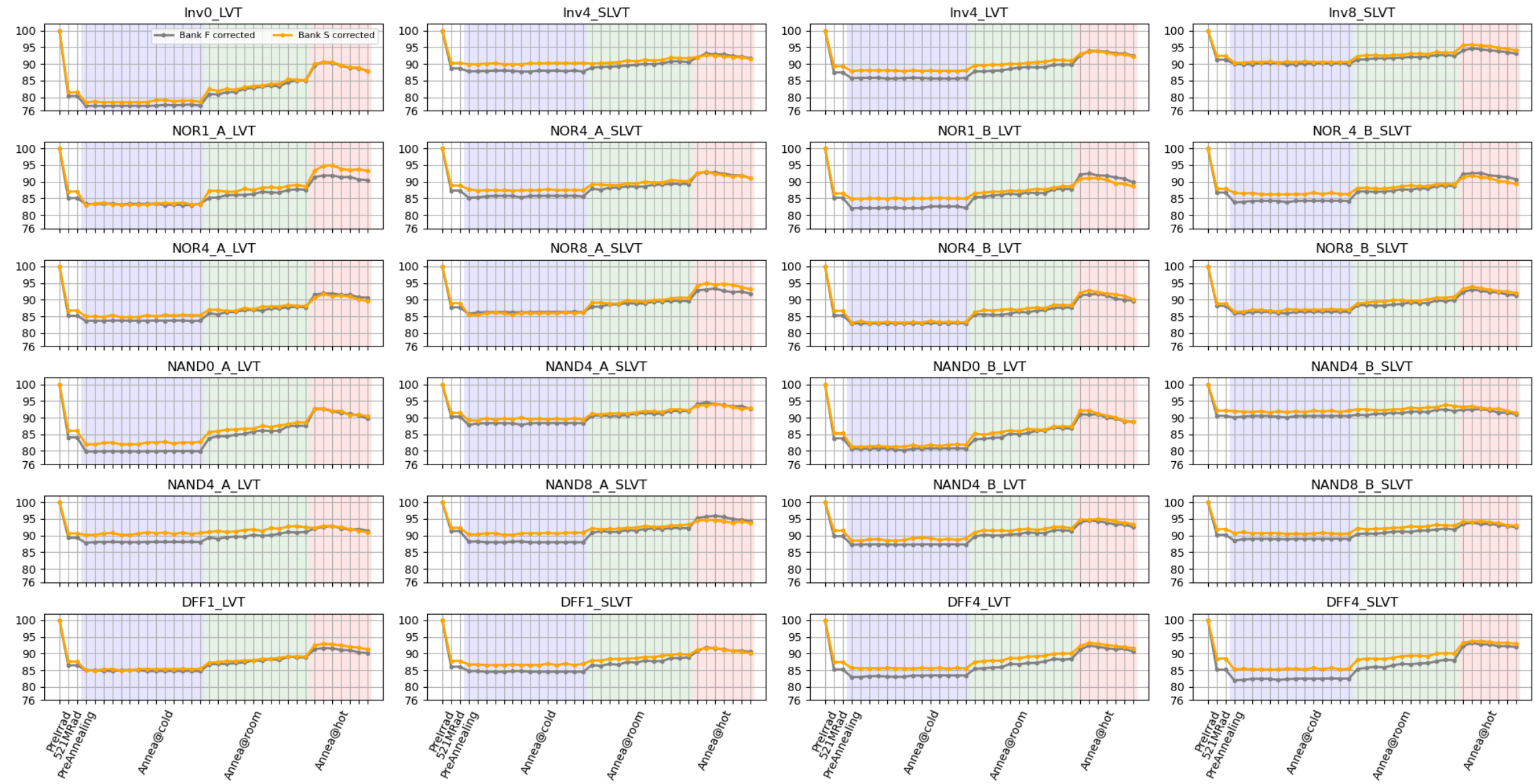


# Chip1 and chip2 relative difference

Difference (%) from 0kRad to ~530MRad - comparison chips 1&2



# Chip2 annealing with temperature correction



# Conclusions

- The temperature has an impact (**decrease of the frequencies with increasing temperature**) that can be quantified.
- Irradiation shows a decrease of the frequencies for all types of RO with a level different depending on the cell (**from 12 to 25% at 830 Mrad**).
- The size of the cells is an important parameter, the smaller cells (e.g Inv0) being more affected than the bigger ones (e.g Inv8).
- The difference between the two banks is not clearly visible while similar results were obtained for both chips tested.
- Annealing seemed dependent of the temperature with a better impact (recovery) at ambient (25°C).
- A poster has been presented at **TWEPP 2022** and associated proceedings accepted early 2023.
- This **limited degradation opens perspective** for the usage of digital cells of this technology in high radiation environments.
- **Resubmission with new ER → to be tested summer 23.**

**Digital cells radiation hardness study of TPSCo 65nm CIS technology by designing a Ring Oscillator**

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**Introduction**  
The CPPM group has long been designing and testing HV-CMOS blocks to complete monolithic chips in various technologies (T130, LF50, AMS) in the framework of several collaborations. In 2020, we participated in the MLRI run in Toverazz 65 nm technology through CERN's EP-R&D WP1.2, by designing a ring oscillator test chip. Its aim is to characterize the standard cells of this technology and evaluate their radiation hardness against TID as well as their behavior at different temperatures.

**Description**  
24 ring oscillators were designed and duplicated to form two banks: the Functional (F) bank which is made to oscillate during irradiation and the Static (S) bank, under bias in a state state while the chip is being irradiated. Each ring oscillator is composed of a chain of 101 cells, to count a realistic frequency, interrupted by an AND gate, that commands the start/stop of the cell. They differ from each other by the type of cells they are made of, with variations of length, threshold and input locations.

**Measurement set-up**  
The test chip is bonded on a DUT board connected to a Beaglebone DAQ system (Linux Os embedded). For the communication, each sequence is described in VHDL, inside a FPGA and launched thanks to a C++ script. Data recorded are analyzed with python programs.

**Temperature tests**  
A climate chamber regulating the temperature from -40 to 80°C was used for the temperature tests that were performed for different VDD. Each RO exhibits a decrease of the frequency while the temperature increases (5-10% over 70°C).

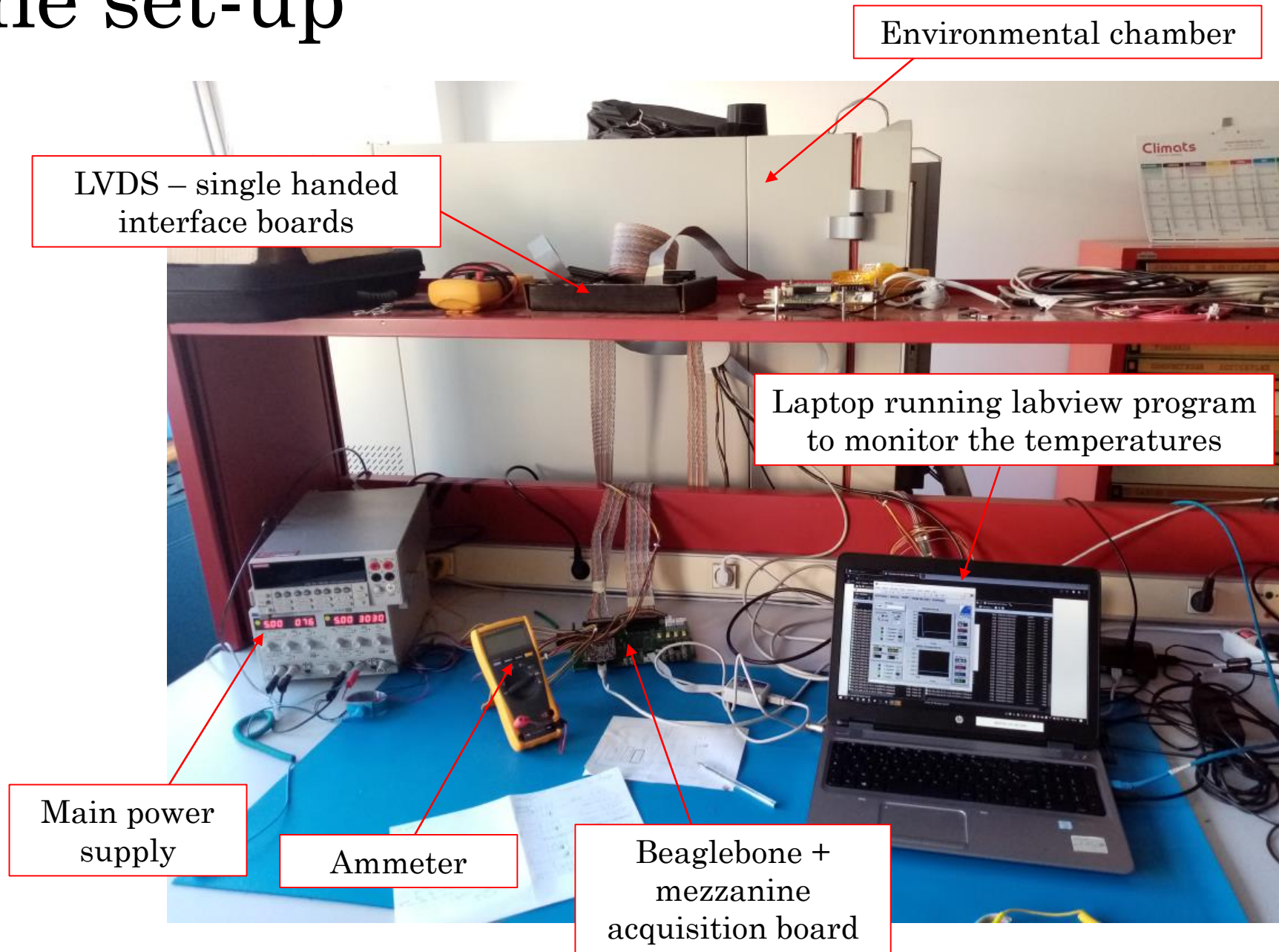
**Irradiation campaigns**  
Two chips (1 and 2) have been irradiated, at ambient temperature with an X-ray machine, up to 830 and 520 Mrad respectively (20% attenuation can occur due to a 3µm thick stack-up of copper on the top side). The dose rate delivered was 20 kRad/min (calibration performed with an AXUVIS photodiode + 150 µm mask at later before each campaign). During the exposure time, the ring oscillators from the functional bank were kept oscillating while the ones from the static bank were not. Regular measurements of the frequencies, with both banks put in oscillating mode, were performed along the irradiation periods.

**Annealing**  
After irradiation, the chips went for annealing periods at three different temperatures, successively 20, 25 and 80 °C, following a procedure described in a document from the ESA (E. B. S. No. 22900 "Total dose steady-state irradiation test method," Issue 3 (2007)). The duration of each period was adjusted from 1 week to several weeks. At 20°C, the DUT board was installed in a freezer and the DAQ system on a table next to it. At 25°C, the DUT board was relocated next to the DAQ system in a regulated room. Finally at 80°C, the DUT board was installed in the same climate chamber used for the temperature tests. We applied a correction to take into account the temperature difference of the three annealing periods. For all the ring oscillators, we observed no recovery at cold temperature (20°C), a small recovery at room (25°C) and what looks to be a reverse annealing at warm temperature (80°C).

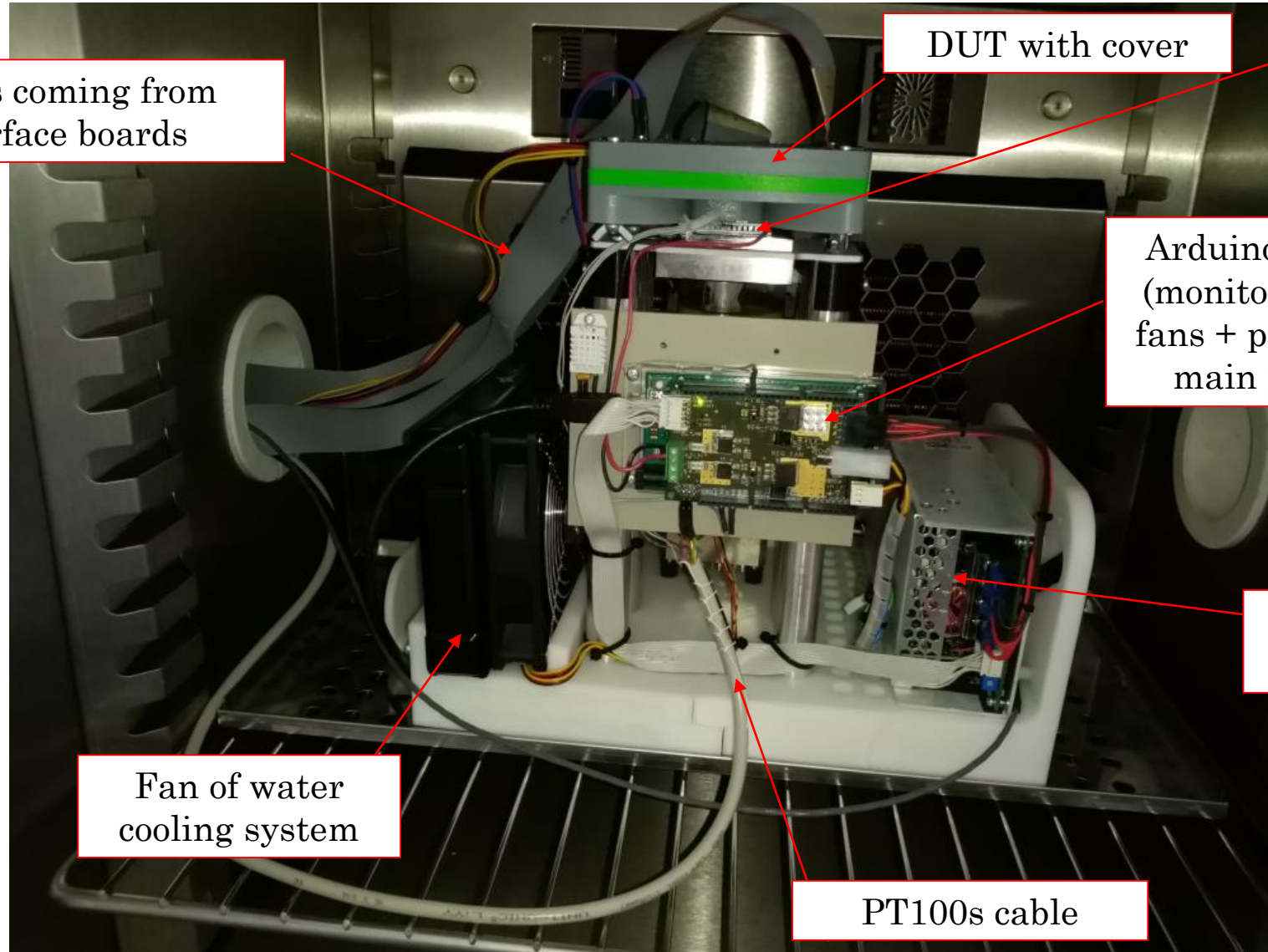
**Conclusions**  
The study of radiation hardness of TPSCo 65nm (T165) technology based on ring oscillators measurements showed relevant results. The frequencies decreased for all types of ring oscillators exhibiting different impact of the TID (from 12 to 25% at 830 Mrad). This limited degradation opens perspective for the usage of digital cells of this technology in high radiation environments. The temperature has an impact that can be quantified and corrected. Finally, the annealing period at high temperature (80°C) can be interpreted like a reverse annealing behavior and must be considered for the future developments in this technology.

End

# The set-up



# The set-up inside the chamber



Cables coming from interface boards

DUT with cover

Peltier with PT100 used for the temperature regulation

Arduino + power board (monitoring of Peltier + fans + pump and Peltier main power supply)

15V Peltier main power supply

Fan of water cooling system

PT100s cable