AIDA innova bluesky

Production of a demonstrator for the Silicon Electron Multiplier concept

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Gemma Rius (IMB-CNM)

2nd AIDAinnova conference, 25th April 2023

Centro Nacional de Microelectrónica IMB

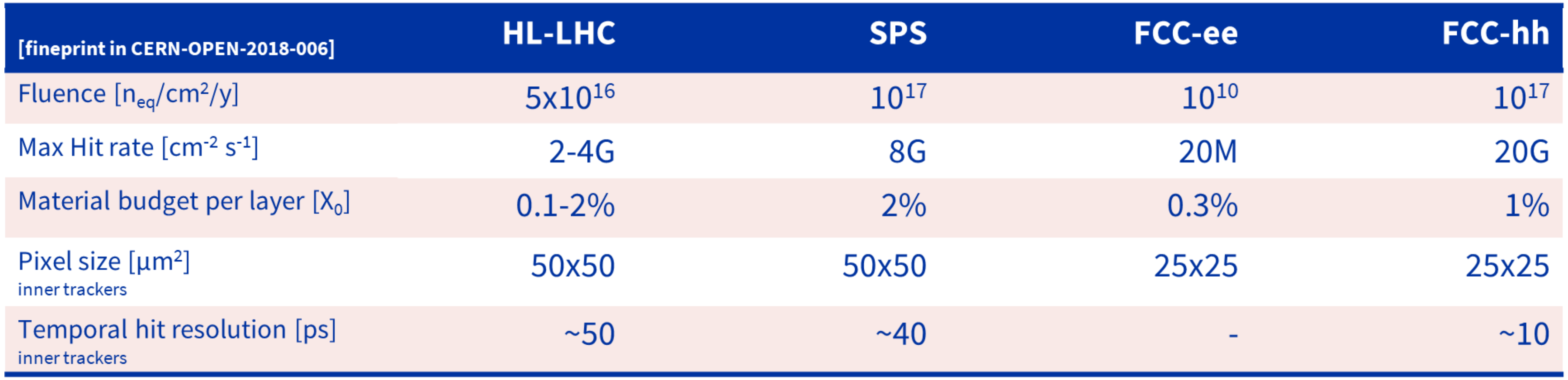
CSIC Consejo Superior de Investigaciones Científicas

www.imb-cnm.csic.es

Motivation

- New HEP accelerator applications require increasing radiation hardness (cumulative dose per year)
  - From 5×10^{15} n_{eq}/cm^2 in ATLAS IBL lifetime to 10^{17} n_{eq}/cm^2 in FCC-hh **per year**
- Inner trackers start requiring excellent time resolution
- High pile-up requires finer granularity

from the CERN Strategic R&D Programme on Technologies for Future Experiments [CERN-OPEN-2018-006]

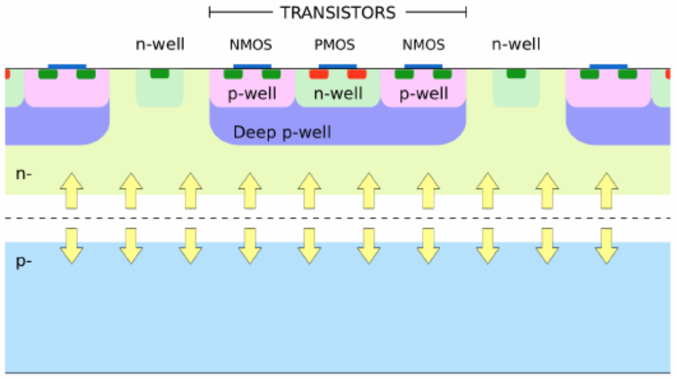


[fineprint in CERN-OPEN-2018-006]	**HL-LHC**	**SPS**	**FCC-ee**	**FCC-hh**
Fluence [$n_{eq}/cm^2/y$]	5×10^{16}	10^{17}	10^{10}	10^{17}
Max Hit rate [cm^{-2} s^{-1}]	2-4G	8G	20M	20G
Material budget per layer [X_0]	0.1-2%	2%	0.3%	1%
Pixel size [µm²] inner trackers	50x50	50x50	25x25	25x25
Temporal hit resolution [ps] inner trackers	~50	~40	-	~10

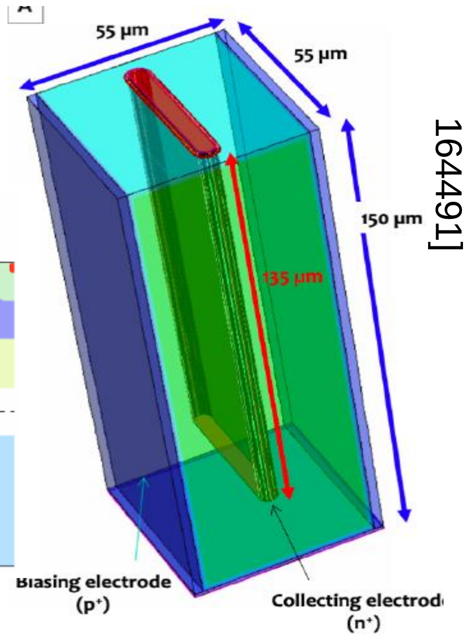
Challenge: pixelated detector with resolutions of down to 10 ps, able to survive high fluences

Motivation

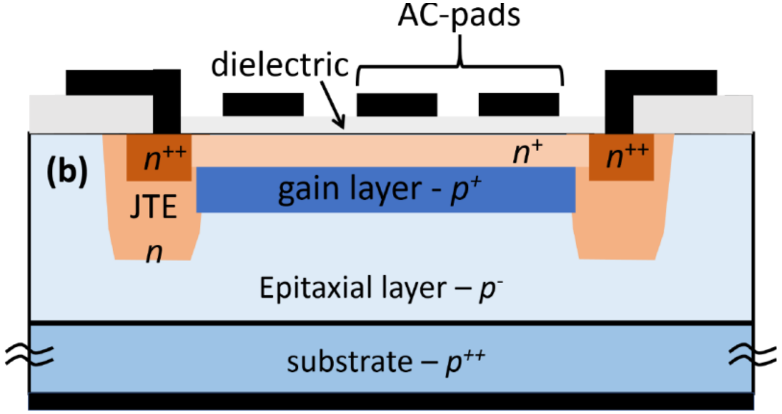
- Monolithic sensors:
  - **PRO:** resolution (spatial & temporal), material budget
  - **CONS:** radiation hardness, data rate (but could be bonded to CMOS), temporal resolution
- **3D sensors :**
  - **PRO:** radiation hardness, temporal resolution, spatial resolution
  - **CONS:** spatial resolution, fill factor, capacitance
- LGAD familly:
  - **PRO:** temporal resolution
  - **CONS:** radiation hardness, spatial resolution (could be solved by AC-LGAD, Ti-LGAD or iLGAD
- **Internal gain without radiation damage sensitivity**?



[MALTA; NIM A 990(2021) 164895]



[Timespot; NIM A (2020) 164491]



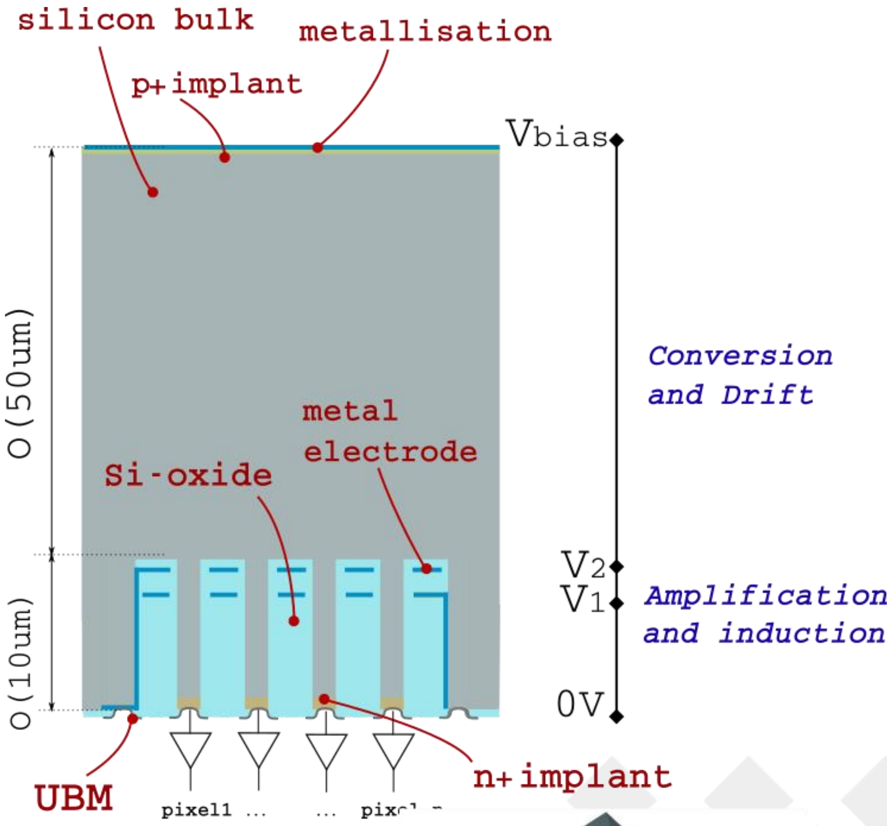
[AC-LGAD; JINST 14 (2019) P09004]

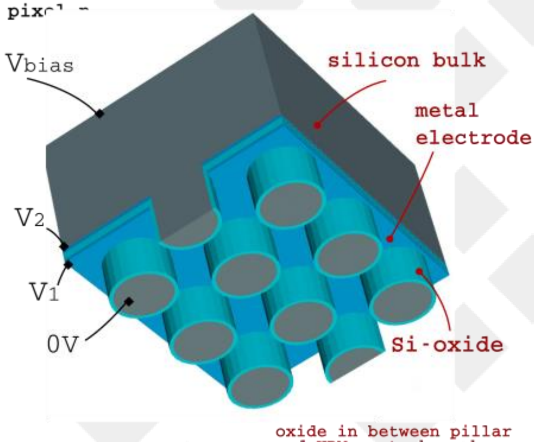
The Silicon Electron Multiplier concept

- Instead of relying on high doping concentration for charge multiplication (LGAD), adapt the **geometry of the device for high fields**
  - Multiplication mechanism not compromised by acceptor removal
- Electrons generated by ionisation in the bulk, multiplied in **amplification region** (high field from electrodes 1&2)
  - After charge multiplication, charge carriers induce signal on the readout electrodes
- Individual readout pillar width: ~2-4 um
  - Possibility of small pitch/pixel size

Potential for small pixel size, multiplication not affected by radiation and 100% fill factor

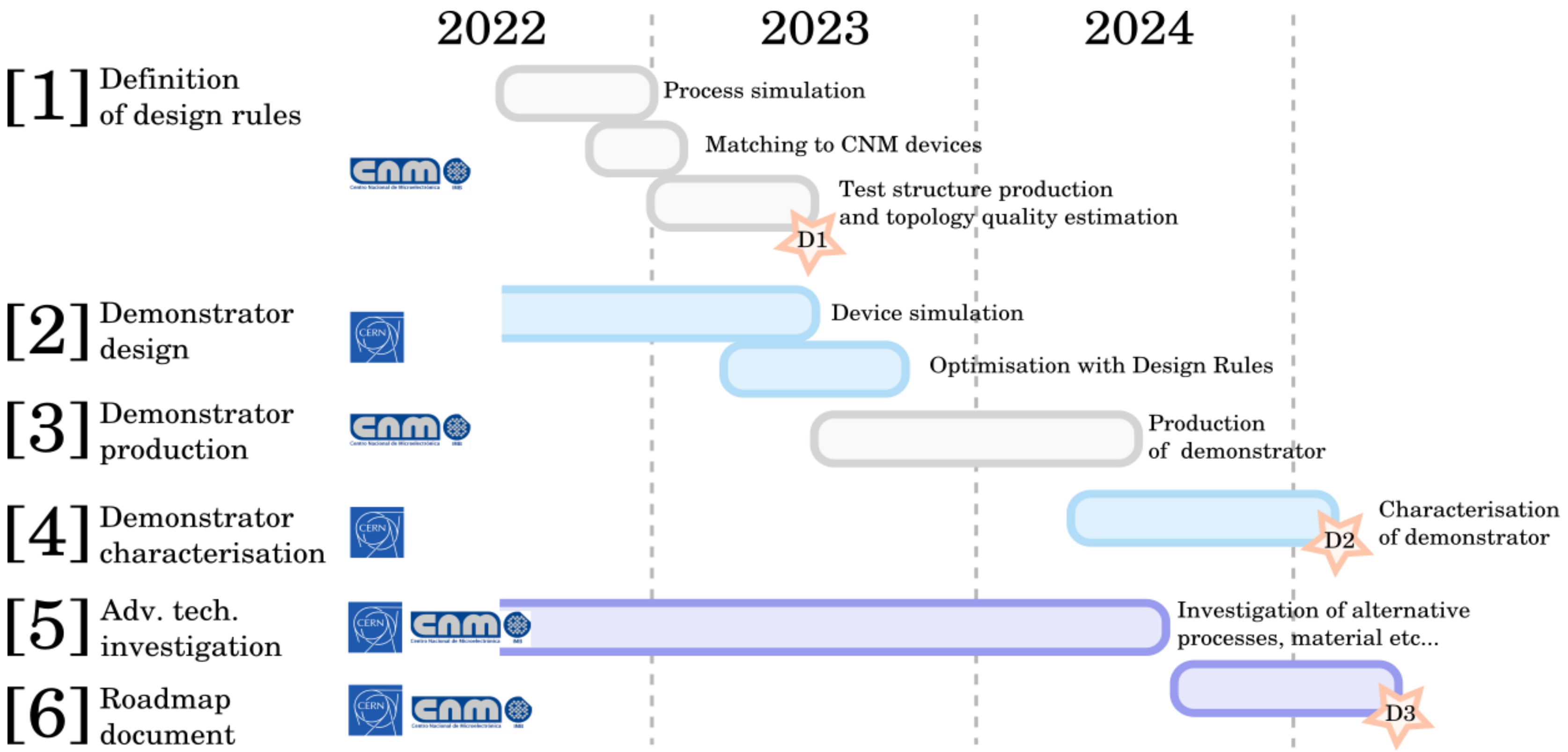
→ **Promising for future colliders**





NIM A 1041 [2022] 167325

Planning towards demonstrator


2022
2023
2024

[1] Definition of design rules
Process simulation
Matching to CNM devices
Test structure production and topology quality estimation
D1

[2] Demonstrator design
Device simulation
Optimisation with Design Rules

[3] Demonstrator production
Production of demonstrator

[4] Demonstrator characterisation
Characterisation of demonstrator
D2

[5] Adv. tech. investigation
Investigation of alternative processes, material etc...

[6] Roadmap document
D3

Milestones

D1 Specifiaction of design rules for buried electrodes with DRIE process

D2 Demonstrator performances description

D3 Roadmap document on the technology

Team

- **CERN**
  - Victor Coco [coordination]
  - Marius M. Halvorsen [PhD] until Oct 2023
  - Federico De Benedetti [PhD] to start ~Feb 2023 [25% AIDAinnova]
  - Vagelis Gkougkousis until Feb 2023 – Edgar Cid Lemos fellow to joined in 2023 [support]

- **CNM**
  - Giulio Pellegrini [coordination]
  - Ivan Lopez Paz [postdoc] started in July for 2 years 100% AIDAinnova
  - Gemma Rius [researcher]
  - + technical and executive support from the Clean Room staff (DRIE expert etc…)

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Simulation

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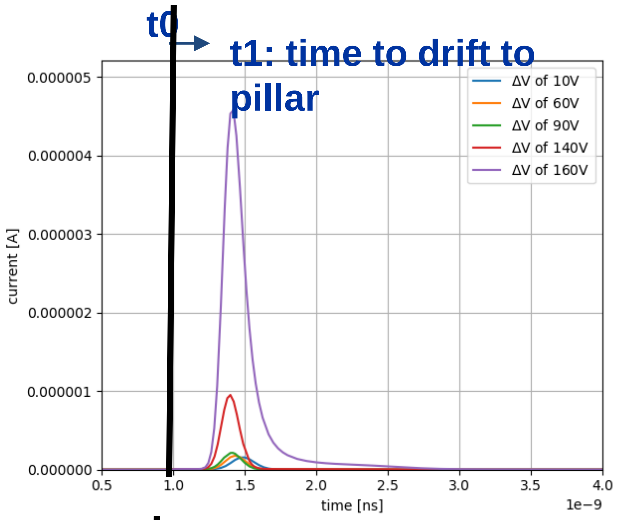
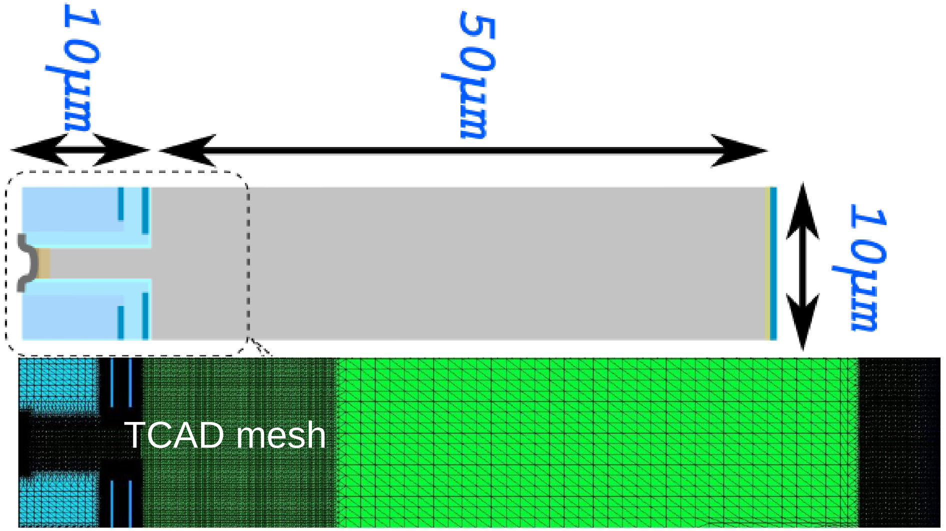
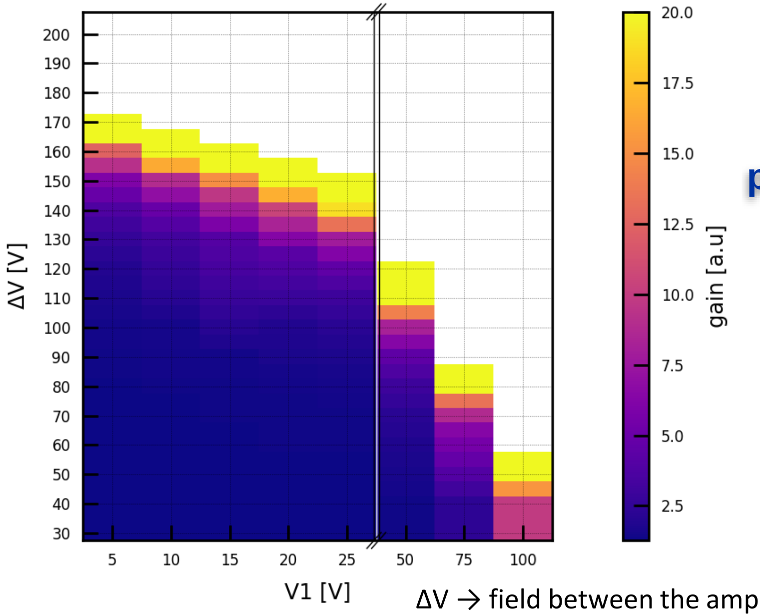
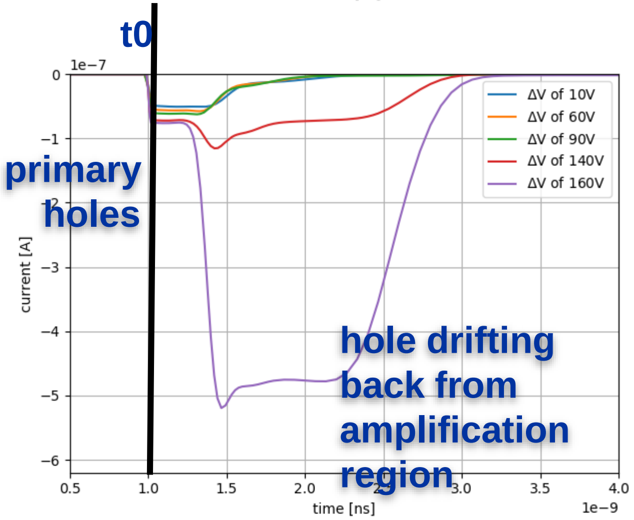
- Simulation demonstrates charge multiplication mechanism:
  - Carriers multiplication when electrons reach amplification region
  - Gains of up to x20 observed in simulation study (depending on geometry and applied bias)



t1: time to drift to pillar







primary holes

hole drifting back from amplification region

ΔV → field between the amplification electrode (V_2-V_1)
V_1 → between upper and readout electrode
V_{bias} = -30 V (depleted bulk)

Carrier multiplication to be verified in hardware
→ Physical realisation: **Production of demonstrator device**

Demonstrator layout design

Matching simulation dimensions

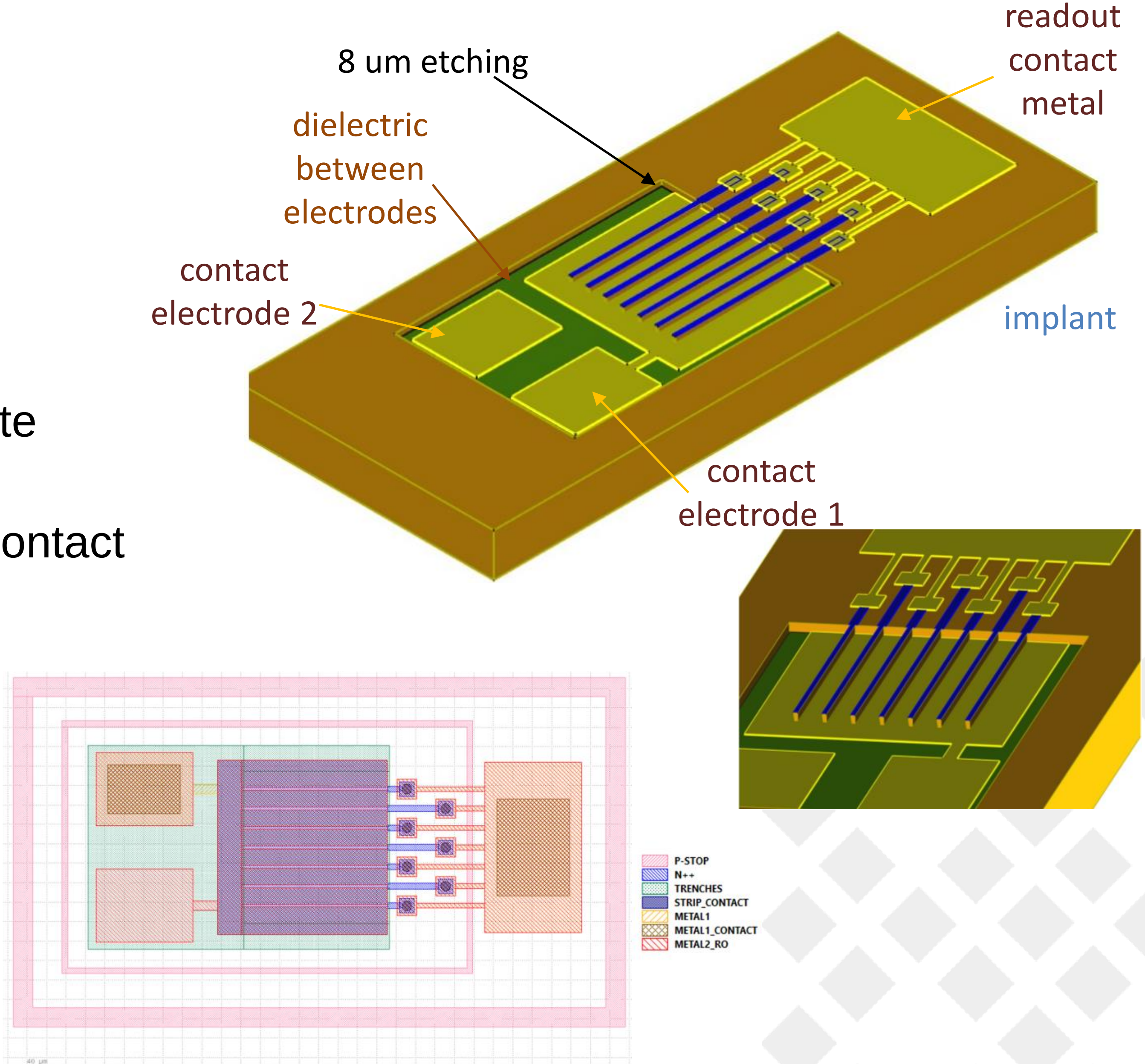
- Pillar widths: 2, 3 and 4 um
- Inter-electrode dielectric thickness: 1 um

Strip design for proof-of-concept: demonstrate amplification mechanism

- Interconnected strips, shorted to readout contact
  - Allow for wirebonding for testing

2 amplification electrodes

Opening on back side for TCT tests

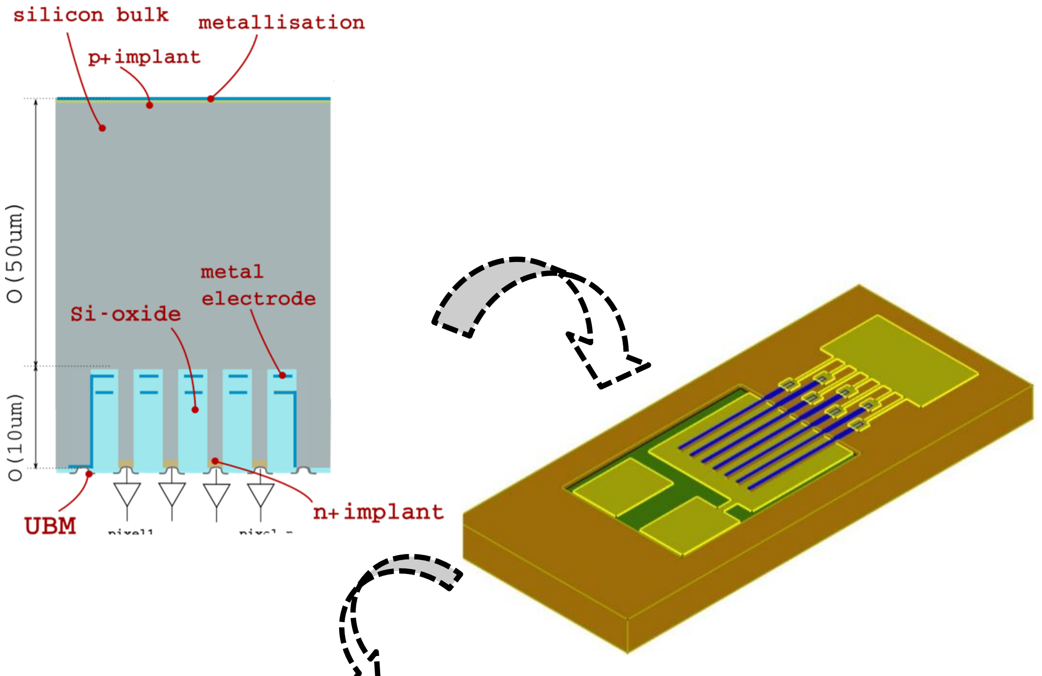


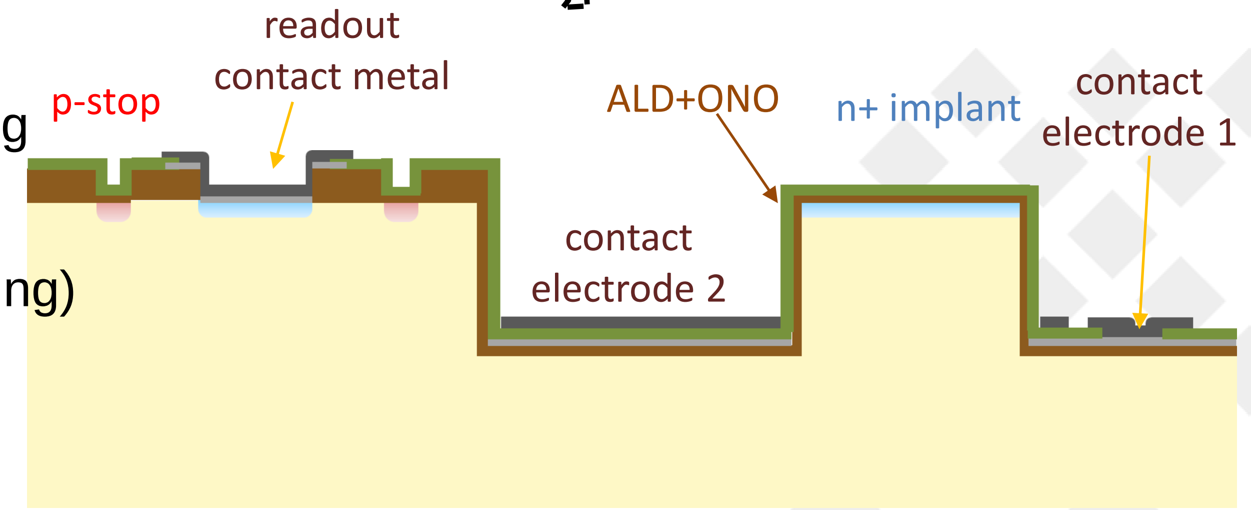
Design and processing definition

- Trenches
  - laser photolithography → trenches
  - Si etching depth ~8um
- Electrode 1 deposition
  - surface treatment
  - ALD 50nm oxide, metal deposition, ALD 50nm oxide
  - Oxide deposition O(um)
- Electrode 2 deposition

Challenges:

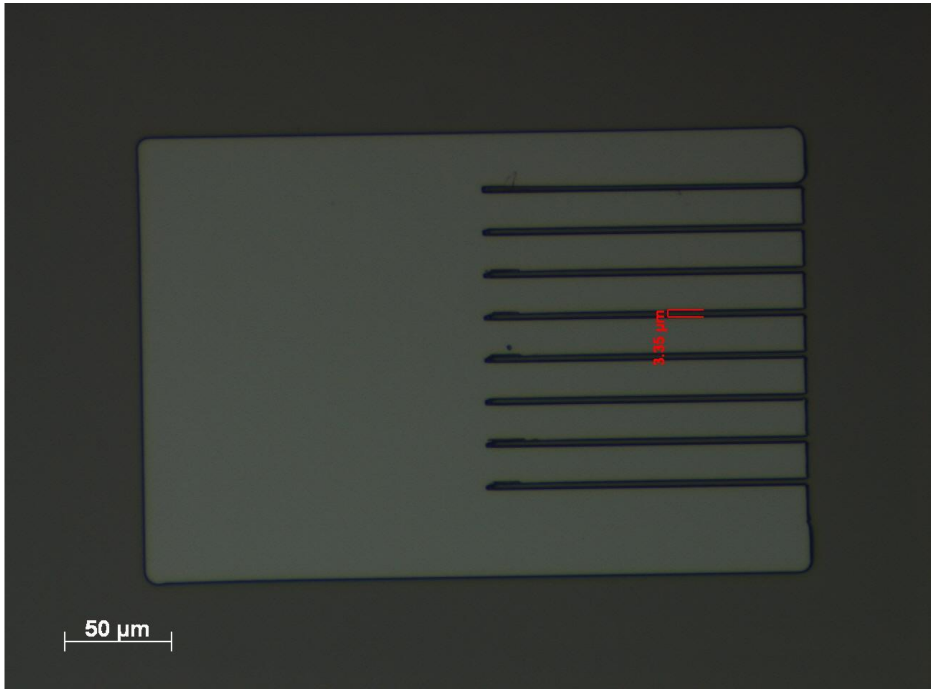
- Oxide layer can induce stress ⇒ limit the gap between electrodes 1 and 2
- Etching limited in width depending on patterning process used:
  - laser photolithography down to 2um (design/layout fliexibility, good for prototyping)
  - electron beam lithography (adjustment needed)



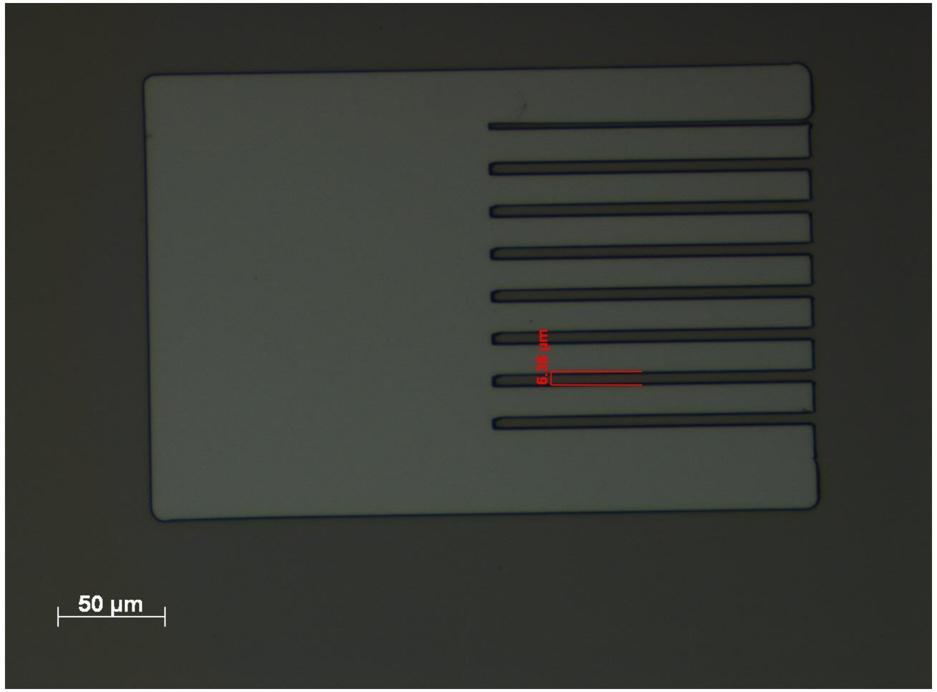


Photolithography tests

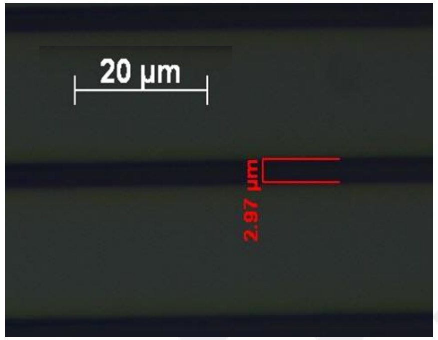
- **Pillar diameter / width test**
  - test with 3 and 6um wide trenches OK
    - optimisation of exposition and development parameters
  - probably possible to go to 2um
    - ⇒ limited by the laser resolution

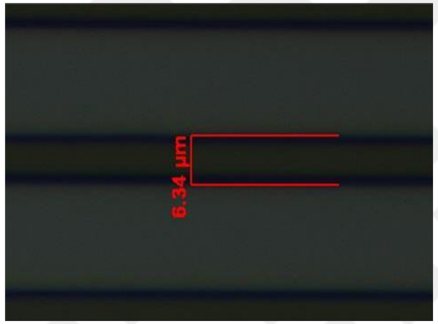


Photolithography test (3um)



Photolithography test (6um)



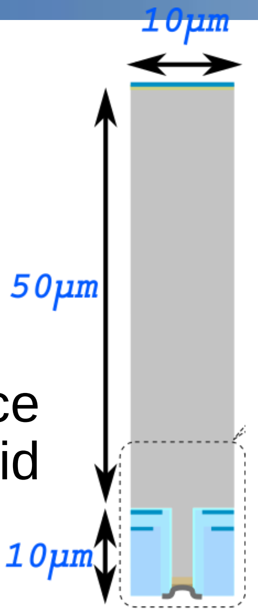


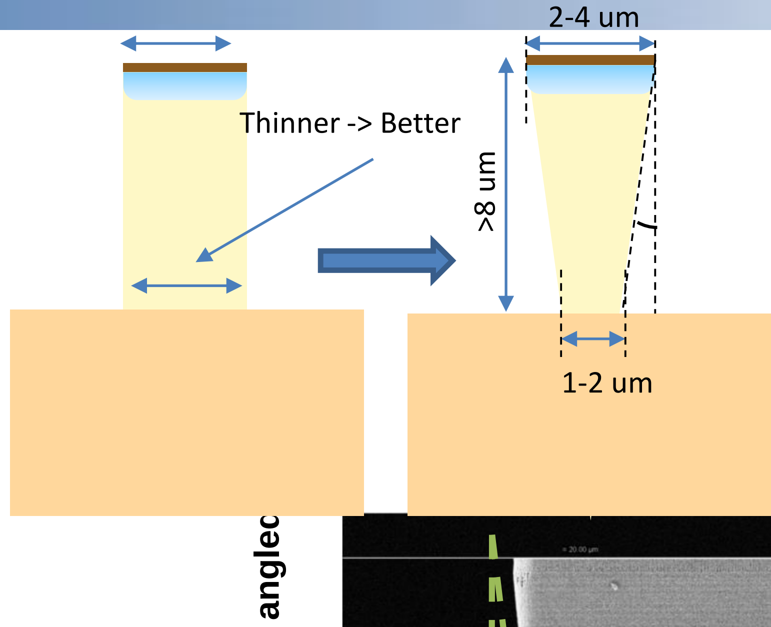
Etching tests

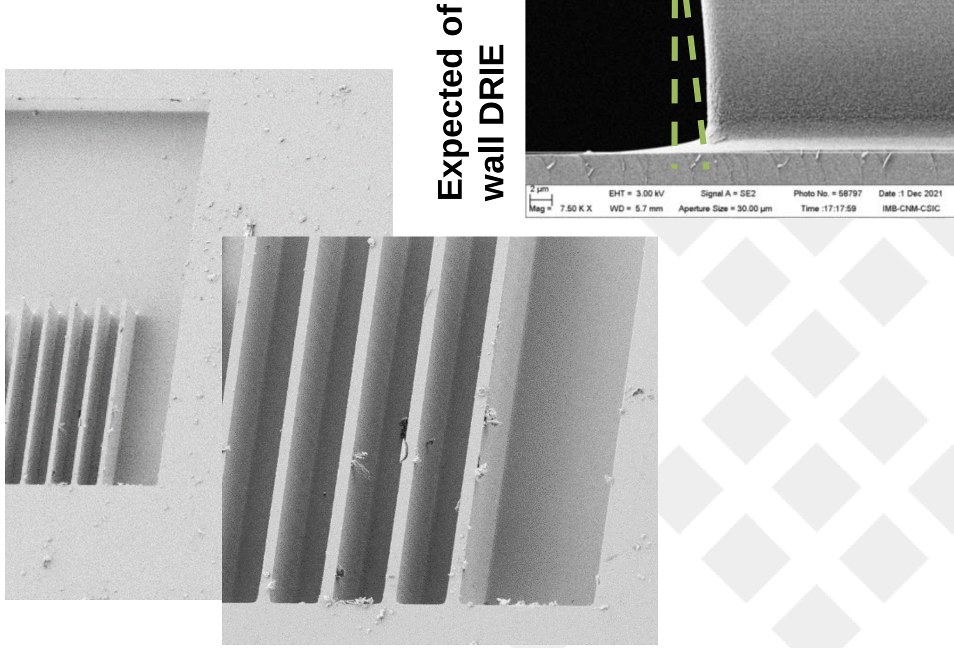
- Thinner pillar width -> More charge multiplication
  - Currently limited by lithography
  - Trying to reduce distance across pillar base to reduce distance between electrode sides -> Inverted pyramid profile
- Over-etching in the first batch (25 um instead of 8 um)
  - Adjust recipe

Next steps

- Metallisation and oxide deposition tests (~1-2 months)
- Production (~end-of-year)

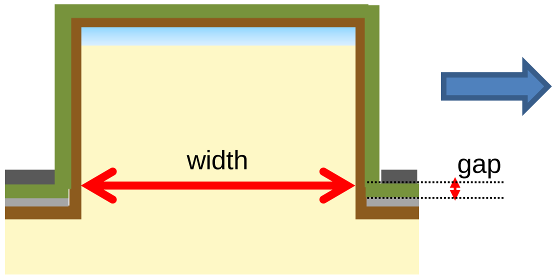


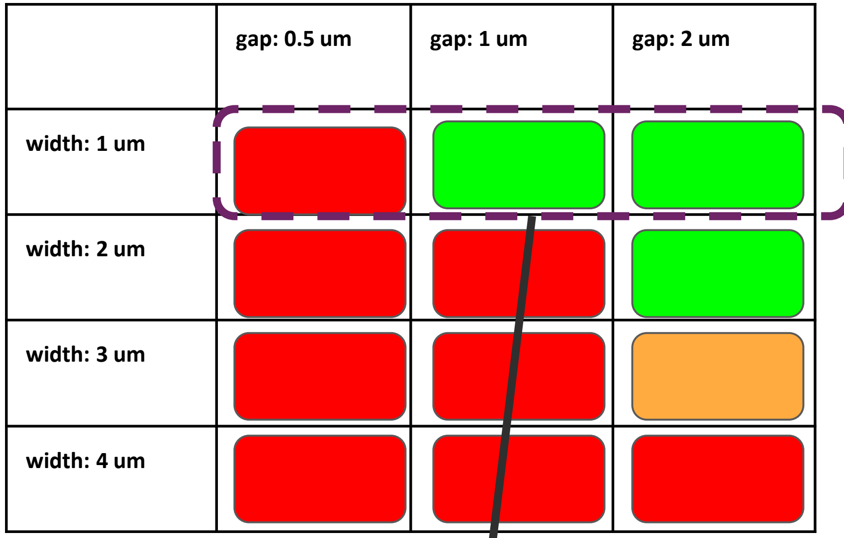




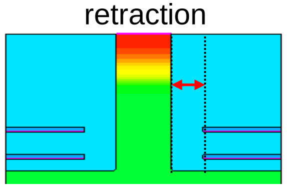
Device simulation

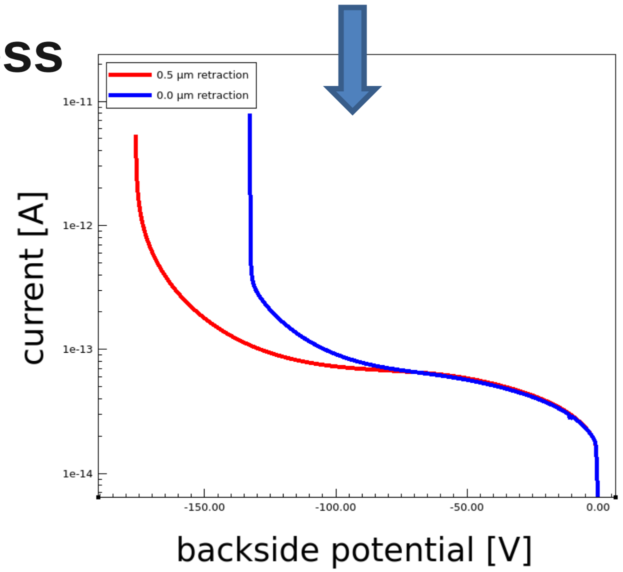
- **Geometry adapted to the real production process**
- **Specific geometrical constraints**
    - width of the amplification pillar
    - gap between amplification electrodes
    - distance between pillar and electrodes
- **Study with TCAD simulation of geometry compatible with process**
    - IV used to check if amplification happens before breakdown (checked with transient sim.)
    - best for low width and high gap
    - width limited by lithography and gap limited by oxide deposition
    - retraction of the electrode from the pillar still allow amplification



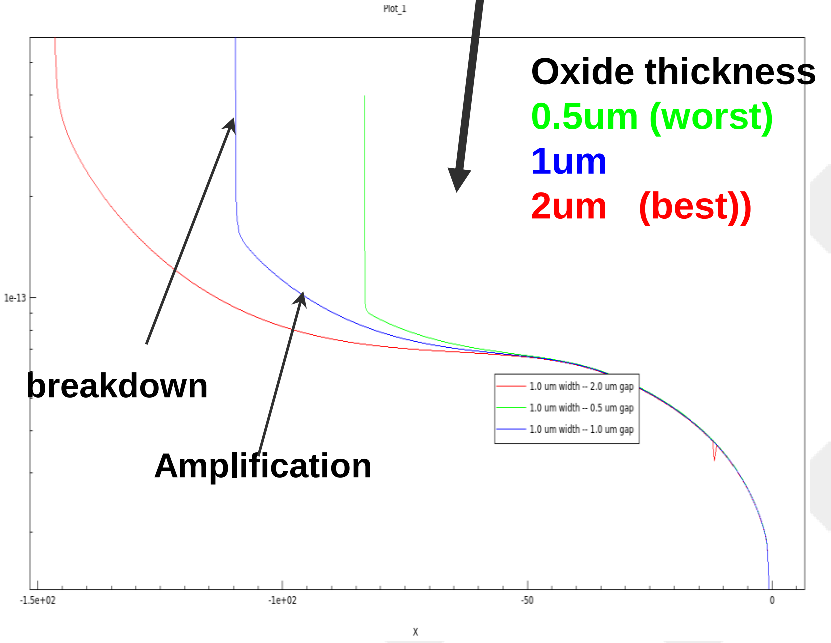


	gap: 0.5 um	gap: 1 um	gap: 2 um
width: 1 um	🟥	🟩	🟩
width: 2 um	🟥	🟥	🟩
width: 3 um	🟥	🟥	🟧
width: 4 um	🟥	🟥	🟥





Simulated IVs with different electrode retraction



Oxide thickness
0.5um (worst)
1um
2um (best))

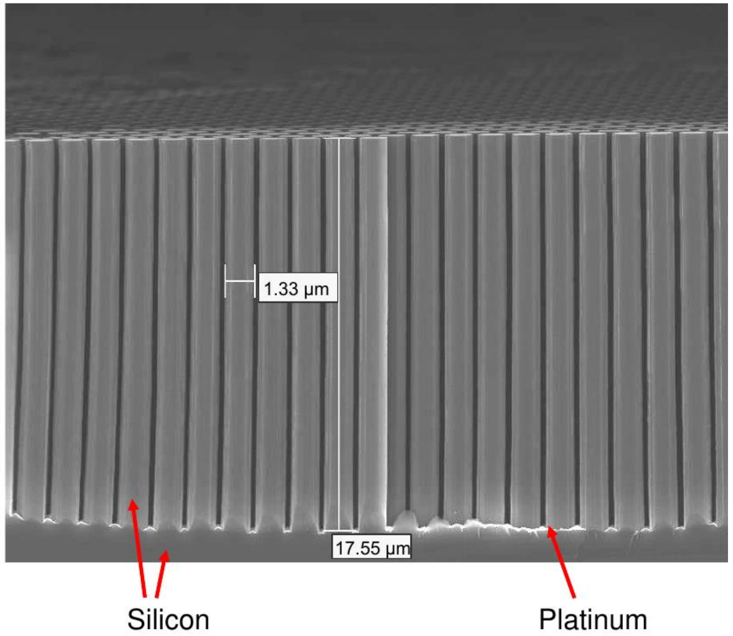
Simulated IVs with different gaps

Alternative approach to SiEM

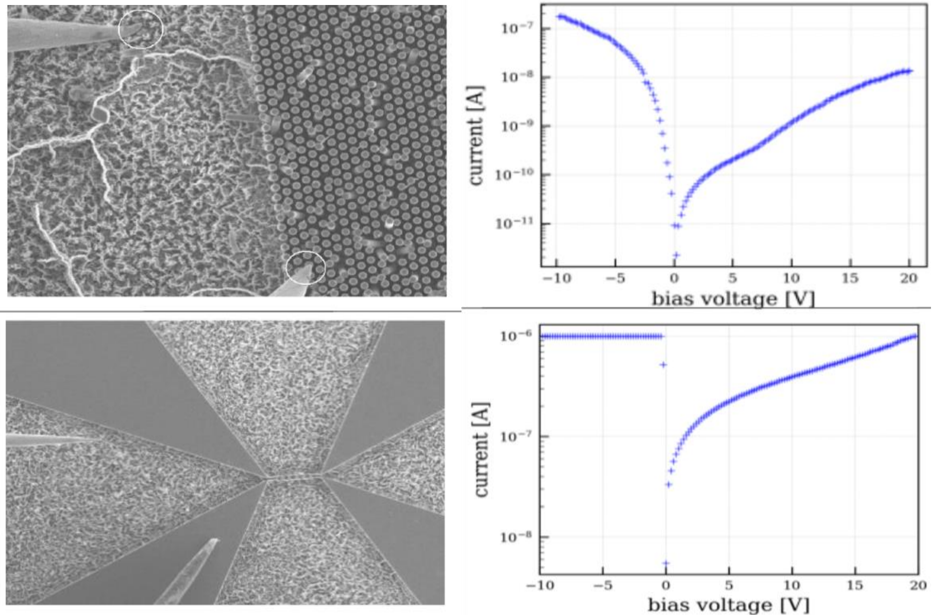
- **Study possible use of Metal assisted etching**
  - parallel project between CERN and PSI, based on AdEM 22 (2020) 2000258
  - very different process constraints (cheap, high aspect ratio, first electrode deposited while etching), but never used in active device

- **Testing the structures**
  - IV just after production with probe-station ⇒ pn junction conserved
  - bonding of test structures for IV in the lab
  - preparing setup for laser/ source test.

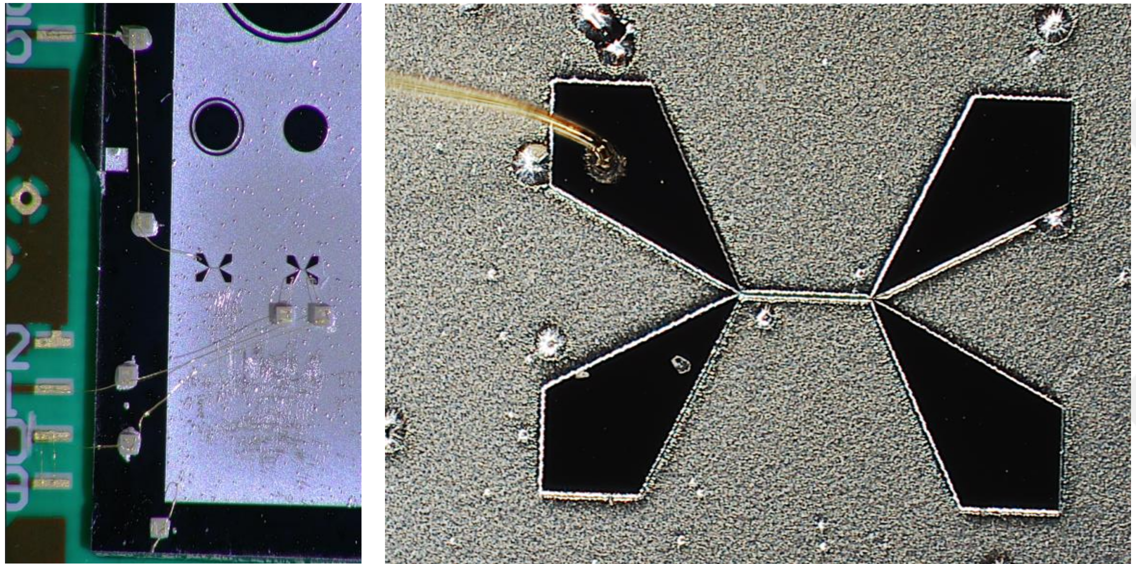
see M. Halvorsen @ RD50 41st workshop



Pillar made with MacEtch process



IV measured under SEM after prod.



Strip structure bonded for testing

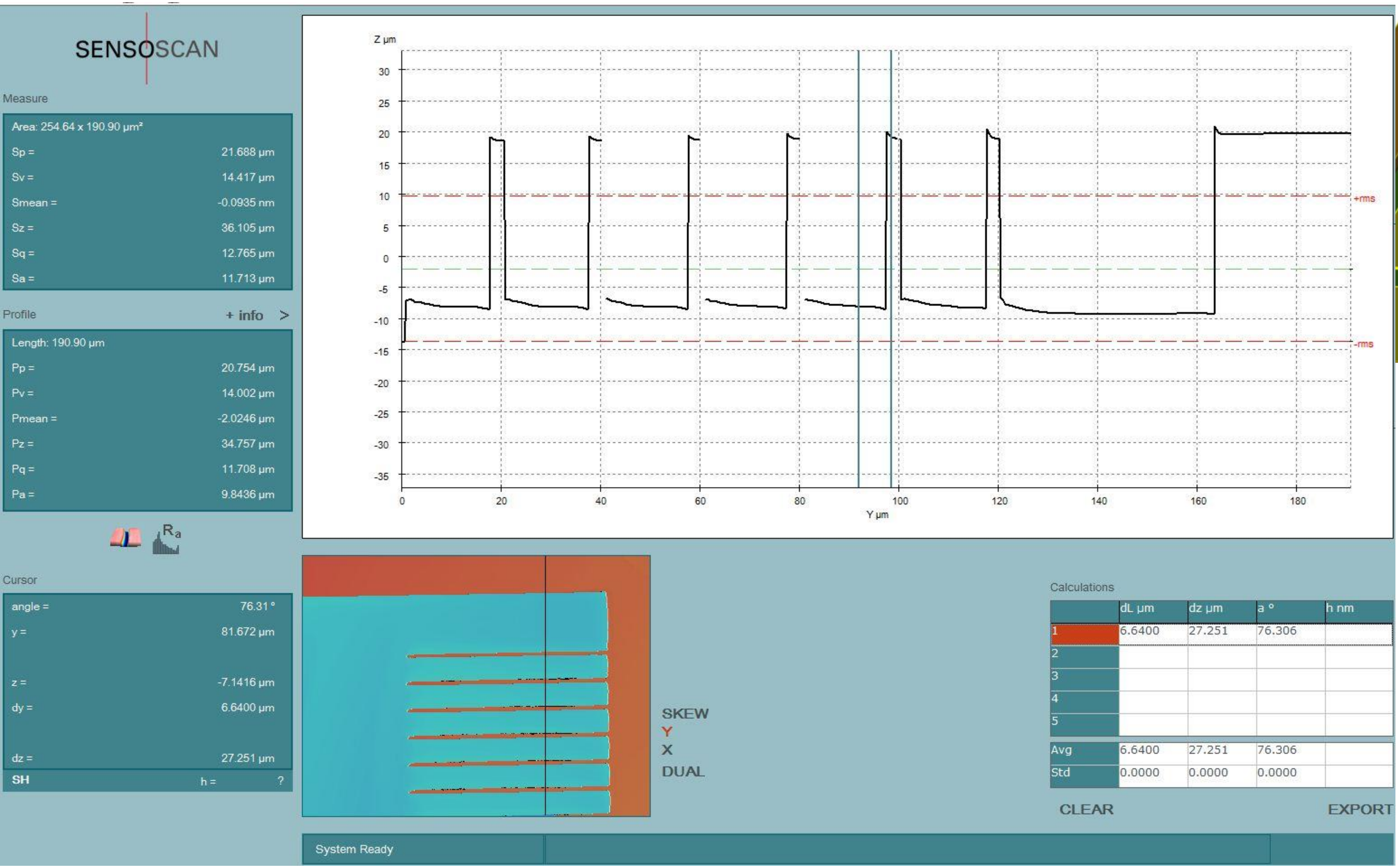
Summary and outlook

- Electron Multiplier concept on Silicon Radiation allows charge multiplication not relying on high doping implantation
  - Mechanism depends on geometry only -> not sensitive of acceptor removal
- First processing tests being performed for the fabrication of demonstrator
  - RIE, laser lithography, oxide and metallisation
  - Exploring inverse pyramid profile to reduce pillar width (to overcome the limit on pillar width, limiting charge multiplication according to simulation)
- Simulation being updated to match CNM processes
  - Inter-electrode gap and pillar width, different dielectrics, etc

Fabrication and simulation interplplay

- Alternatives approaches to the SiEM geometry being studied by means of metal-assisted etching

Back-up



Measure

Area: 254.64 x 190.90 µm²
Sp = 21.688 µm
Sv = 14.417 µm
Smean = -0.0935 nm
Sz = 36.105 µm
Sq = 12.765 µm
Sa = 11.713 µm

Profile

Length: 190.90 µm
Pp = 20.754 µm
Pv = 14.002 µm
Pmean = -2.0246 µm
Pz = 34.757 µm
Pq = 11.708 µm
Pa = 9.8436 µm

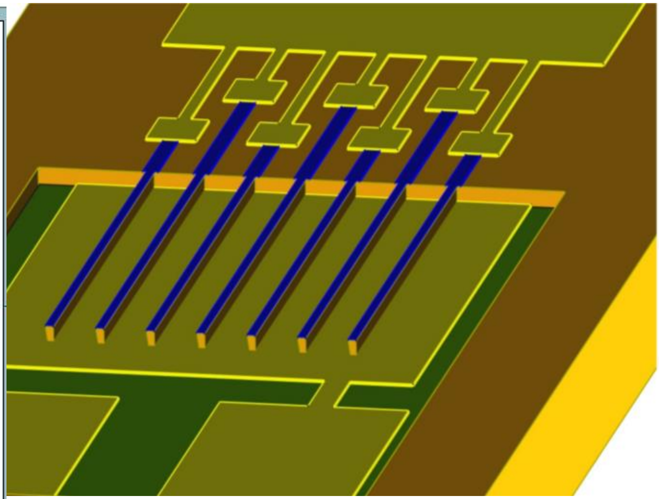
Cursor

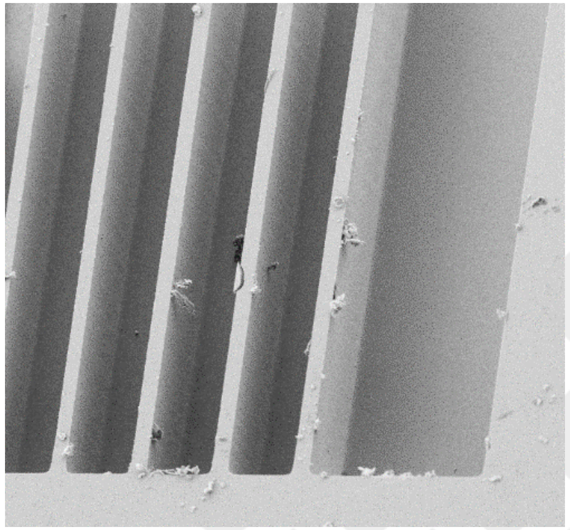
angle = 76.31 °
y = 81.672 µm
z = -7.1416 µm
dy = 6.6400 µm
dz = 27.251 µm
SH h = ?

Calculations

	dL µm	dz µm	a °	h nm
1	6.6400	27.251	76.306	
2				
3				
4				
5				
Avg	6.6400	27.251	76.306	
Std	0.0000	0.0000	0.0000	

System Ready

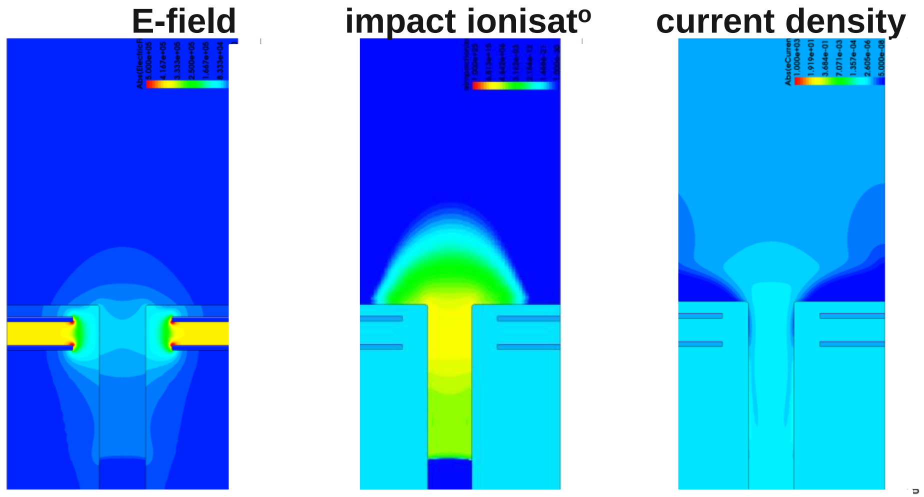




Electric Field

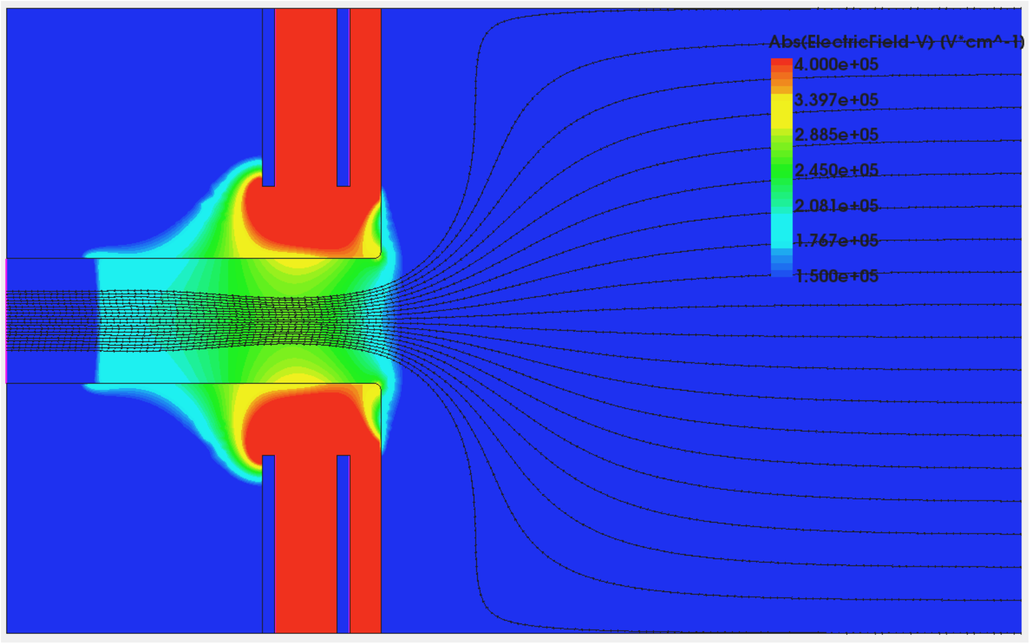
and leakage current

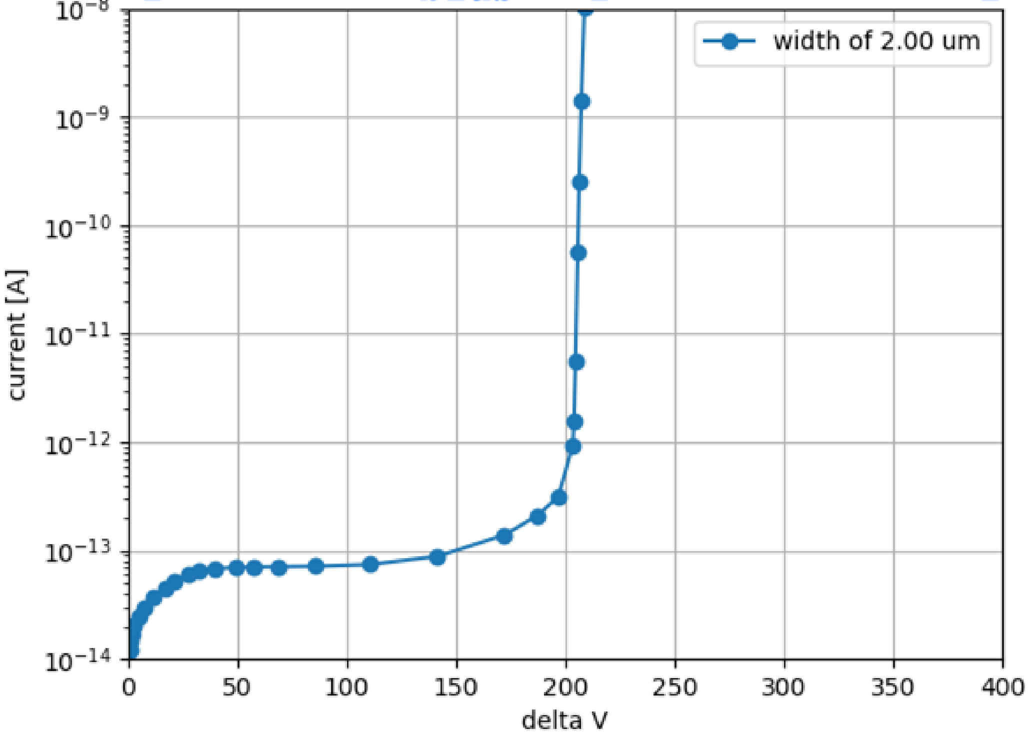
- **The bulk can be depleted**
  - low leakage current
- **High field region can be achieved**
  - between 200 and 300kV/cm
  - field in dielectric < 3MV/cm



$V_1 = -5V,\ V_{bias} = V_2 - 30V,\ \Delta V = V_1 - V_2$

ΔV = 140V





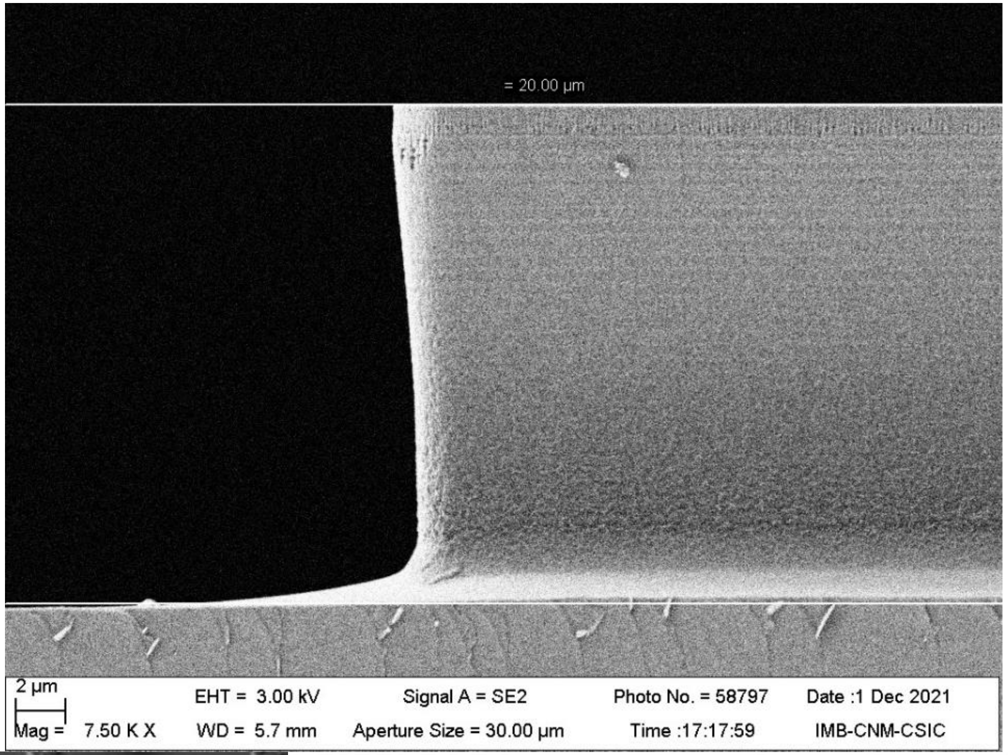
Design rule determination
Activity [1] @ CNM

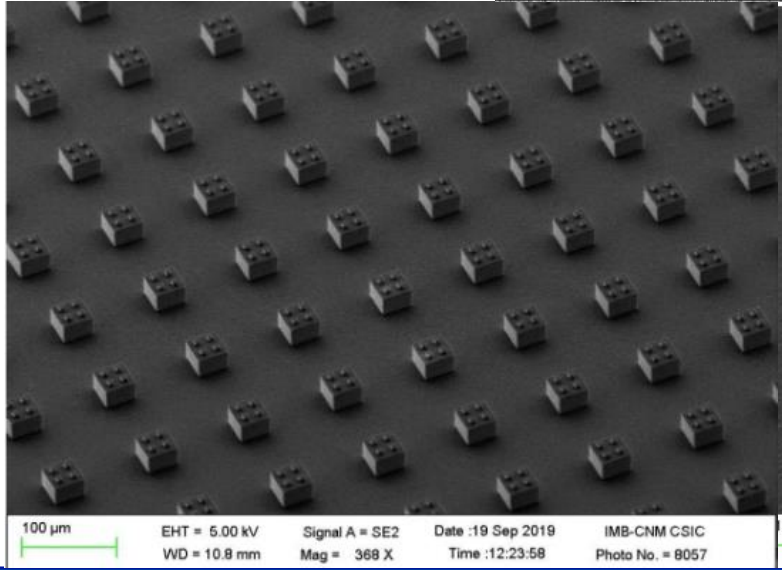
- **Structures with various:**
    - pillar width (1-5µm)
    - inter-pillar distances (2 to 5x pillar width)
    - depth (6-10µm)
    - guard between elect. and pillar (0.25 to 1µm)
    - inter-electrode distances
    - various DRIE parameters

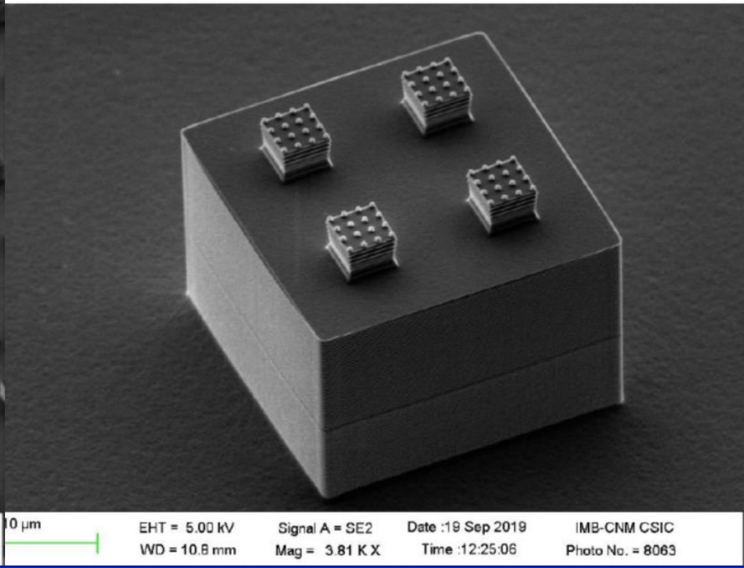
- **Process simulation**
- **Tuning to CNM device parameters**
- **Production of the structures**
- **Characterisation of the topologies**

Question
Tech. 1

1µm pillar OK but large structure of 1µm pillar will require dedicated dev. (beyond this project)







Technology demonstrator
design, production and characterisation [2,3,4]

- **Design and optimisation of a demonstrator @ CERN**
    - ~200 x 200 μm active region
    - to be readout by discrete electronics
    - Optimisation of the geometry, including design rules

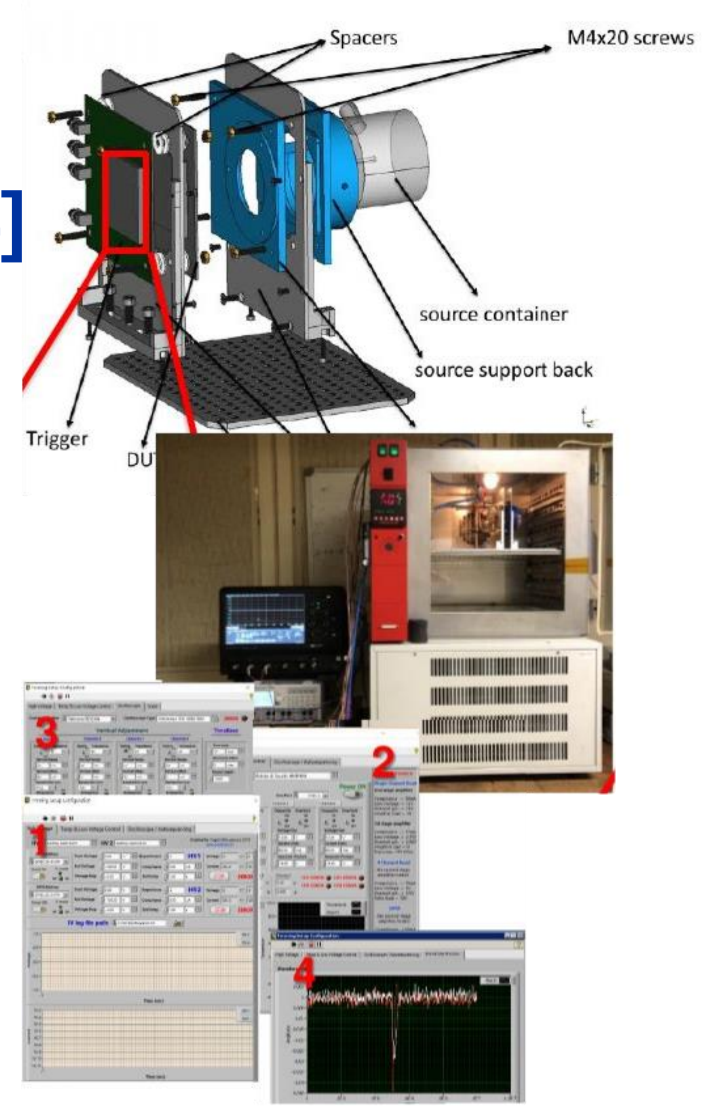
TCAD Tools in place already, Garfield++ simulation for MIP response on-going

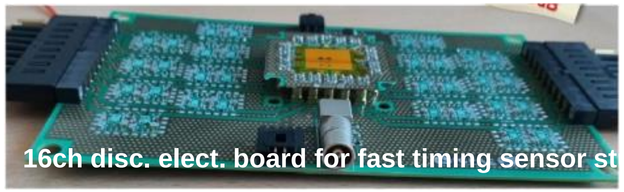
- **Production of a demonstrator @CNM**
    - mask design
    - structure production

Process prototyping done during activity [1]

- **Characterisation of the demonstrator @CERN**
    - IV, CV,CCE and time resolution measurements with Sr90 source
    - irradiation @ IRRAD (10^{14}, 10^{15}, $10^{16} n_{eq}/cm^2$)
    - post-irradiation characterisation

Characterisation suite from CERN EP R&D WP1.1




16ch disc. elect. board for fast timing sensor st

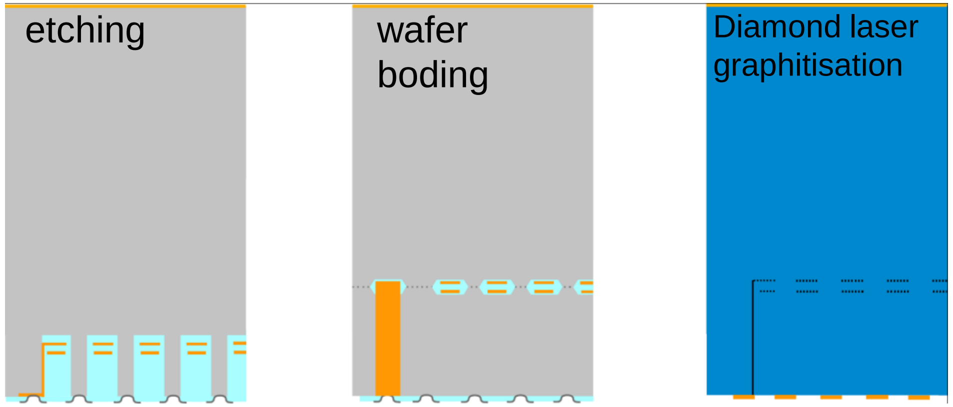
Technology investigation
and roadmap document [5,6]

- **Different sensor geometry**
  - single electrode
  - stack of electrodes
- **Different bulk material (SiC, Diamond,...)**
  - higher radiation hardness, lower charges fr ionisation
  - could be compensated by achieving gain
- **Different process**
  - MacEtch: less production ready but simple and different contraints (parallel project with PSI)
  - Wafer bonding: more complex but different constraints
- **Hardware implementation are beyond the scope of this project**

Question Tech. 3

Question Tech. 6

Roadmap document to prepare the next R&D steps and other applications



[L. Romano *et al*; AdEM 22 (2020)