Integration aspects of highly granular calorimeters
WP8 T2.1

Vincent Boudry

LLR, **Institut Polytechnique de Paris**

for

CERN, CNRS-IJCLab, CNRS-LLR, CNRS-LPNHE,
DESY-HH, FZU, JGU, TAU
materials from Y. Benhammou, J. Kvasnicka, J. Nanni, J. Maalmi, *et al.*

AIDAinnova 2nd Annual Meeting
25/04/2023, Valencia

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

WP8 Task 8.2/1

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

Task 8.2.1 Towards next generation highly granular calorimeters

Task 8.2.1

- Development of a common electromagnetic and hadronic calorimeter data concentration interface for minimised space and power consumption
- Demonstrator with functional active detector elements and full read-out chain

Integration aspects of highly granular calorimeters

Highly granular electromagnetic and hadronic calorimeters at future colliders will have up to 10^8 readout cells, calling for common solutions for services such as data concentrators interfacing the embedded front–end electronics and the data acquisition outside the detector.

⇨ *This subtask will develop **compact and innovative data concentrator and power distribution units**, serving more than 10^6 cells and satisfying the tightest space and power constraints.*

⇨ *The technical solutions will be embedded in **a demonstrator** that will be **applicable** to particle physics detectors at future e+e− colliders such as ILC, CLIC, CEPC, FCC-ee.*

*For this demonstrator, mechanical structures and silicon and scintillator **based active elements will also be provided***

Specifications for a “CalAiDAQ”

Technical specifications for common DAQ interfaces

- based on CALICE SiW–ECAL SL Board v2:
  Update of AIDA-2020 Deliverable during AIDAinnova

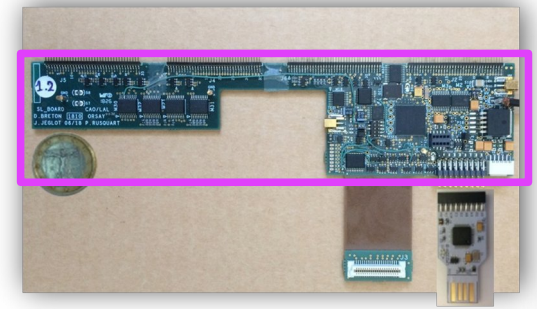
List of Relevant questions for adaptation to CALICE AHCAL

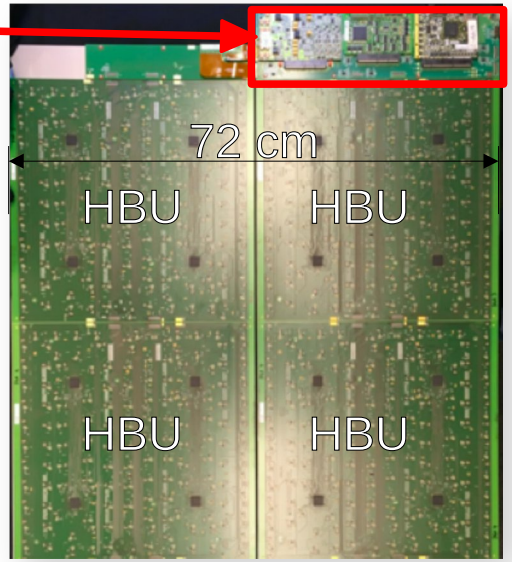
identified in 3 meetings, ⊃ 2 physical side-meeting @ CALICE

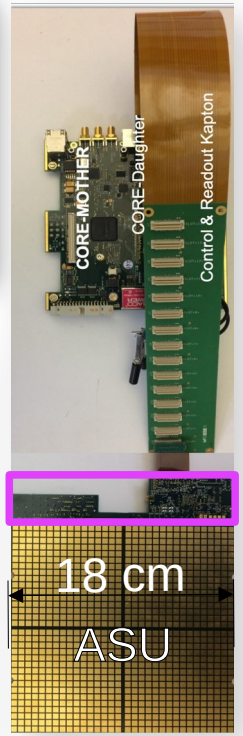
- Central Interface Board for AHCAL have to be reduced : 10 cm ➞ 6–7 cm
- Power board (ASIC, SiPM, LED pulsing) may stay as a mezzanine
  - Can the Power pulsing integrated on AHCAL Board ?
- Signal transmission via “CORE Kapton” not feasible (length, and not needed)
- HDMI cables still optimal, also since five differential pairs
- AHCAL may consider combining functionalities in FPGA

Some improvements for SiW-ECAL (implemented):

- Add an analogue line for VFE board monitoring
- Add a single wire protocol for temp & ID device (Battery chip)







Beam Tests (28/3–4/4)

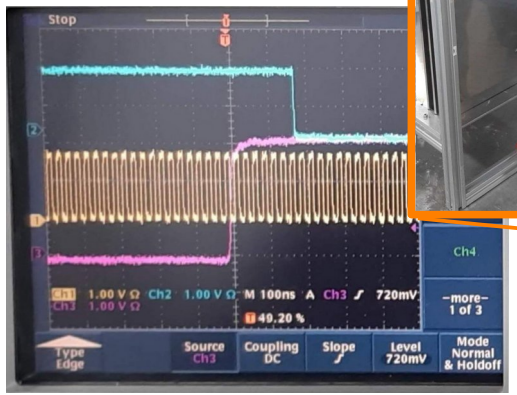
The measurements leading to these results have been performed at theTest Beam Facility at DESY Hamburg (Germany), a member of theHelmholtz Association (HGF)".

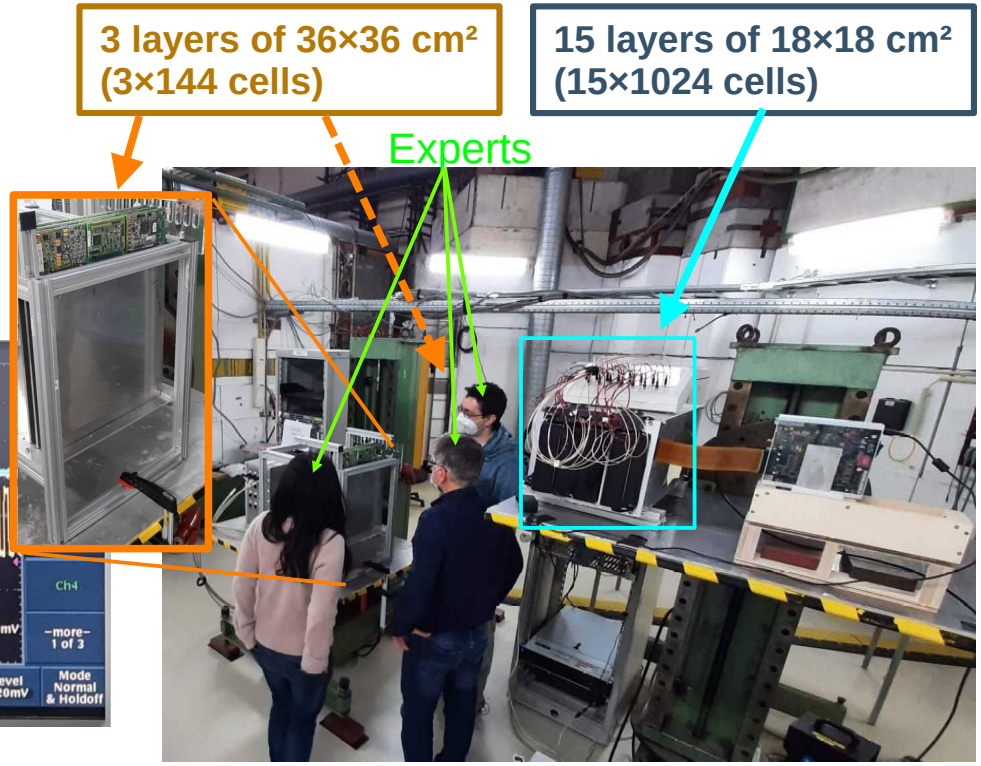
3 layers of AHCAL + 15 layers SiW-ECAL

- 2 Acq Systems
  - Same frequencies (40/5 MHz, ~100 Hz)
  - Same Logic (Self-trigger, local storage, delayed readout)

Synchronisation:

- Hardware: CALICE CCC
  - Clock, StartAcq, Busy
- Software: AIDA EUDAQ
  - Start/Stop Run,
  - common + indiv data streams
  - Monitoring



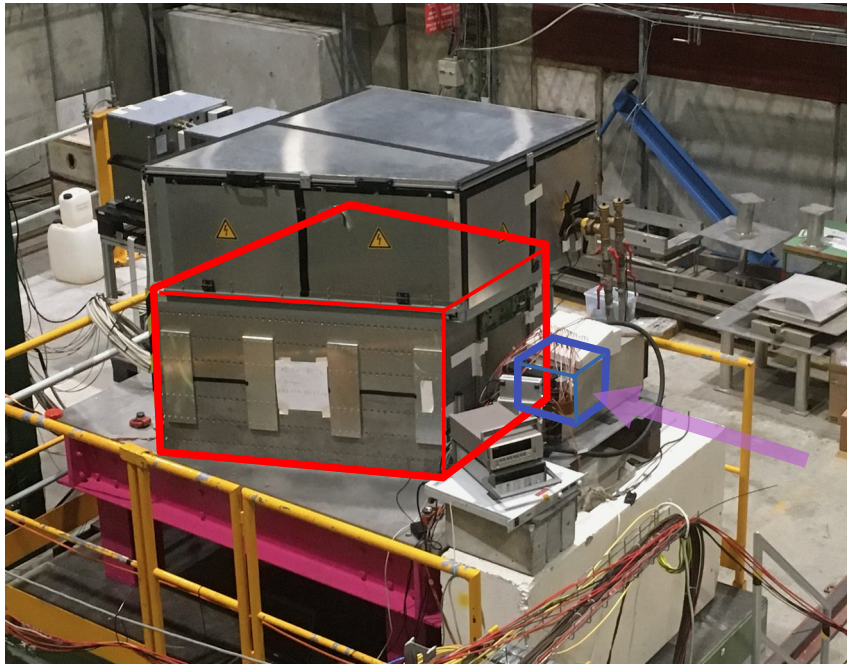


➡ **mips (punch-through electrons) coincidences in time / position**

Beam Test (08/06–22/06)

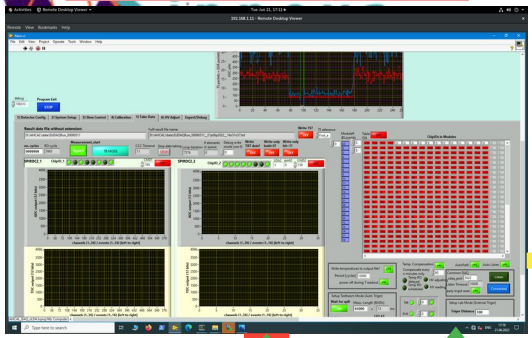
“Full” SiW-ECAL + AHCAL

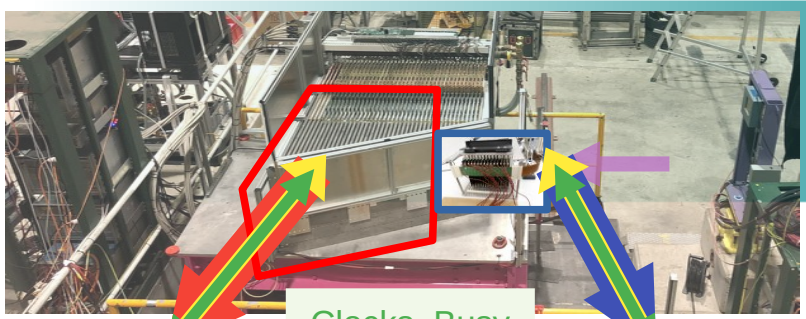
AHCAL :
- **38 layers 72×72 cm²**
- 3×3 cells scintillator + SiPM
- 1.7 cm Stainless Steel (~4λ)
- **6t, 1×1×1.5 m³**



SiW-ECAL
- **15 layers 18×18 cm²**
- **0.5×0.5 cm² Si cells**
- **2.8+5.6 mm W (24 X_0)**
- **100 kg, 0.4×0.4×80 cm³**

AHCAL LabView





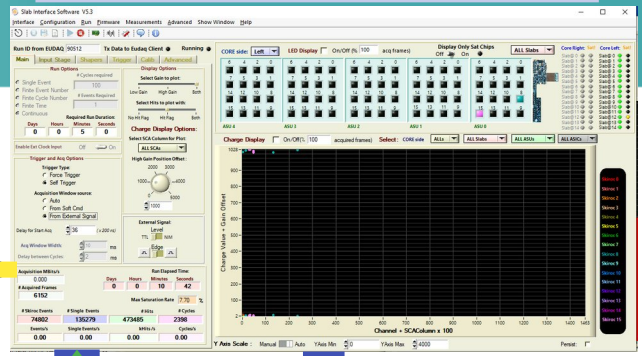
Clocks, Busy

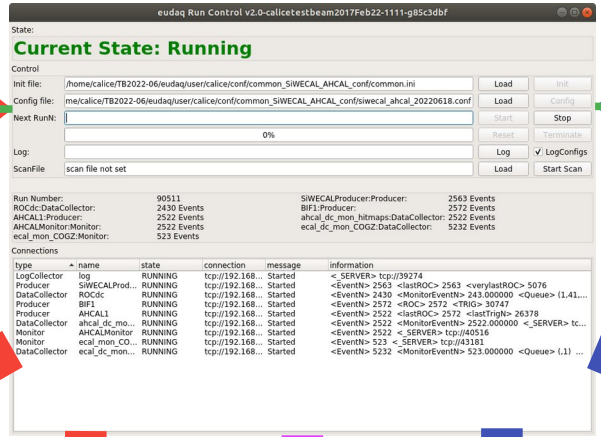
LDA ↔ CCC ↔ CORE

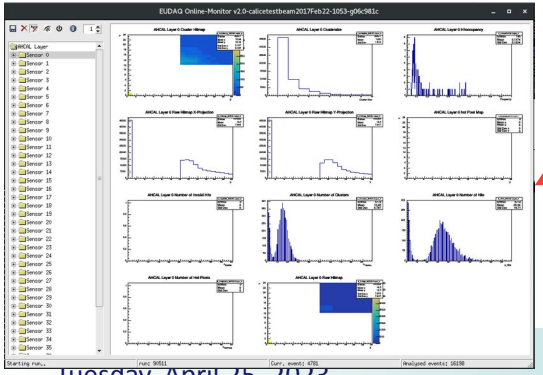
Command

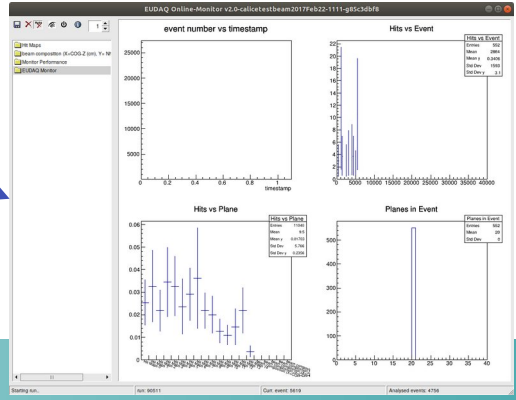
Configs

SiW-ECAL LabWindows





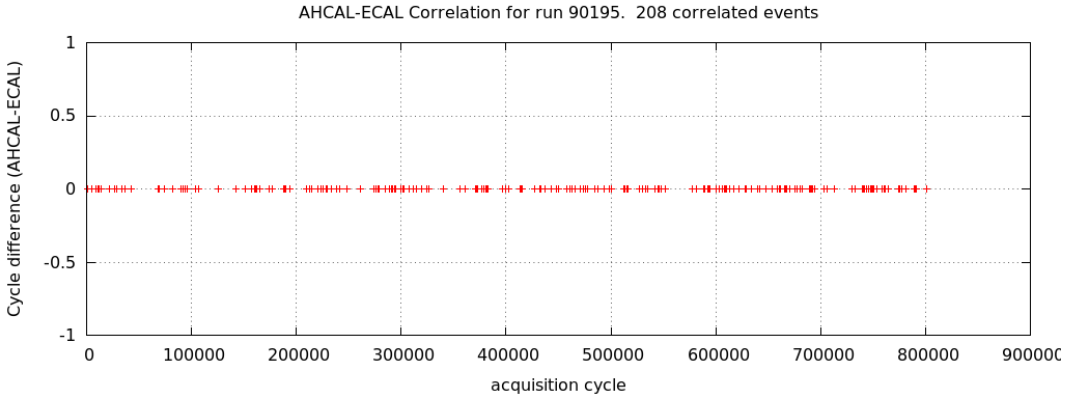




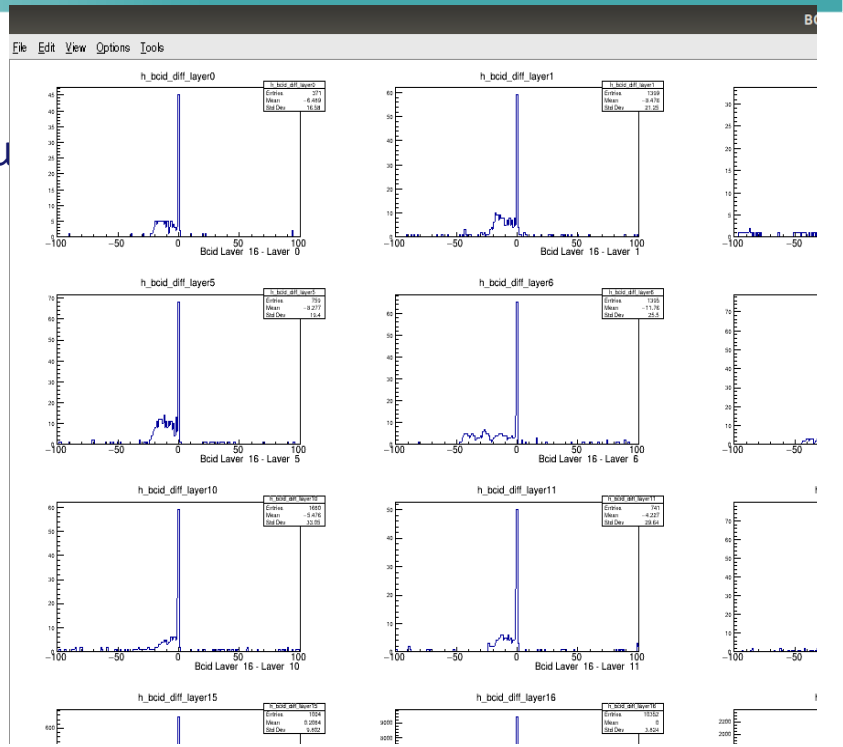
Synchronization

Offline synchronisation checks

- identical BCID corrected for fixed offset

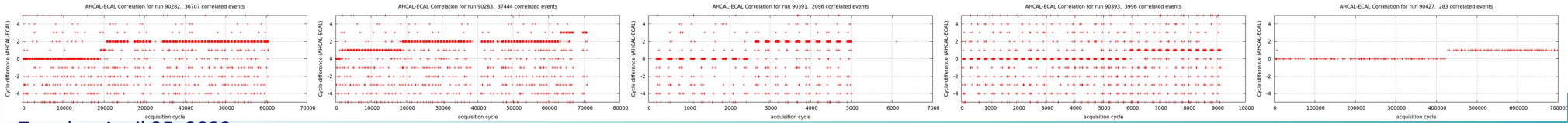


on μ



Some (rare) desync. : couple of runs / 500+

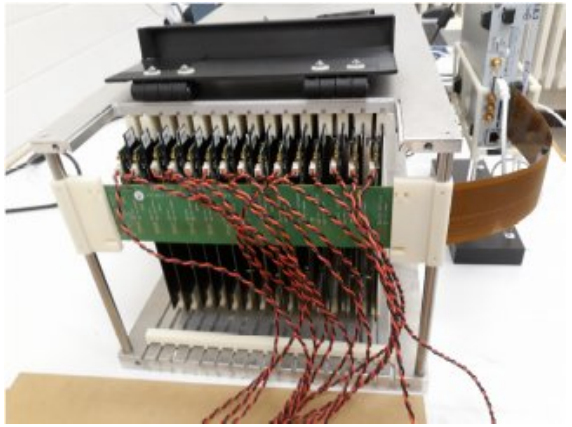
- probably due to one faulty connector

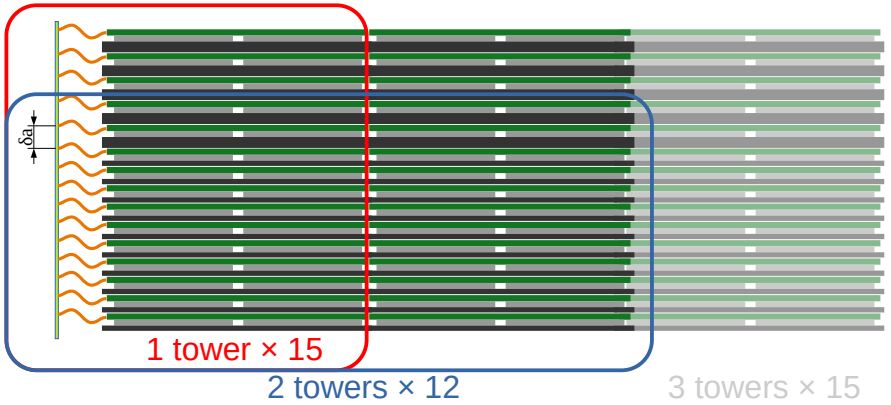


Building of a uniform SiW-ECAL prototype

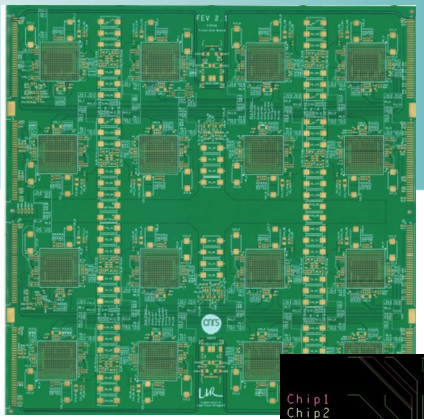
Rationale:

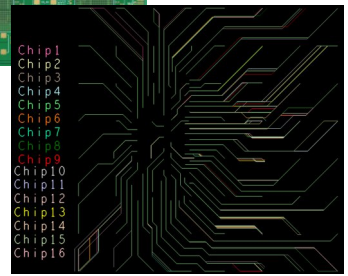
- Current prototype
  - 4(5) types of PCBs ⊗ 3 sensor thicknesses (320, 500, 625 µm)
  - (un)gluing issues
- Material for 15 ASUs available ➞ full single tower
  - FEV2.1 boards, wafers, components
- Application cases :
  LUXE@XFEL, EBES@KEK, Lohengrin@ELSA
  - Extreme QED & Dark *γ* searches
  - low energy, rates, …
  - LUXE: FCAL prototypes ➞ common DAQ Application.
  - Could be built from *same cards* in 2×12
    - Needs: sensors (€), (Mech. structure), W

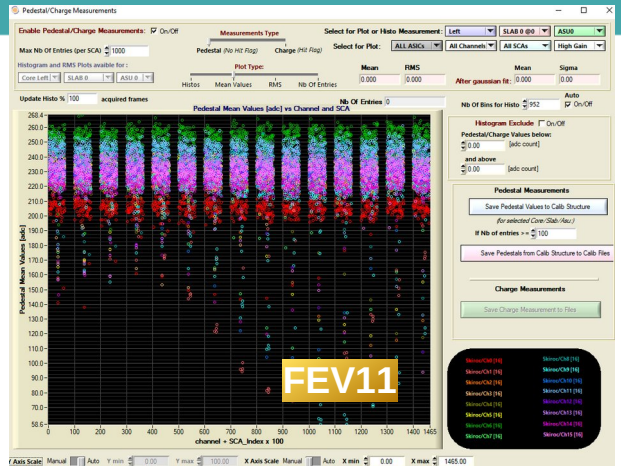




New FE boards







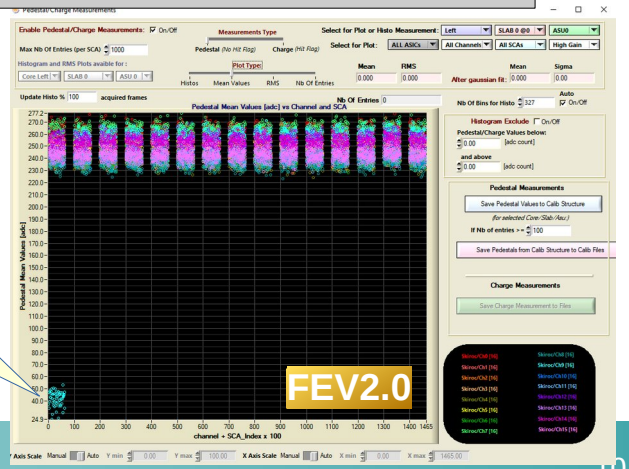
Pedestal measurements vs. Ch# + Mem#×100)

Improvements:

- Power distributions
  - Local power regulation: LDO's
  - Local High Voltage filtering & Supply
- Signal distribution (buffering), data paths
- Monitoring (single ID, temp, probe analogue line)
- ASIC shielding/routing

Status:

- pre-version 2.0 tested, minor corrections needed
  - Noise uniformity dramatically improved (ex: outliers in thr. / 20 !)
- version 2.1 produced, … in metrology
  - before cabling, 2nd metrology, gluing, …
  - All material available : ASICs being tested

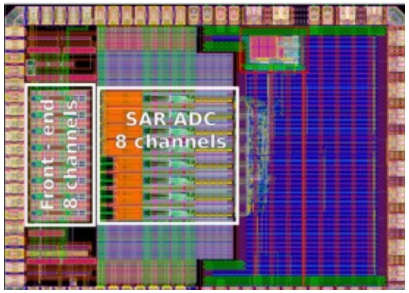


SIngle channel → the fault on the ASIC/packaging

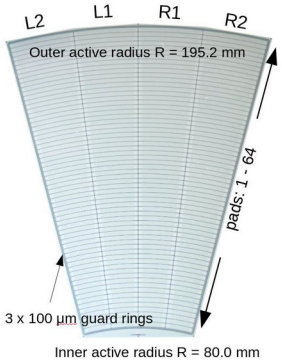
Compact calorimetry

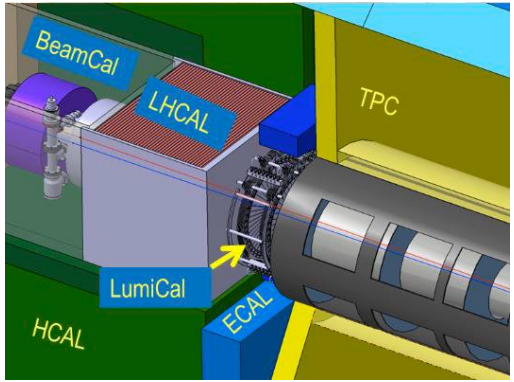
LumiCal (FCAL collaboration)

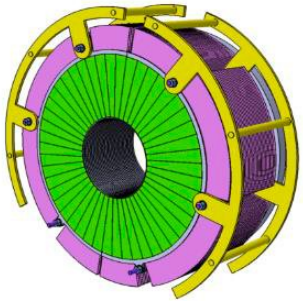
- 320 µm sensors by Hamamatsu
- Beam test with FLAME ASICs:
  - **FcaL Asic M**ultiplane r**E**adout



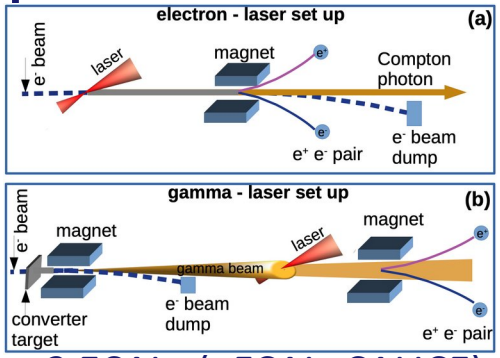
UST Krakow

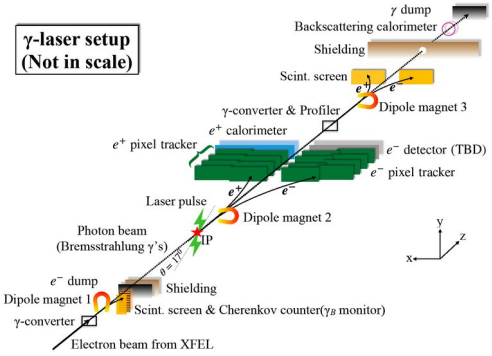






Application for the LUXE experiment (2025+?)



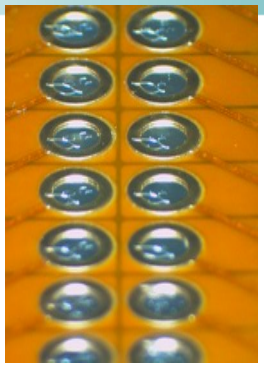


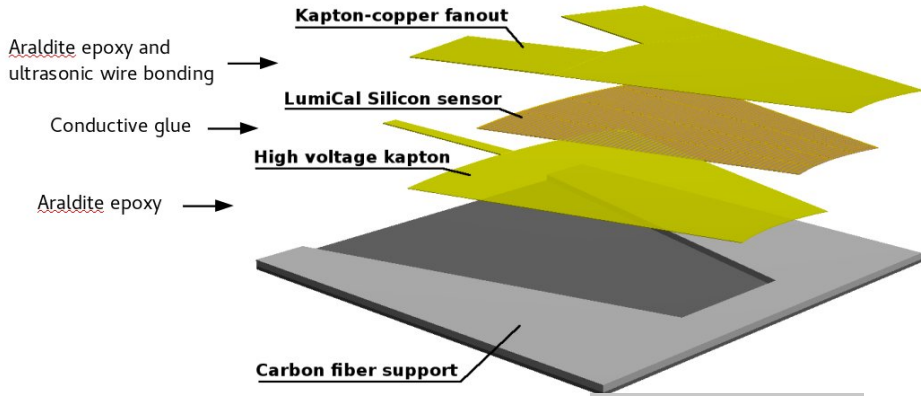
- 2 ECALs (~FCAL, CALICE) + EuDAQ ?
  - Collab on DAQ, sensors, integration...

FCAL/LUXE integration

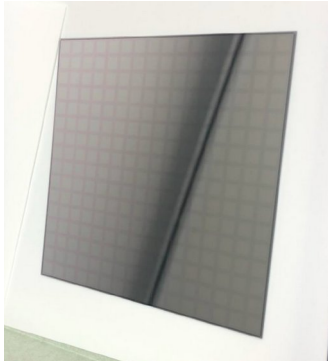
Bonding vs Gluing vs AFS

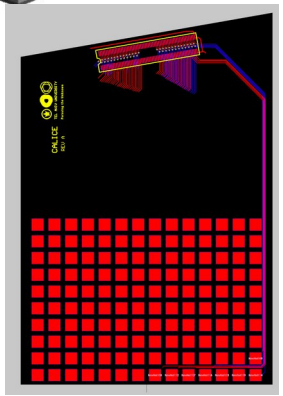
- Bonding: loop size & fragility





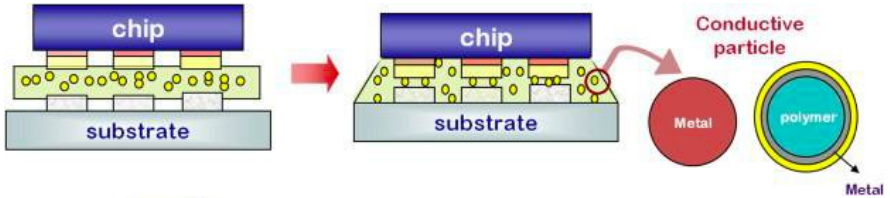
- Silver glue (*à la* CALICE)
  - tested on 4 CALICE-like wafers and ad-hoc fanout



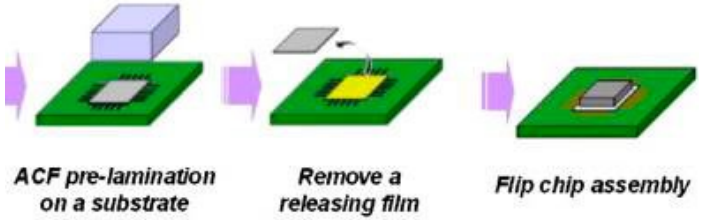


Anisotropic Conducting Film (ACF)

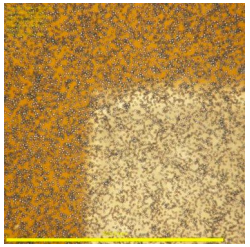
- **Anyisotropic conductivity :**
  - along z only

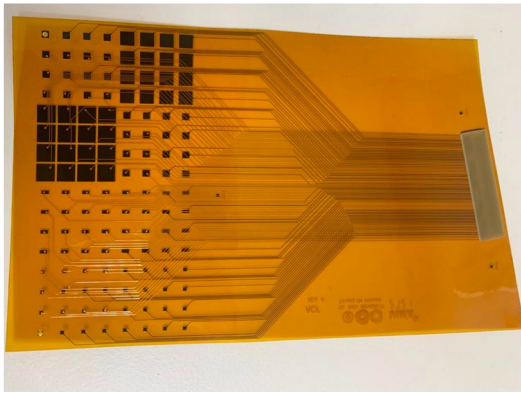


- **require pressure and heating**



- **Test set-up:**
  - flex with various pad size ⬌ CALICE sensor
    - Y. Benhammou (TAU) + M. Pinto (U. Geneva)
  - 2 types of ACF:
    - 3M – 50 µm
    - Dexerials – 3 µm after curing
  - Performances under evaluation



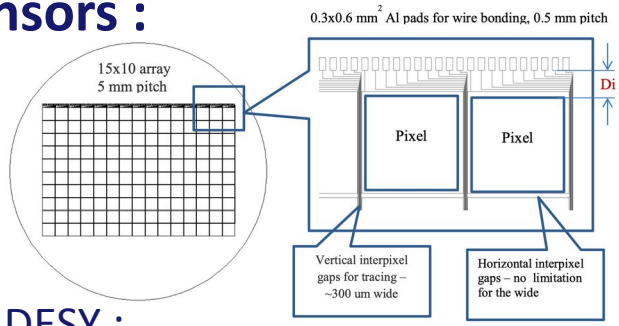


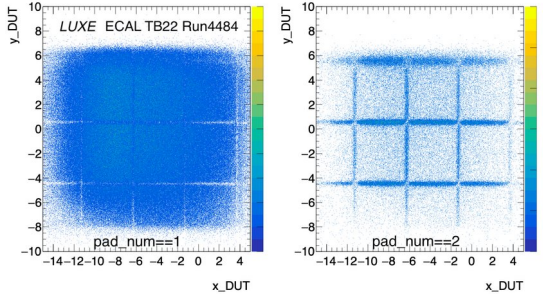
see also Status of ACF in WP6

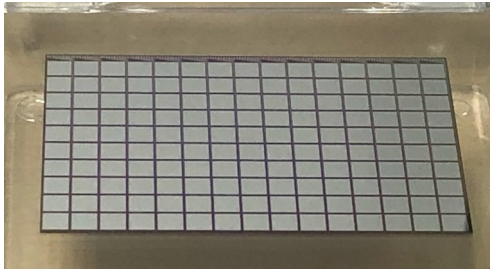
Other integrations

Readout line in sensors :

- 500µ AsGa
- 2021
- Bonding
- Tested in 2022 at DESY :
  - signal, cross talk, noise,…
  - Preliminary result promising

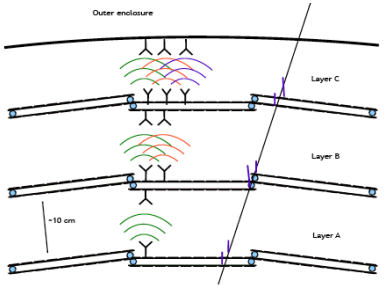






R&D on wireless transmission

- WADAPT collaboration
  - mockup detetor & transmission chip
  - transmission between layers
- Work :
  - Antennas
  - update existing chips



see pres of D. Dancila, *et al.*
Wireless Data Transfer for High-Energy Physics Applications, report in WP13

Publications

SiW-ECAL

- New results from the technological prototype of the CALICE highly-granular silicon tungsten electromagnetic calorimeter
  Pisa'22 NIM A 2023, 168185 [arXiv:2211.05614] (AiDAinnova)
- The CALICE SiW ECAL Technological Prototype -- Status and Outlook
  CALOR'22 Instruments 2022, 6, 75 [arXiv:2211.07457] (AIDAinnova)

to be loaded on AIDAinnova Zenodo…

FCAL

- Very forward calorimeters for future electron-positron colliders
  Lepton Photon'22 doi:10.5281/zenodo.6784018 [Arxiv:2301.09423] (AIDA-2020)
- Compact LumiCal prototype tests for future e+e− colliders
  PSD12 JINST 17 (2022) 07, C07024 [Arxiv:2112.01816] (None)

Common DAQ operations:

- 1st operation SiW-ECAL (15 layers) + AHCAL (3 layers) @ DESY: low-E electrons as mips **March 22, 2022**
- 2nd operation SiW-ECAL (15 layers) + AHCAL (38+1 layers) @ CERN: High-E e, μ & π **June 22, 2022**

MS30 publication: *Conceptual design and technical specifications of DAQ interfaces for highly granular electromagnetic and hadronic calorimeters*

Integration in FCAL and Application to the LUXE calorimeters (in the making)

- Compact calorimeters connections: ACF, Line on Sensor, (Wireless DAQ)
- Possible use the SiW-ECAL CALICE calorimeter together with the FCAL-type one
  - With news boards (FEV2.1)
- DAQ integration using EUDAQ → perfect case for this task
  - XFEL beam ↔ ILC beam : design conditions for VFE chips