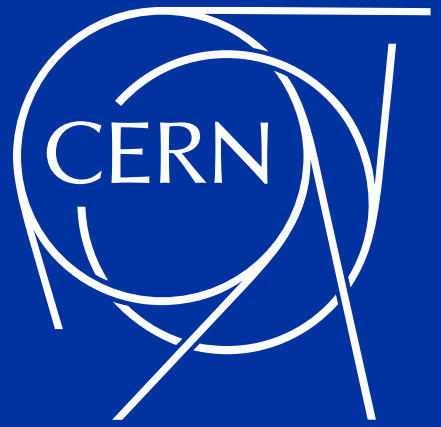


POPS Operational Issues during October 2022

Joint Accelerator Performance Workshop December 2022

Aramis Schwanka Trevisan and Fulvio Boattini (SY-EPC/HPC)

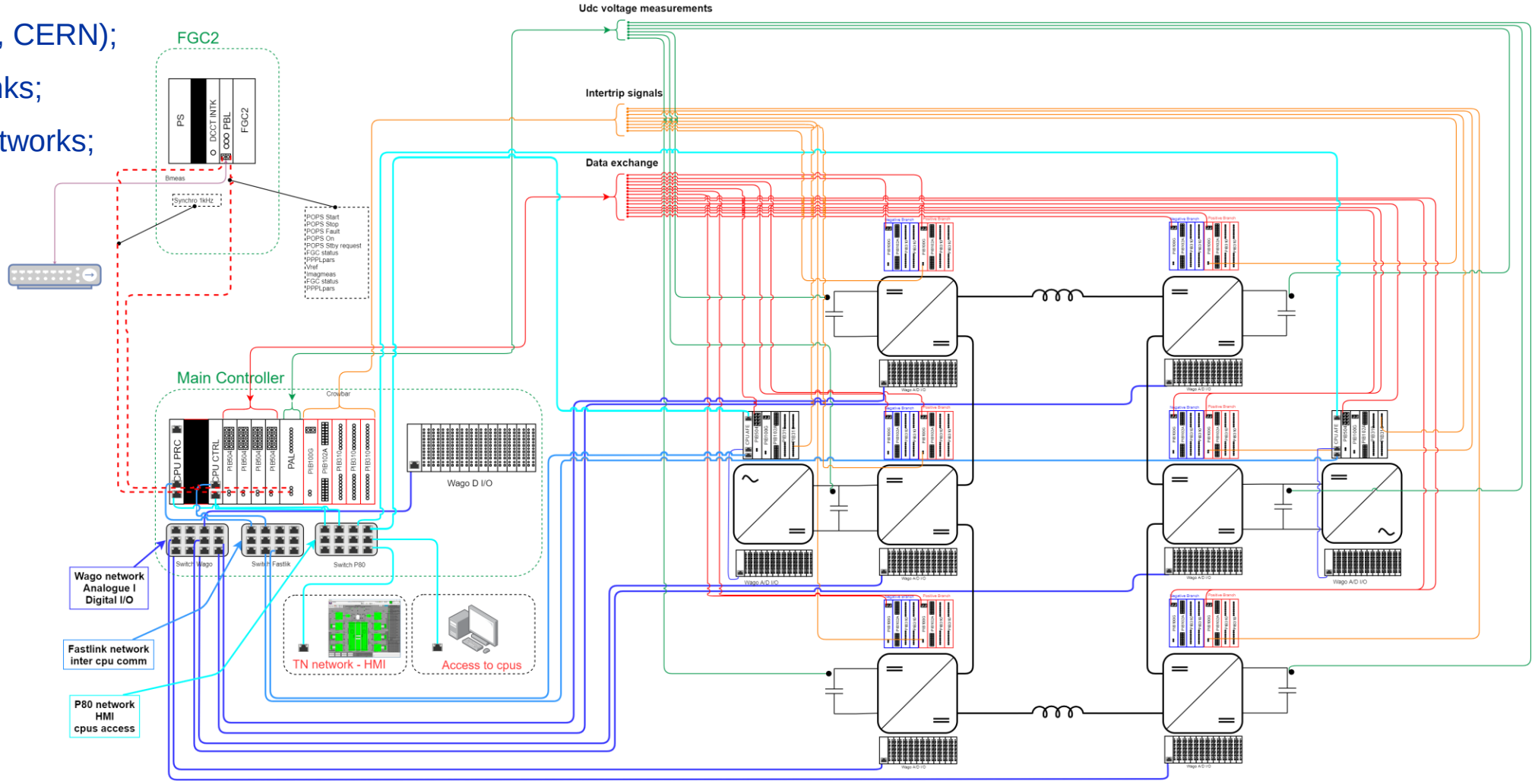
Date: December 7th , 2022

Agenda

- POPS controller: a quick overview
- Chronology of the Mad October event
- Problem solved
- A look at the statistics
- What’s next
- Conclusions

POPS control

- POPS control is structured with 8 power converter control crates (GEPC);
- 1 centralized Main Controller (MC) (GEPC);
- 1 FGC controller (Type 2, CERN);
- Data exchange optical links;
- Data exchange RG45 networks;

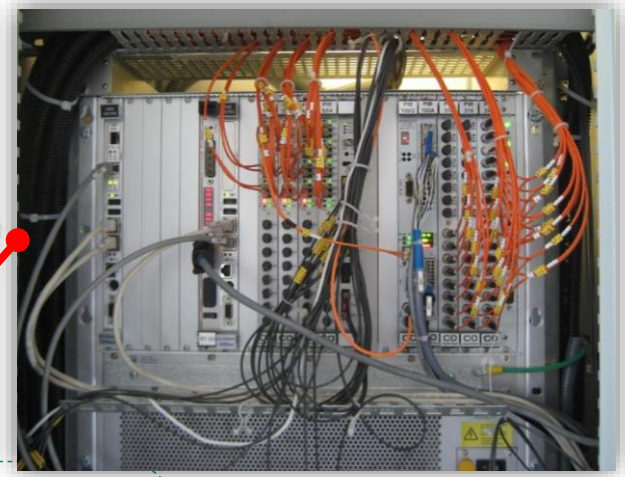


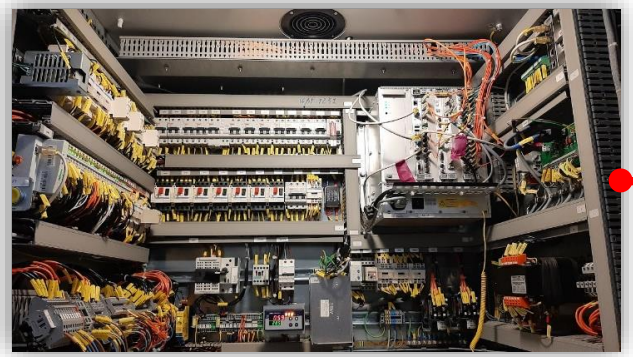
POPS control

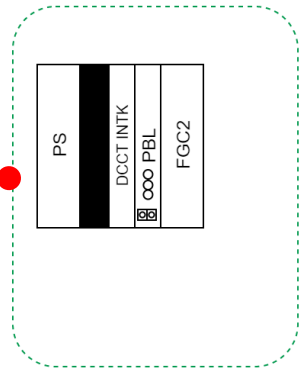
- FGC2 controller (CERN)
- Controller CPUs (COTS, but old design. Choice from GEPC*)
- Different purpose processing cards (propriety design from GEPC)
- The GEPC part of the controller is essentially handled by the POPS team with HW/SW EPC experts support limited to the FGC2

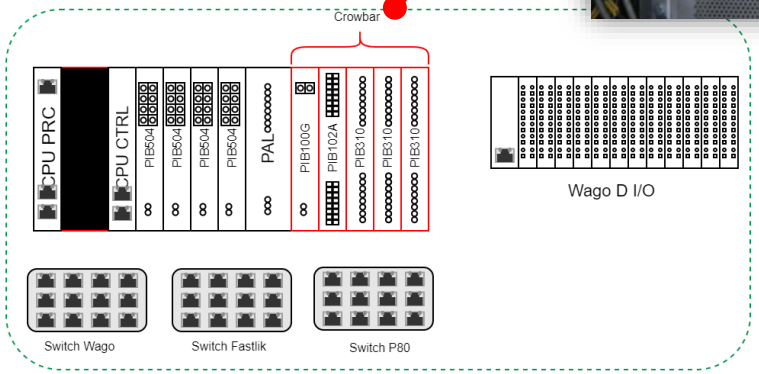
(*) GEPC = General Electric Power Conversion

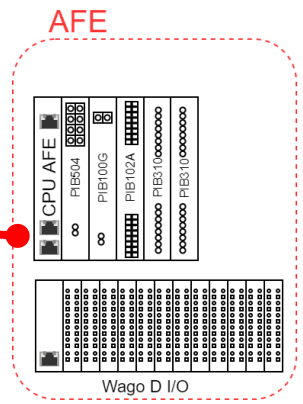
VME-7807RC GE-Fanuc











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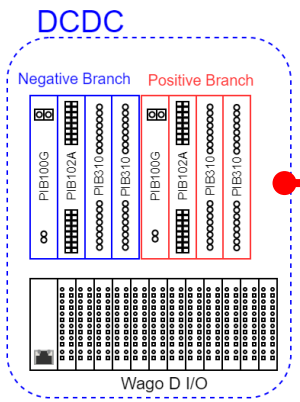

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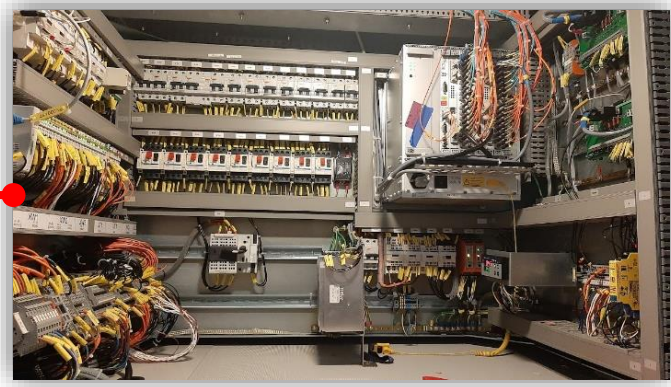


POPS control

Type of cards in operation	No. in operation	No. of spares	Comments
VME-7807RC CPU (GEPC)	4	5	One additional spare does not seem to work. To be retested
Pib100G (GEPC)	15	13(*)	2 replaced during 11 years of operation
Pib504 (GEPC)	6	5	1 replaced during 11 years of operation. Recently found HS
Pib102A (GEPC)	15	12	3 replaced during 11 years of operation
Pib310 (GEPC)	31	29	2 replaced during 11 years of operation
PAL (CERN)	1	2	0 replaced during 11 years of operation (but few upgrades were done)
FGC2 (CERN)	1	2	0 replaced during 11 years of operation
PBL (CERN)	1	1	0 replaced during 11 years of operation (but few upgrades were done)

- It is not possible to buy additional spares, because all cards have been put out of construction since years now.
- Overall, the VME control type showed to be robust so far and we believe that we have enough working spares.
- Nevertheless, POPS was already a special system back then for GEPC → the knowledge of the system is literally disappearing even by the manufacturer.

(*) Additional tests are ongoing.

When it all started…

- **September 29th, at 09:02:51**
  - Symptoms:
    - POPS not resettable.
    - No communication with the CTRL or PRC cards.
    - No post-mortem data generated by CTRL or PRC.
    - "*VS_COMMS*" → Issue between FGC and MC?
      - More specifically: between PBL and PAL cards?
  - Actions:
    - Visual inspection on site
    - P80i environment looked suspect
      - Re-load of CTRL and PRC libraries and files
    - Reset Main Controller

	STATE.PC	FLT_STOPPING	SET
	VS.STATE	INVALID	SET
	DIG.STATUS	VS_READY	CLR_BIT
	STATUS.FAULTS	VS_COMMS	SET_BIT
2022-09-29 09:02:51.201000	STATUS.WARNINGS	VS_COMMS	SET_BIT
	PAL.STATE	LINK_FAULT	SET
	PAL.LINKS.LOGGEDCONTROL	READY	CLR_BIT
	PAL.LINKS.STATUS	ON	CLR_BIT
	PAL.LINKS.STATUS	VME_IRQ_ENA	CLR_BIT
	VS.STATE	OFF	SET
	DIG.STATUS	VS_POWER_ON	CLR_BIT
	DIG.STATUS	PWR_FAILURE	SET_BIT
2022-09-29 09:02:51.206000	DIG.STATUS	VS_RUN	CLR_BIT
	STATUS.ST_UNLATCHED	LOG_PLEASE	SET_BIT
	STATUS.ST_UNLATCHED	VS_POWER_ON	CLR_BIT
	PAL.LINKS.LOGGEDCONTROL	POPSRUN	CLR_BIT

But then it continued…

- **Between the 1st and 4th of October:**
  - ~10 trips with required intervention of POPS team.
  - Begin of a process of replacement of cards…
  - … until the complete control rack (October 3rd).

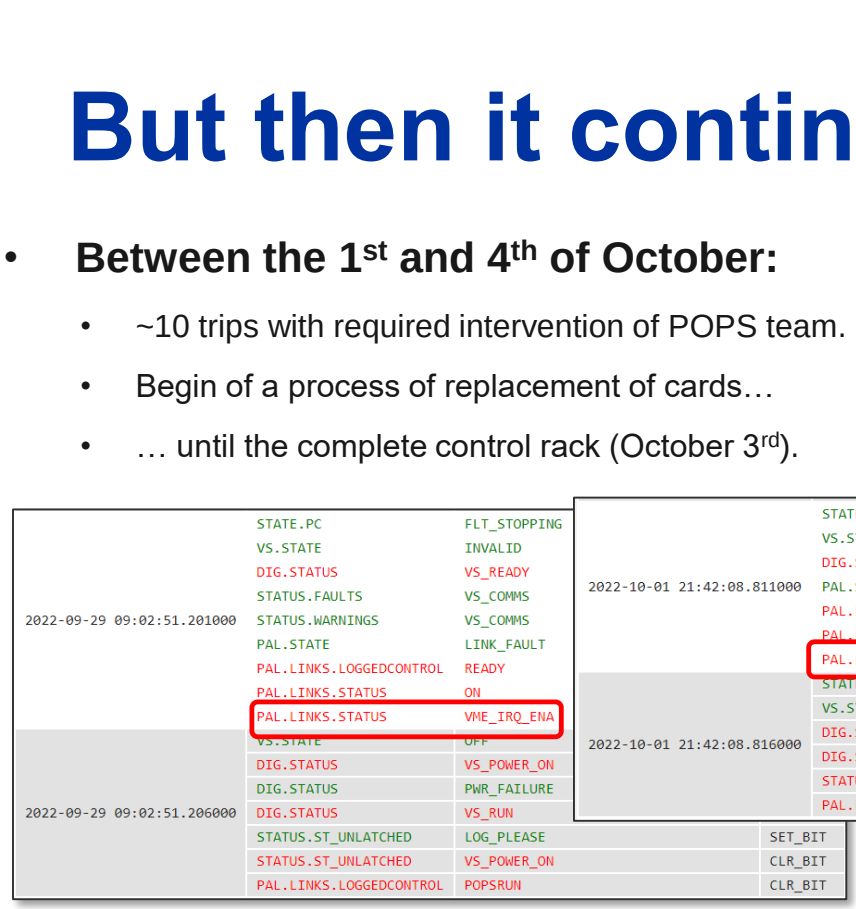
2022-09-29 09:02:51.201000	STATE.PC	FLT_STOPPING
	VS.STATE	INVALID
	DIG.STATUS	VS_READY
	STATUS.FAULTS	VS_COMMS
	STATUS.WARNINGS	VS_COMMS
	PAL.STATE	LINK_FAULT
	PAL.LINKS.LOGGEDCONTROL	READY
	PAL.LINKS.STATUS	ON
	PAL.LINKS.STATUS	VME_IRQ_ENA
2022-09-29 09:02:51.206000	VS.STATE	OFF
	DIG.STATUS	VS_POWER_ON
	DIG.STATUS	PWR_FAILURE
	DIG.STATUS	VS_RUN
	STATUS.ST_UNLATCHED	LOG_PLEASE SET_BIT
	STATUS.ST_UNLATCHED	VS_POWER_ON CLR_BIT
	PAL.LINKS.LOGGEDCONTROL	POPSRUN CLR_BIT

2022-10-01 21:42:08.811000	STATE.PC	FLT_STOPPING
	VS.STATE	INVALID
	DIG.STATUS	VS_READY
	PAL.STATE	LINK_FAULT
	PAL.LINKS.LOGGEDCONTROL	READY
	PAL.LINKS.STATUS	ON
	PAL.LINKS.STATUS	VME_IRQ_ENA
2022-10-01 21:42:08.816000	STATE.PC	STOPPING
	VS.STATE	OFF
	DIG.STATUS	VS_POWER_ON
	DIG.STATUS	VS_RUN
	STATUS.ST_UNLATCHED	VS_POWER_ON CLR_BIT
	PAL.LINKS.LOGGEDCONTROL	POPSRUN CLR_BIT

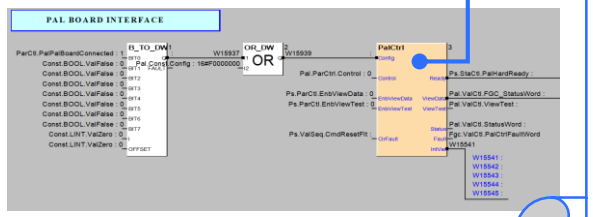
2022-10-02 20:37:00.916000	STATE.PC	FLT_STOPPING
	VS.STATE	INVALID
	DIG.STATUS	VS_READY
	PAL.STATE	LINK_FAULT
	PAL.LINKS.STATUS	ON
	PAL.LINKS.STATUS	VME_IRQ_ENA
2022-10-02 20:37:00.921000	STATE.PC	STOPPING
	VS.STATE	OFF
	DIG.STATUS	VS_POWER_ON
	DIG.STATUS	VS_RUN
	STATUS.FAULTS	VS_COMMS
	STATUS.WARNINGS	VS_COMMS
	STATUS.ST_UNLATCHED	VS_POWER_ON CLR_BIT
	PAL.LINKS.LOGGEDCONTROL	READY CLR_BIT
	PAL.LINKS.LOGGEDCONTROL	POPSRUN CLR_BIT

2022-10-08 15:08:54.851000	STATE.PC	FLT_STOPPING SET
	VS.STATE	INVALID SET
	DIG.STATUS	VS_READY CLR_BIT
	PAL.STATE	LINK_FAULT SET
	PAL.LINKS.LOGGEDCONTROL	READY CLR_BIT
	PAL.LINKS.STATUS	ON CLR_BIT
	PAL.LINKS.STATUS	VME_IRQ_ENA CLR_BIT
2022-10-08 15:08:54.856000	STATE.PC	STOPPING SET
	VS.STATE	OFF SET
	DIG.STATUS	VS_POWER_ON CLR_BIT
	DIG.STATUS	VS_RUN CLR_BIT
	STATUS.ST_UNLATCHED	VS_POWER_ON CLR_BIT
	PAL.LINKS.LOGGEDCONTROL	POPSRUN CLR_BIT

- **A common failure path started to emerge: VME_IRQ_ENA register**
  - The master CPU reset the VME_IRQ_ENA register written at dual-ported RAM of the PAL card
  - Allow PAL and FGC to send Interrupt Request to VME chassis
  - No synchronization, no Main Controller.
    - The MC was orderly shutting down in the middle of the run!



VME_IRQ_ENA register writing logic



Search for suspects

- **Controller update during TS2**
  - New software for improved DC/DC management
  - New FGC2 class

  → Versions' rollback on October 13th

- **Network switches**
  - VS_COMMS fault
  - Doubts about P80 connection

  → Installation of new switches

- **Faulted electronic card**
  - All control cards of both the MC and FGC2 have been replaced with spares;

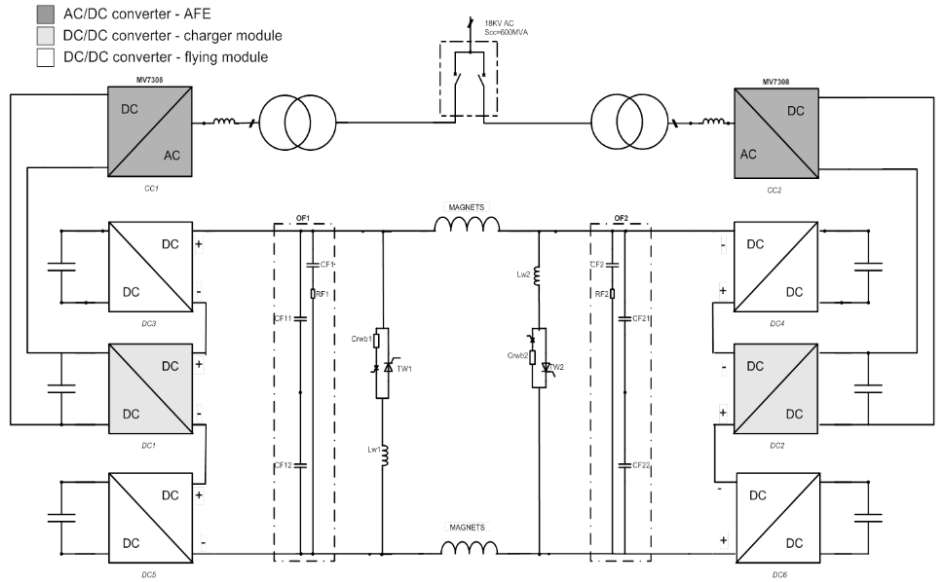
  → Systematic replacement of cards, however tedious process as very often it resulted in unforeseen problems; Several resets required!

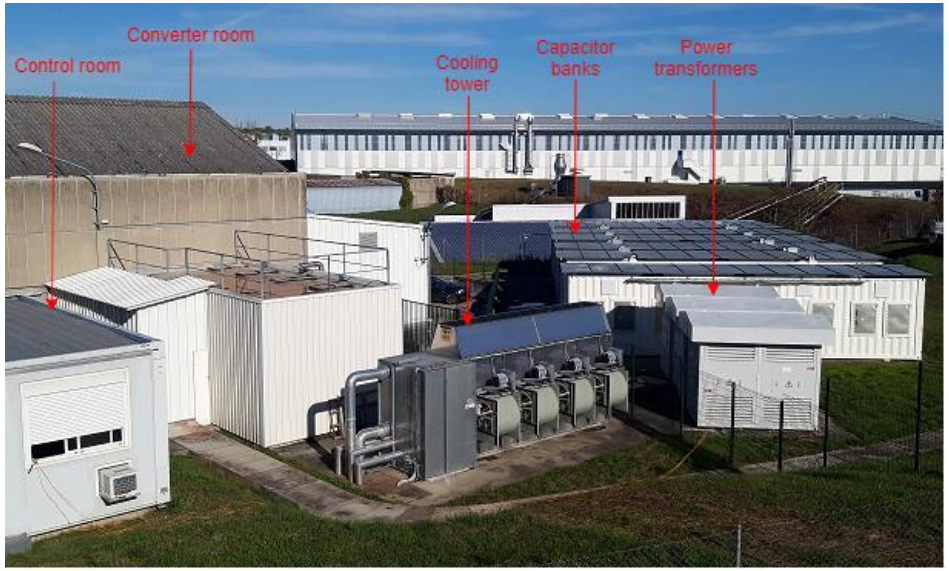
- **Power supply**
  - Following exchange with other experts at CERN
  - Experience from other converters

  → Dedicated measurements and installation of spare units

Difficulties along the way…

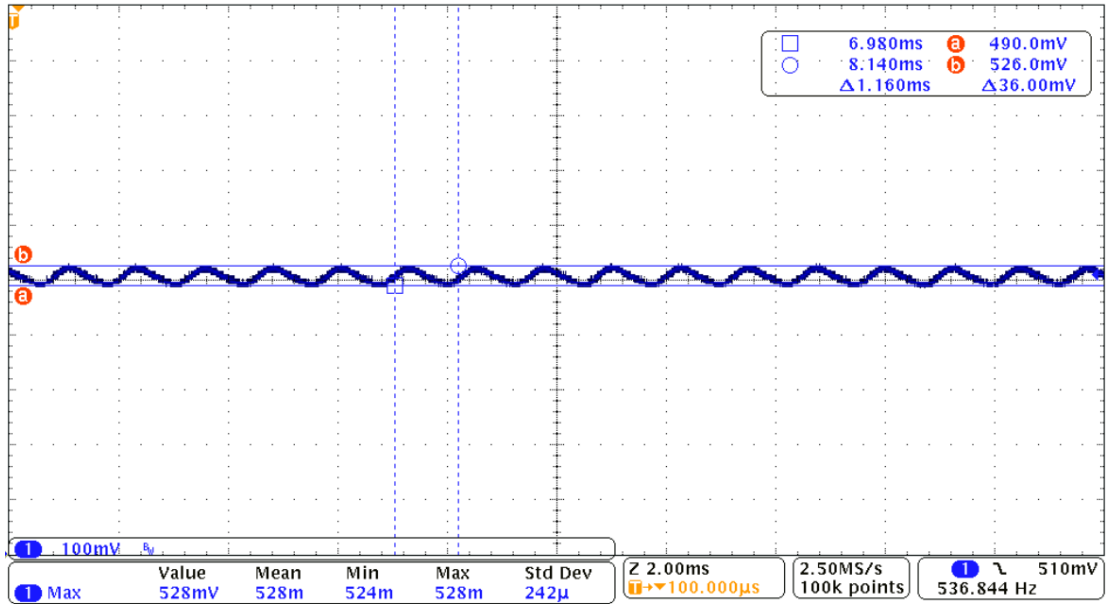
- **POPS is “not only a converter”**
  - Overall behavior is hardly (perfectly) reproduceable “offline”
- **Non reproducibility of results after cards swap**
- **POPS: turnkey project with more than 10 years**
  - **Turnkey project:**
    - Finest details (cards/electronics) are not known to CERN
  - **(…) more than 10 years:**
    - Typical life-cycle of industrial control systems: 10 years
      - Obsolescence → purchase of additional spare parts impossible
    - Knowledge on Manufacturer’s side not necessarily maintained
  - **Consequences:**
    - longer reaction times, risky to test on spares, …

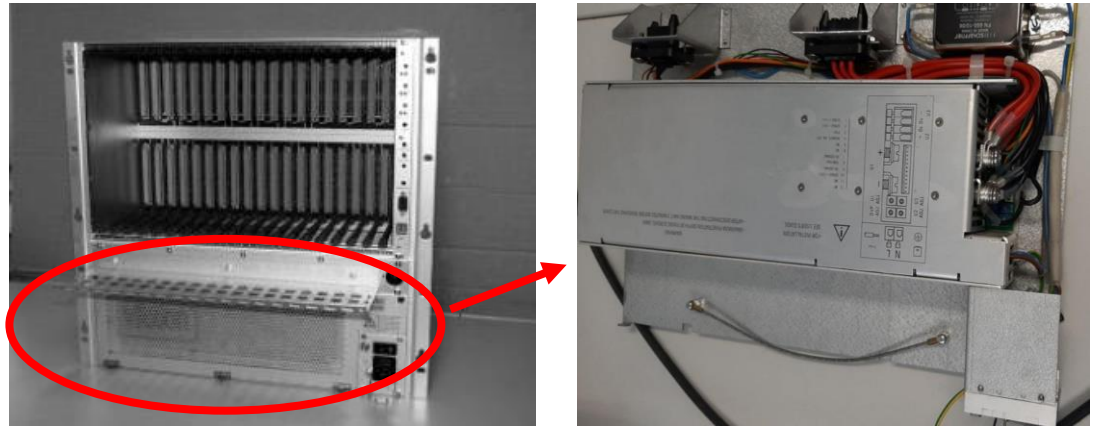




Power supply of the VME chassis

- **Built-in to the Schroff chassis**
  - +5V (100A), +12V (8A), -12V (6A)
  - The 24V for the fans is taken from the ±12V → Very bad idea!
  - Specification: max. ripple of 50mVpp
- **POPS measurements:**
  - 5V → ~300mVpp ripple **(!)**





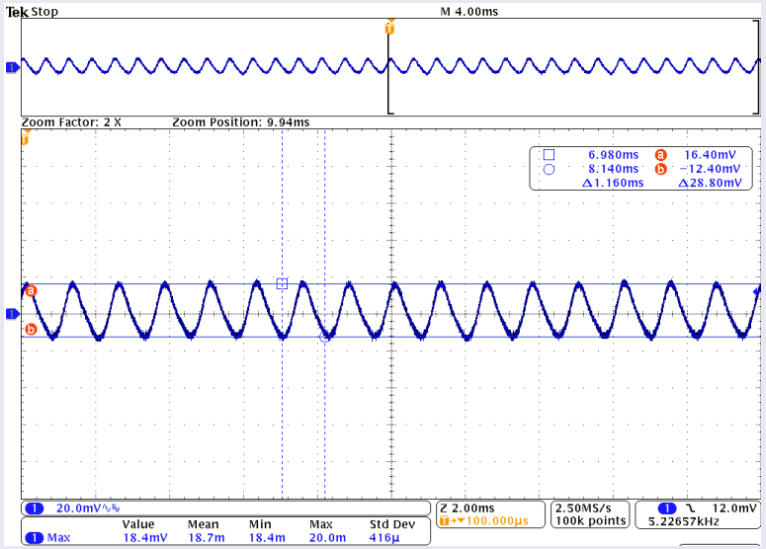
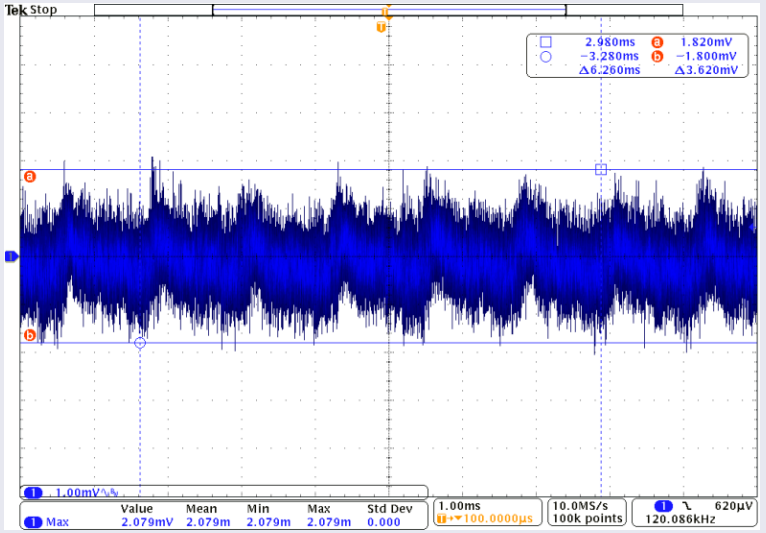
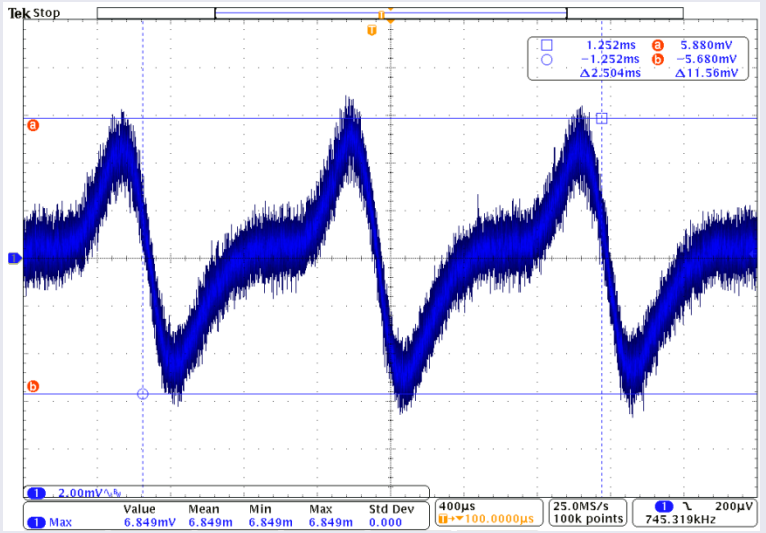
VME (20 slots) - Schroff BGTR 10HE Power supply

5.0 Power Supply Tray

5.1 PSU data

Input data :
Nominal voltage 90-264VAC Autorange, PFC complying with EN 61000-3-2
Max AC inrush current : < 25A
Max AC input current : < 10A
Efficiency (U_I = 230V) : 75%
PSU Input fuse : on line L, value 15A, dimensions 6.3 x 32mm
Output data :
Output voltages : 5V/100A, 12V/8A, 12V/6A
Available output power : 600W (that means that all 3 outputs cannot deliver 100% of power simultaneously)
Line regulation : +/- 0.1%
Load regulation : Output 1 : +/- 0.1% of Unom, Output 2 : +/- 0.2% of Unom,
Output 3 : +/- 05% of Unom
Ripple : max. 50mVpp
Protection : Overvoltage on all outputs ,current limitation, excessive temperature
Operation range : 0°C to 70°C, derating (on overall W per PSU) 50°C to 70°C = 2,5% per °C
Signals : Power Fail, FANFAIL
Hold up time after assertion of AC Fail : >= 20ms (at full load)

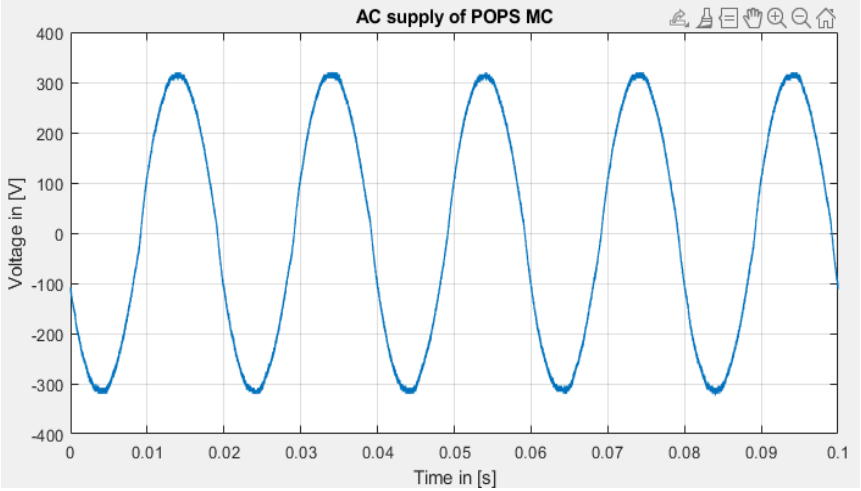
Measurements (1/2)

5V	+12V	-12V
• 300 mVpp ripple • 800 Hz	• 36 mVpp ripple • within specs	• 120 mVpp ripple • 800 Hz
		

- **Why 800 Hz ?!**
- **To add to the complexity: oscillations behavior non reproduceable after cards swap, MC resets, …**

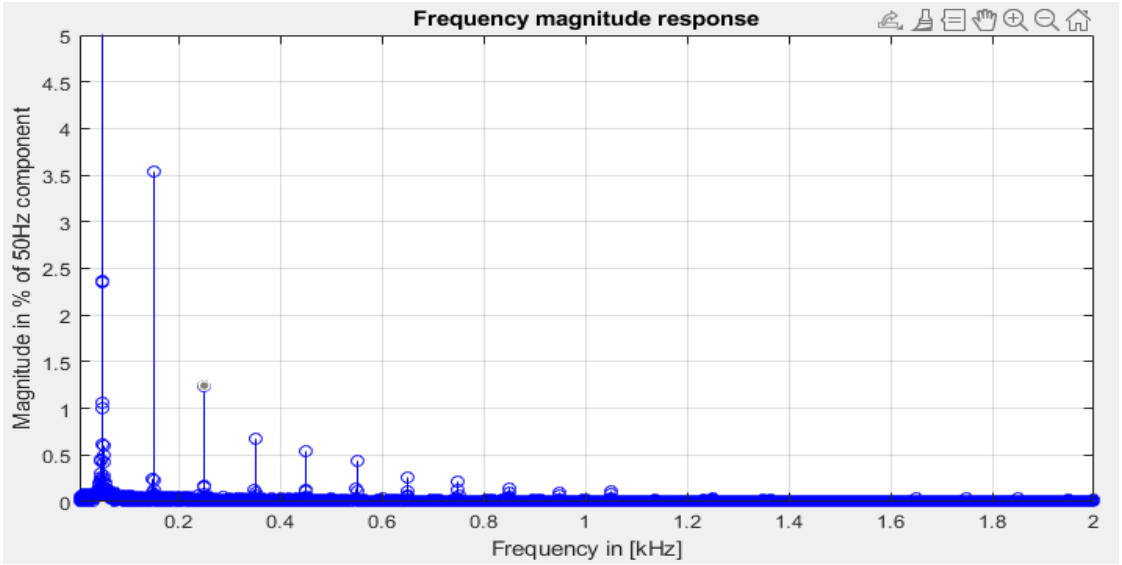
Measurements (2/2)

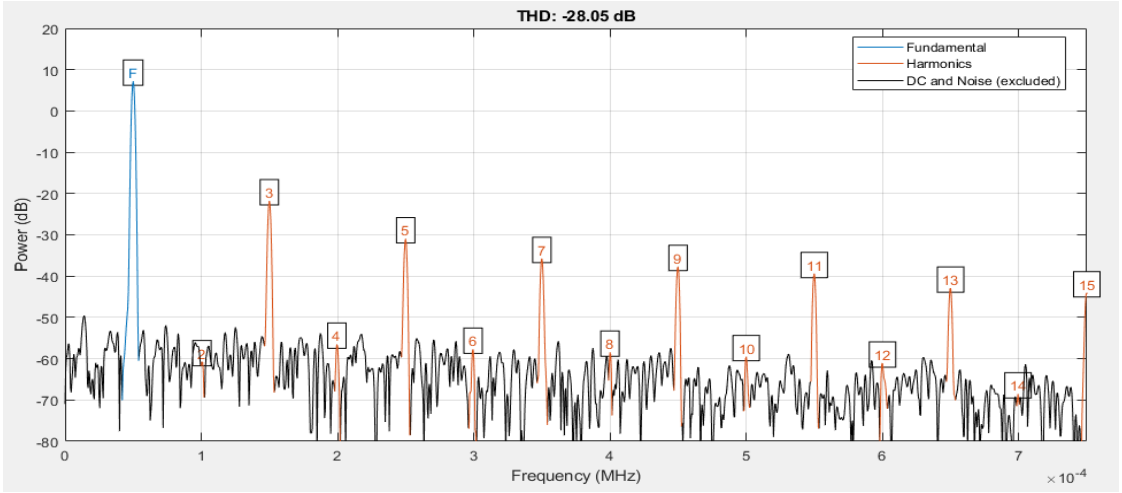
- **Can it be caused by its AC Power Supply?**



Recent dedicated tests with AC power supply exclude this hypothesis !

Common mode voltage still to be checked !





THD ~ 5%

- **EN 50160: 8%**
- **IEEE 519: 5%**

Mitigation of power supply DC voltages

- **First attempt: spare power supplies**
  - Spare 1 (never used, ~10 years old): did not solve the problem!
  - Spare 2 (~10 years in use in the spare chassis): did not solve the problem!
  - New power supply (should replace the “old” ones): non compatible!
    - Oscillations persisted in all cases…

      … were the oscillations there from the beginning? …

- **Second attempt: capacitors**
  - Additional 10mF installed into the output filter
  - However, it started well…

    … but after around 30 minutes the oscillations appeared once again !
  - **Another example of “strange behavior” (non reproduceable) throughout process (!)**

Problem Solved

- **Final attempt**
  - Motivated by discussions with RF experts on similar problems
  - Knowledge about the VMEbus → SysFail → Orderly shutdown of cards in MC

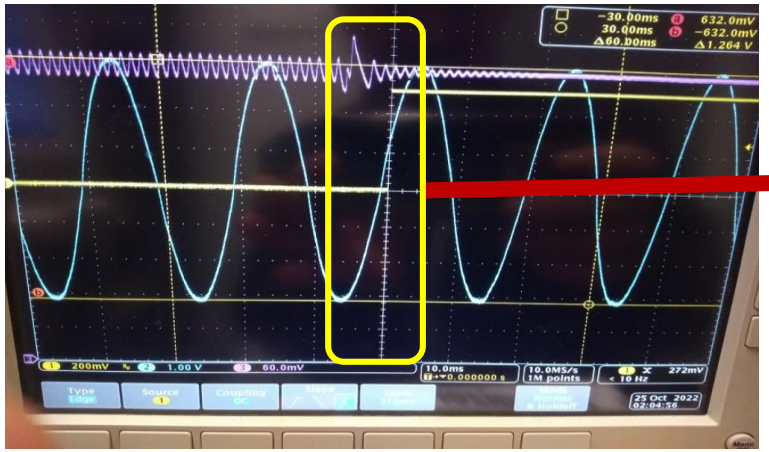


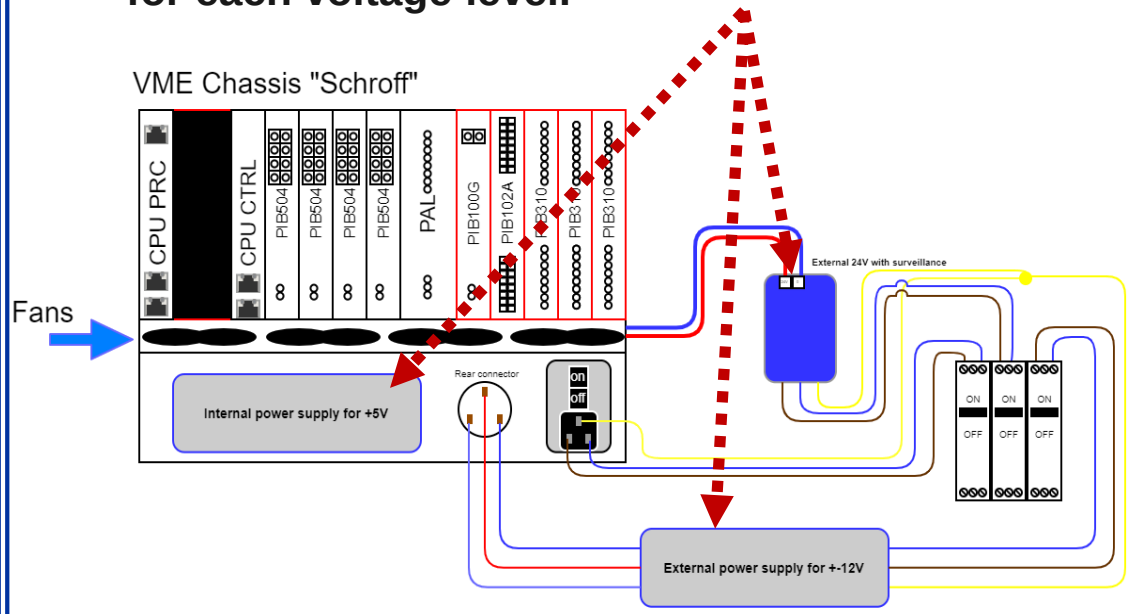
Figure taken during POPS intervention!

5V, SysFail, AC voltages during a real POPS trip

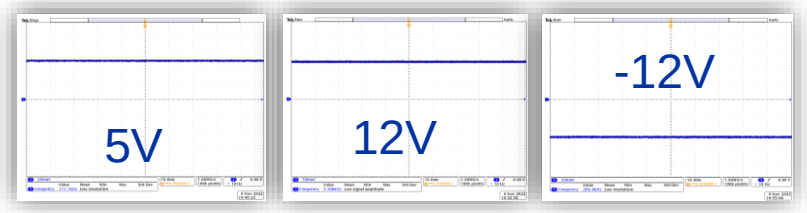
Strengthen the doubt of a PS problem

- **Implementation on October 26th … and, since, POPS runs stably!**

- **“Frankenstein” approach: 1 power supply for each voltage level.**

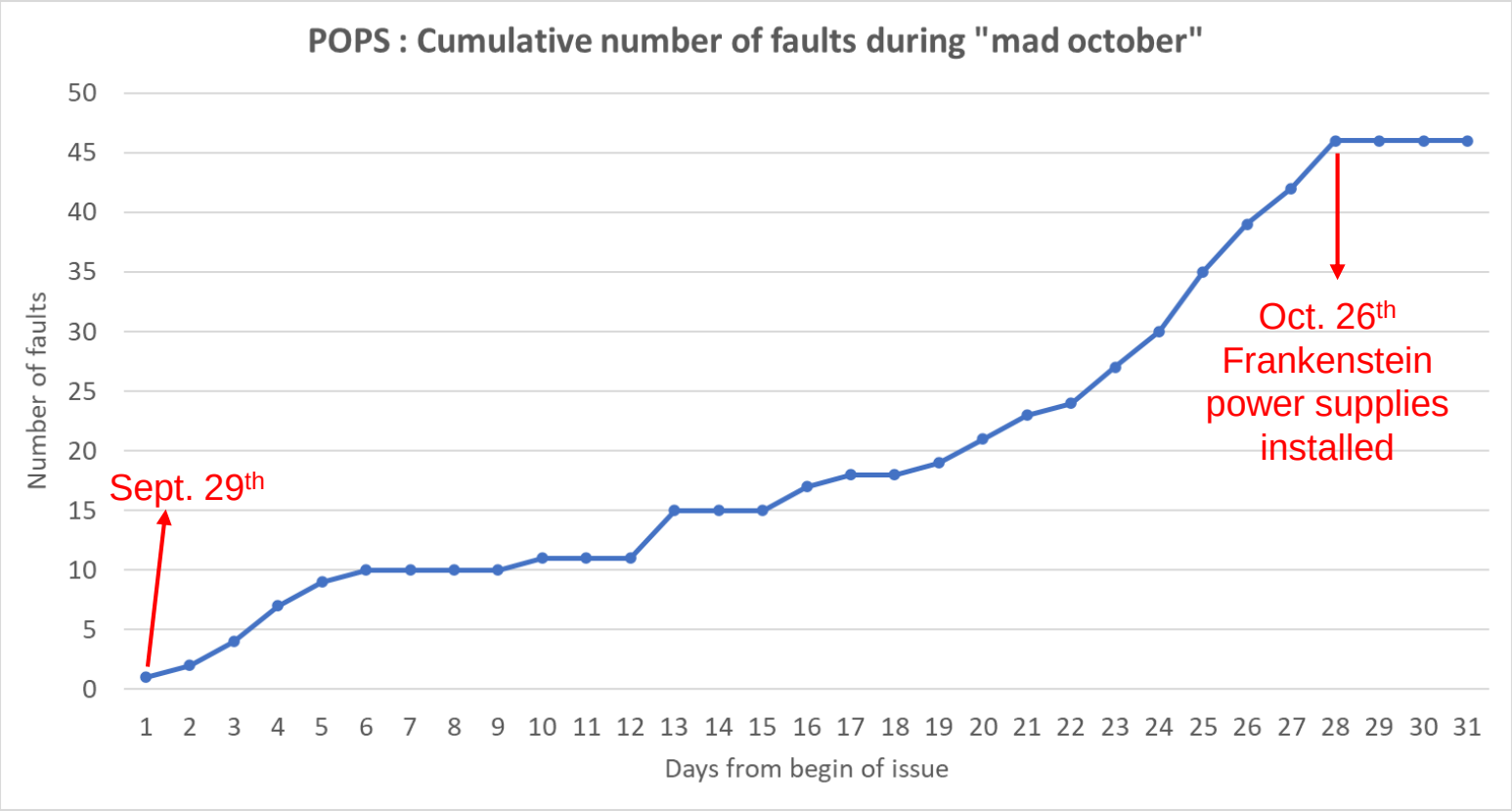


Ripple-free voltage levels in Frankenstein ps



Glimpse into the statistics (1/3)

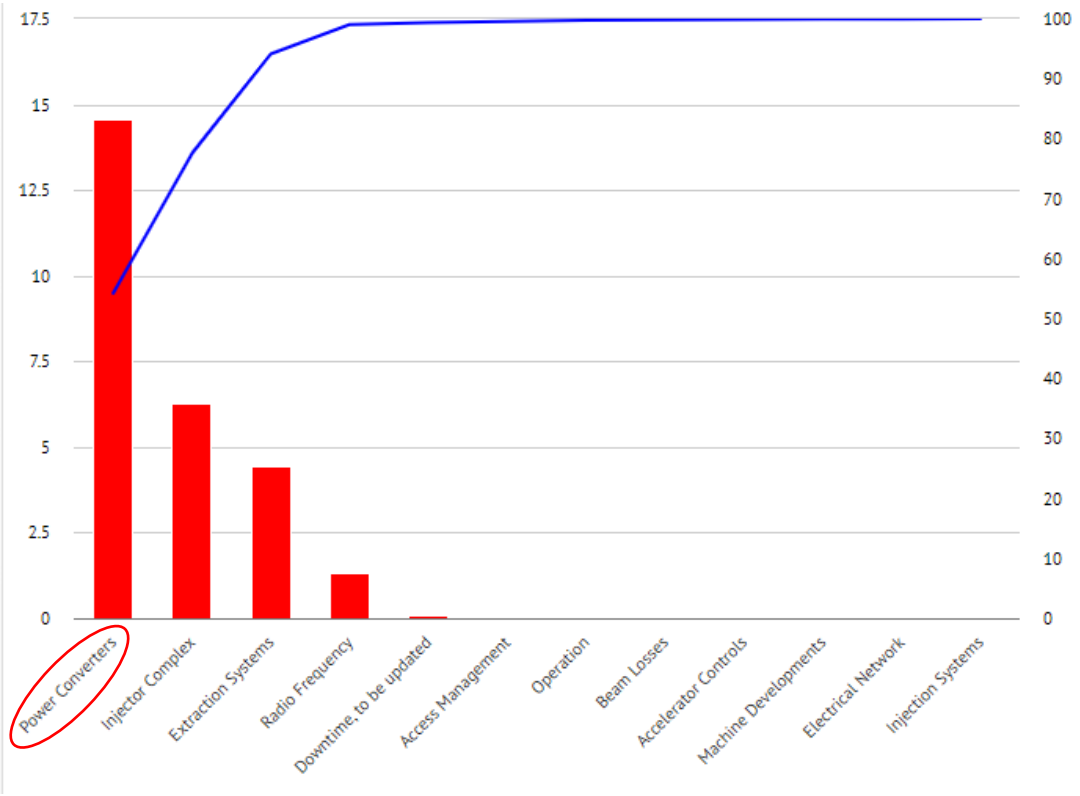
- **Number of trips during “Mad October”**



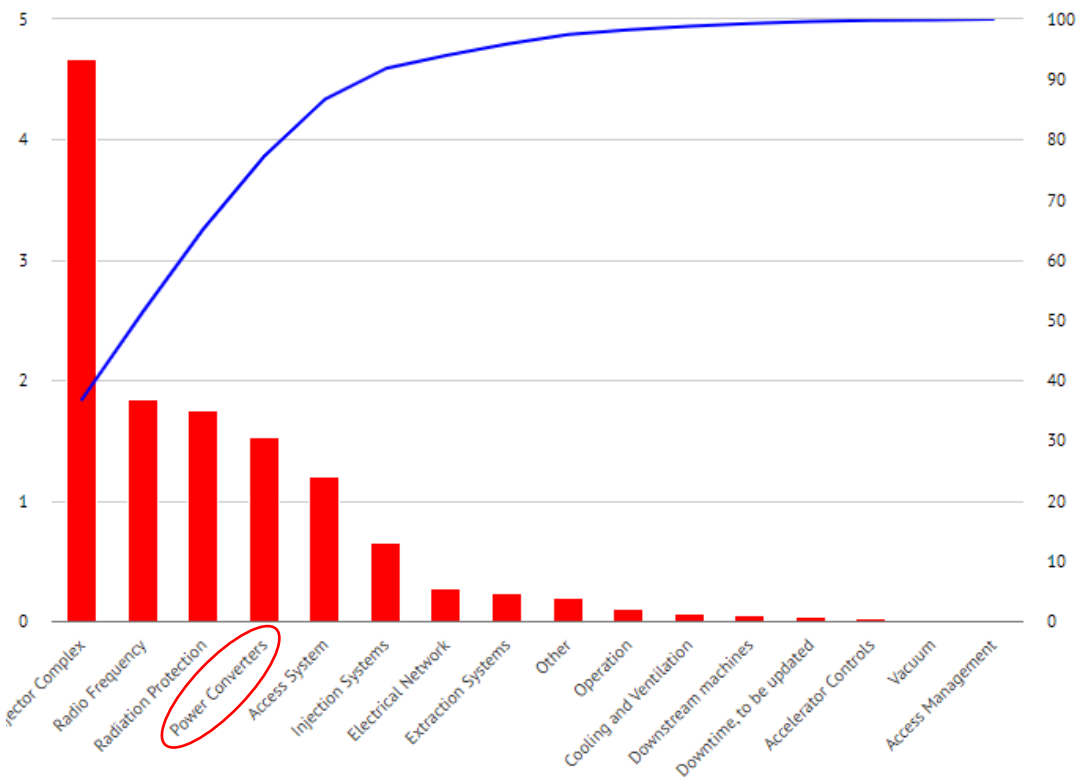
Glimpse into the statistics (2/3)

- **Overview of PS Accelerator unavailability**

- **“Mad October” (Sept. 29th to Oct. 29th)**

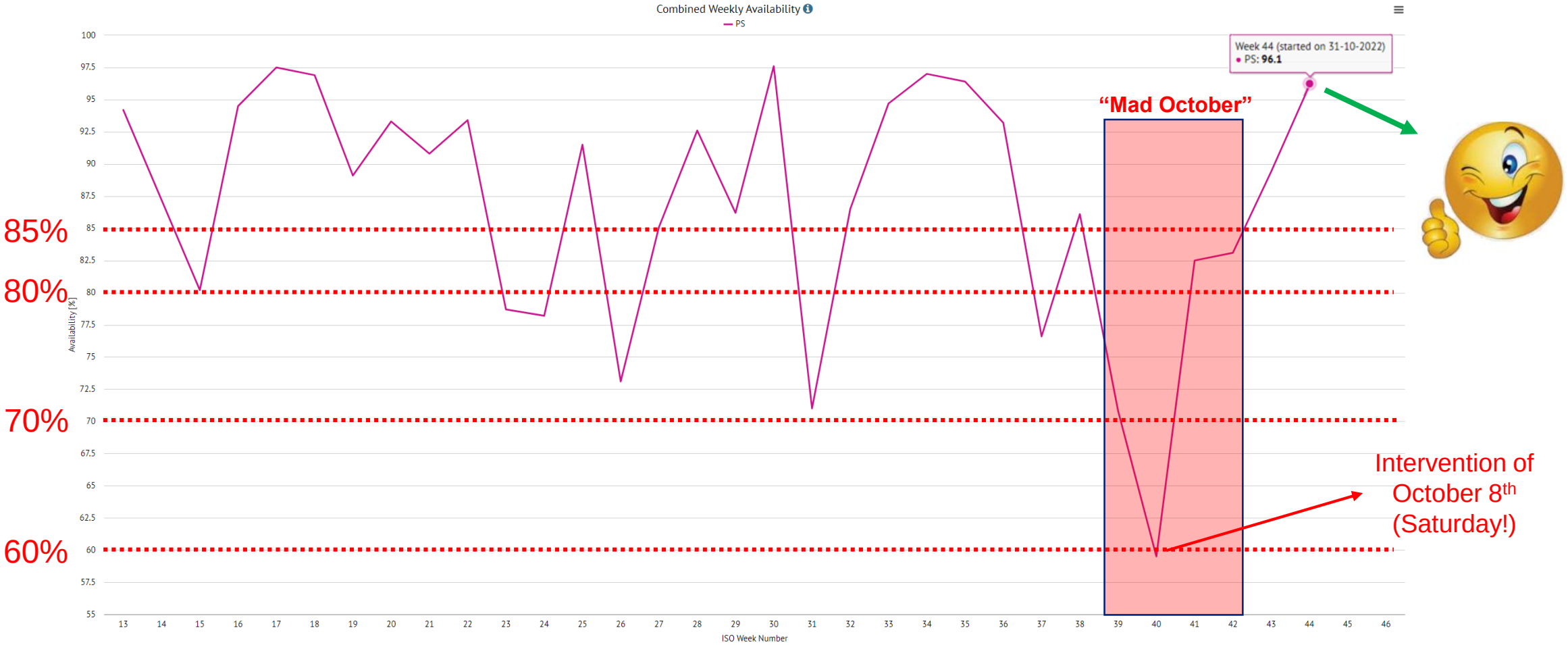


- **“Rest of the year” (May 1st to Aug. 31st)**



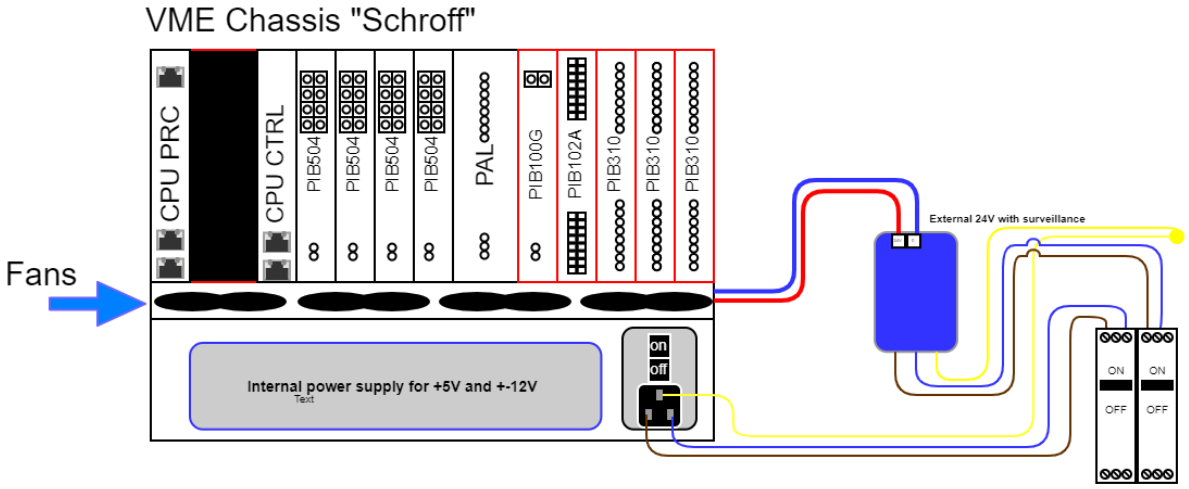
Glimpse into the statistics (3/3)

- **Combined Weekly Availability from “Accelerator Fault Tracking”:**



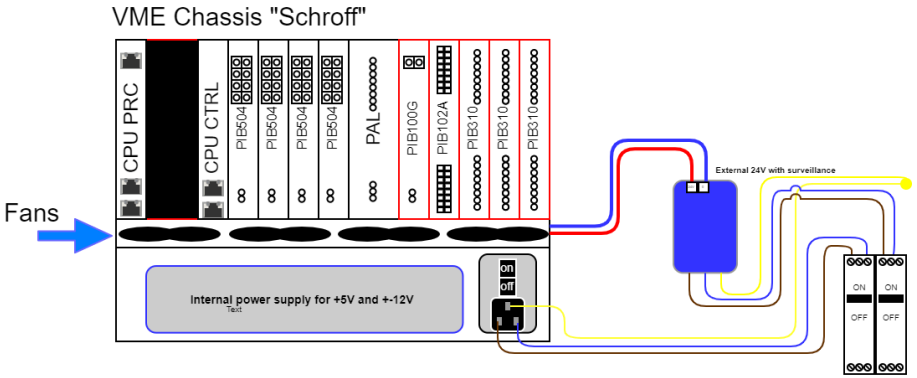
Only possible thanks to “Procedures (including “reset”) + EPC piquet team”!

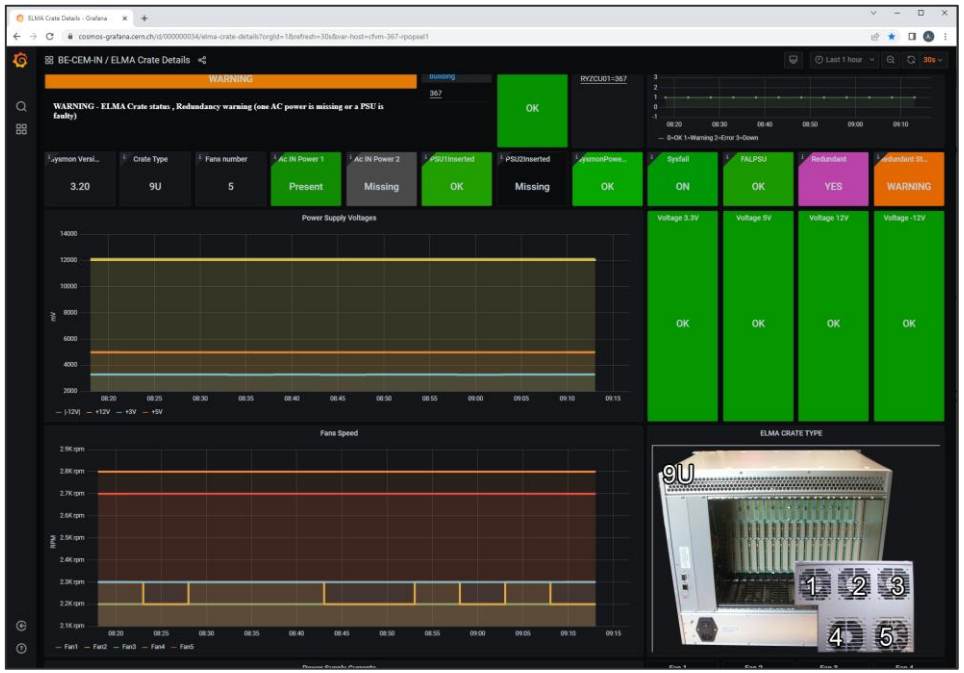
What is next? (short term)



1) **Replacement of the Frankestein with more robust solution**
   i. Alternative power supply for +5V and ±12V that fits into the chassis plus an external 24V for the fans
      i. Two units ordered

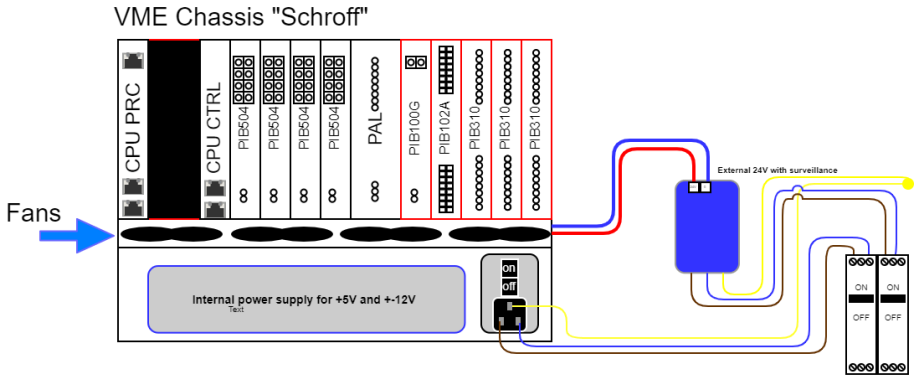
What is next? (short term)

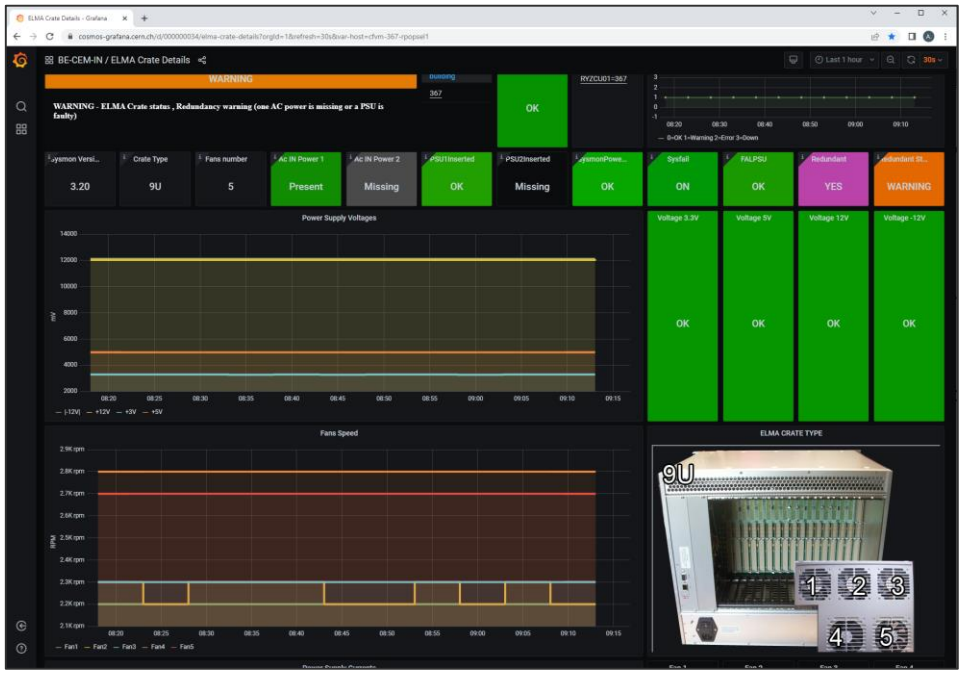




1) **Replacement of the Frankestein with more robust solution**
   i. Alternative power supply for +5V and ±12V that fits into the chassis plus an external 24V for the fans
      i. Two units ordered
   ii. Replacement of the entire chassis with a higher quality model from ELMA, widely used at CERN
      i. First tests **not** successful

What is next? (short term)





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     - i. First tests **not** successful

2) **Test of all main spare control cards**
   - i. Nearly all main “intelligent” GEPC spare cards have been tested
     - i. one CPU and one data transmission cards found not working
     - ii. overall number of spare control cards seems adequate
     - iii. additional tests ongoing for PIB100G

3) **Try and find additional control cards**
   - i. GEPC is looking for additional spare from serviced units (not new)
     - i. Some cards found and presently under test in GEPC

What is next? (medium term, LS3)

1) Replacement of the POPS controller (POPS+ project) with CERN HW

i. It is part of the POPS+ project that aims in addition, at increasing the reconfiguration modes of POPS

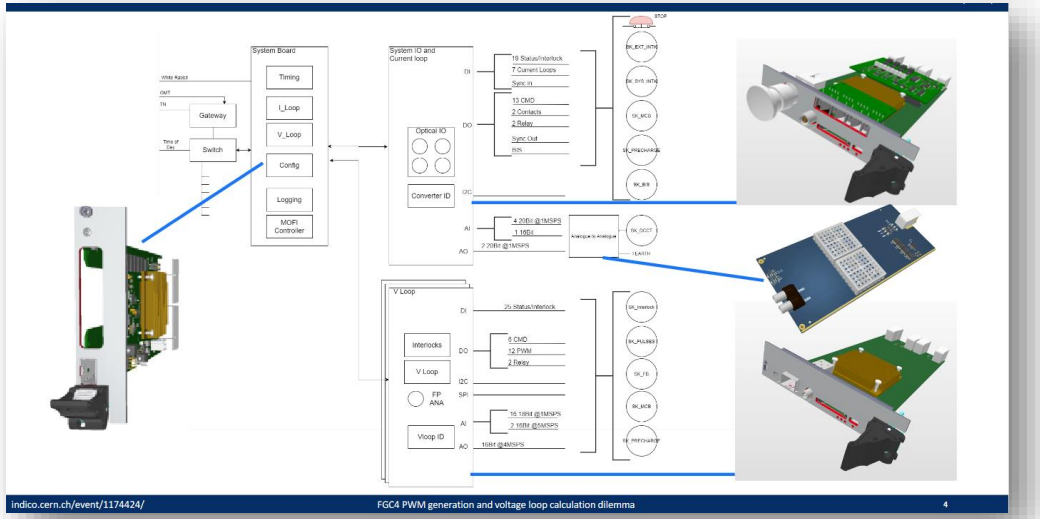
ii. It is in line with the development of the new FGC4 control platform of the EPC group

iii. It is badly needed.

2) Increased participation of control HW/SW experts

i. Presently limited because the POPS control is not CERN based (80% of it);

ii. Will naturally be extended once we adopt the next generation FGC4 control architecture;

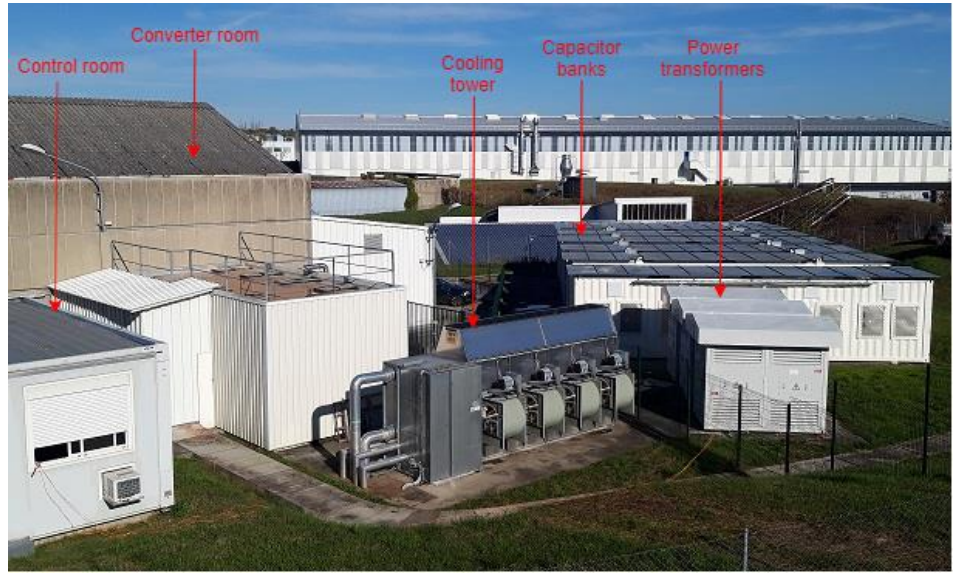


FGC4 preliminary architecture

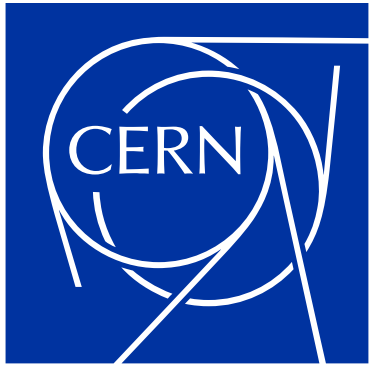
i. FGC4 modern approach (distributed structures) is necessary for POPS+

ii. ACCCONS funds now available for FGC4 project

Conclusions



- **The mad October problem has been solved**
  - Keep doubting (!)…even after the replacement of 3 power supplies (!)
  - We plan to further investigate it. Why suddenly all power supplies have been affected?
- **Spare "intelligent" cards have nearly all been tested**
  - The number of spare parts seems adequate for the next 3-4 years;
  - Some (few) additional spare are under test by the supplier;
- **POPS tests and interventions are complex**
  - The control system is prone to non repetitive "strange" behaviors.
  - Several communication layers that (unnecessarily) complicate overall control structure.
  - Time is needed for troubleshooting.
- **Long term (LS3) solution is FGC4 control architecture for POPS+**
  - Keyword for the new controller is: $(\text{simplify})^3+(\text{standardize})^2$
  - Common spare parts management with EPC controls;
  - Group level support for HW / SW problems;
  - Generous dedicated test time shall be agreed for the new control system during LS3 !



Thanks.

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